IOP 480 AA

Design Note Rev. 1.3
March 2002

Design Note Documentation

A. Affected Silicon Revision

This document details Design Notes for the following silicon:

Product	Part Number	Description	Status
IOP 480 AA	IOP480-AA60PI	60MHz Local Bus 208-pin PQFP Product	In production October 1999
IOP 480 AA	IOP480-AA66PI	66MHz Local Bus 208-pin PQFP Product	In production October 1999
IOP 480 AA	IOP480-AA60BI	60MHz Local Bus 225-pin PBGA Product	In production October 1999
IOP 480 AA	IOP480-AA66BI	66MHz Local Bus 225-pin PBGA Product	In production October 1999

B. Documentation Status

The following documentation is the baseline functional description of the silicon. Errata are defined as behaviors in the affected silicon that do not match behaviors detailed in this documentation.

Document	Revision	Description	Publication Date
IOP 480 Data Book	2.0	Released Data Book	July 2000
IOP 480 AA Errata	See www.plxtech.com for latest revision	IOP 480 Errata Documentation	

C. Design Note Summary

#	Description
1	End-of-Transfer (EOT) During Chaining DMA End Link Mode with Write-back
2	DMA Channel 2 with End-of-Transfer (EOTx#) asserted coincident with ADS#
3	Zero Wait State SRAM Writes
4	External local master write to IOP 480 internal configuration registers with WAIT# being used to insert wait states
5	Modifying internal configuration registers that affect on-going transfers
6	Operation of IOP 480 Buffers in 3.3 Volt Signaling Environment
7	LCSx# Chip Select output delayed when IOP 480 is initiating access to SRAM
8	CompactPCI Hot Swap Insertion Bit Status
9	DMPAF# (Direct Master Programmable Almost Full) negation timing
10	Messaging Unit data corruption if Queue Prefetch (Inbound Free List FIFO Prefetch and/or Outbound Post List FIFO Prefetch) is enabled
11	Local Bus Timeout with SDRAM
12	WAIT# input signal when using the Memory Controller

13	ALE Output Timing
14	PCI Delayed Read Mode bit (PCICTL[25])
15	Power Management Interface Specification version support

D. Design Notes

1. End-of-Transfer (EOT) During Chaining DMA End Link Mode with Write-back

Design Issue:

When write back cycles are enabled (C0MODE[16]=1 and/or C1MODE[16]=1) during DMA transfers with chaining enabled (C0MODE[9]=1 and/or C1MODE[9]=1), the IOP 480 will write back to the DMA descriptor a value of zero in the byte count field. However, if the EOTx# End Link mode is also enabled (C0MODE[20]=1 and/or C1MODE[20]=1) and an EOTx# occurs right as the last data in the DMA link has been transferred, the subsequent write back of zero happens twice. Both write backs will write to the same address with the same value 0 (zero).

Recommendation:

There should be no noticeable impact except for waveforms looking a bit odd.

2. DMA Channel 2 with End-of-Transfer (EOTx#) asserted coincident with ADS#

Design Issue:

If an End of Transfer (EOTx#) is asserted when the IOP 480 is asserting ADS# during a DMA Channel 2 transfer, two (2) words will be transferred rather than one (1) word before the DMA terminates. DMA 0 and 1, on the other hand, transfer only one (1) word if an EOTx# is asserted on the same clock cycle as ADS#.

3. Zero Wait State SRAM Writes

Design Issue:

The memory controller configuration registers allow settings for zero wait state SRAM writes. However, the IOP 480 does not support zero wait state writes to asynchronous SRAM on the local bus. Zero wait state reads from external asynchronous SRAM are unaffected as they do not require the toggling of the MWE# signal.

Recommendations:

1. Use 1 wait state writes when accessing external asynchronous SRAM (WDD=1).
2. Use SDRAM instead of SRAM for fast accesses to memory.
3. Use SBSRAM.

4. External local master write to IOP 480 internal configuration registers with WAIT# being used to insert wait states

Design Issue:

The WAIT# input can be used by an external local bus master to insert wait states when accessing the IOP 480 internal configuration registers or when accessing the PCI bus during Direct Master accesses.

During a configuration write, WAIT# must be asserted (by the external local master) a minimum of two (2) clocks before READY# is asserted by the IOP 480, for the IOP 480 to sense the WAIT# input. The earliest READY# will be asserted is seven (7) clocks after the assertion of ADS#. Therefore, in order to ensure that WAIT# is recognized by the IOP 480, WAIT# should be asserted no later than five (5) clocks after the assertion of ADS#. Any assertion of WAIT# more than five (5) clocks after the assertion of ADS# may be ignored by the IOP 480.

If the IOP 480 does not sense WAIT# it will simply assert READY# for one clock (and think the cycle has ended) instead of waiting until WAIT# has been negated. This problem applies only when an external local master is writing to the IOP 480 internal configuration registers.

Recommendation:

During a Local Master write to the IOP 480 internal configuration registers, assert WAIT# no later than five (5) clocks after the assertion of ADS#, which will ensure that the IOP 480 recognizes WAIT# at least two (2) clocks before it asserts READY#.

5. Modifying internal configuration registers that affect on-going transfers

Design Issue:

IOP 480 internal register settings (which modify ongoing cycles) should not be modified until the chip is no longer doing such cycles. For example, turning off Burst Enable in the middle of a burst is prohibited.

6. Operation of IOP 480 Buffers in 3.3 Volt Signaling Environment

Design Issue:

The IOP 480 has universal buffers that were designed to operate in either a 5 Volt or 3.3 Volt signaling environment. The IOP 480 has a 3.3 Volt core and the I/O buffers are 5 Volt tolerant.

The PCI v2.2 specification specifies clamp diodes to both ground and VCC when operating in 3.3 Volt signaling environment. In the 5 Volt signaling environment, the high clamp diode is optional. The purpose of the clamp diodes is to ensure the reliability and signal integrity of the receiving devices when there are excessive voltage transients on the bus and to improve PCI bus signal integrity.

The IOP 480 buffers have a clamp diode to ground, but no single diode to VCC (The IOP 480 actually has several diodes in series). Based on reliability and signal integrity evaluations, the IOP 480 will operate properly in both 5 Volt and 3.3 Volt signaling environments in likely circuit configurations even though it has multiple high clamp diodes in series. Some of the results of circuit simulations are described below. If the IOP 480 is to be used in a configuration that exceeds the conditions of these simulations, please contact PLX.

- The IOP 480 buffers are not susceptible to damage from input signal voltage transients called out by the specification (up to 7.1 Volts). In fact, the IOP 480 will operate reliably withstanding voltage spikes as high as 11 Volts.

- The response of the IOP 480 PCI input buffers were simulated under various extreme configurations. For example, with a 12” PCI trace length, 90 Ohms bus impedance, 0 degrees Celsius, 3.6 Volts and being driven by a strong output buffer (the IOP 480 output buffer has 35 Ohm output impedance), the IOP 480 correctly interpreted the distorted digital waveform into the correct ideal digital waveform. Graphs of this and other waveforms are available from your PLX Area Sales Managers or FAEs.

Therefore, if the IOP 480 is part of a 3.3 Volt circuit that connects to other PCI devices, it will properly interpret distorted signals. If there are non-IOP 480 devices on the PCI bus, they will also be able to interpret distorted signals properly if they contain high clamp diodes.

7. LCSx# Chip Select output delayed when IOP 480 is initiating access to SRAM

Design Issue:

If DRAM refresh cycles are enabled (default), ongoing refresh cycles will preempt LCSx# assertion. When the IOP 480 is about to initiate a cycle on the local bus (in one of the LCSx# regions), DRAM refresh cycles may come in and jump ahead of the LCSx# assertion. In this case, ADS#, ALE, and the local address will still be generated, but LCSx# will not be generated until the refresh cycle is completed. Any data being transferred will remain on the bus during this time (waiting for READY#), so as a result there is no impact to the data transfer. However, the multiplexed address on the LAD bus may have changed to data by the time LCSx# is finally generated (when the refresh cycle has ended).

Recommendation:

1. Latch the de-multiplexed address on the MA bus instead of the LAD bus.
2. Always latch addresses with ADS# or ALE regardless of LCSx#.
3. Turn off refresh cycles when not using DRAM.

8. CompactPCI Hot Swap Insertion Bit Status

Design Issue:

The IOP 480 Hot Swap insertion bit (HSCSR[7]) defaults to zero (0) after reset. This can be considered a violation of PICMG 2.1 R1.0 CompactPCI Hot Swap specification. This condition will cause a problem if the board switch is closed

prior to reset (RST#) being negated, or if the system has been powered up with the IOP 480 inserted.

Recommendation:

1. The board switch needs to be closed after PCI reset (RST#) is negated.
2. Software should always choose an Extraction procedure for the safe termination of the CompactPCI Hot Swap adapter from the backplane.

9. DMPAF# (Direct Master Programmable Almost Full) negation timing

Specification Clarification:

The multiplexed pin LCS0#/DMPAF# is configured for DMPAF# output functionality if the Local Bus Control register is set to 1 (LOCCTL[0]=1). The default pin configuration is LCS0# functionality.

DMPAF# pin output assertion relies on the programmable value in DMPBAM [12:8] to determine when to signal that the Direct Master Write FIFO is almost full. After DMPAF# assertion, the IOP 480 negates the DMPAF# pin upon the last word of the transfer entering into the Data Out Holding Register. The DMPAF# signal indicates the Direct Master Write FIFO status, not the completion of the transfer status.

10. Messaging Unit data corruption if Queue Prefetch (Inbound Free List FIFO Prefetch and/or Outbound Post List FIFO Prefetch) is enabled

Design Issue:

When the Messaging Unit is enabled (MQCR[0]=1), the Inbound Free List FIFO holds the message frame addresses (MFA) of available message Frames (available to an external PCI agent) in shared Local memory. The Outbound Post List FIFO holds the MFA of all currently posted messages (destined to an external PCI agent) that are in shared Local memory.

To reduce read latency, queue prefetching can be enabled (QSR[2]=1 and/or QSR[3]=1). However, if queue prefetching is enabled, the Messaging Unit data can return incorrect data due to internal updating of the pointers.

Recommendation:

Disable queue prefetching for the Messaging Unit by disabling the QSR register bits (QSR[2]=0 and QSR[3]=0, the default values).

11. Local Bus Timeout with SDRAM

Design Issue:

When a local bus transaction attempts to access an invalid address, the local bus timeout feature in the IOP 480 can be used to avoid hanging the local bus. However, when a local bus timeout occurs when there is SDRAM in the system, this will cause the SDRAM state machine back to the POWER ON state, requiring a re-initialization to start up again. When the SDRAM is in the POWER ON state, a refresh request cannot be issued, so that when the IOP 480 refresh timer expires, the refresh request will be logged but not completed. This will preclude any other transaction onto the local bus, and the local bus will hang.

Recommendations:

1. If using the IOP 480 with SDRAM, do not count on the local bus timeout feature to be able to recover from invalid address accesses.
2. Use software workarounds to recover from this condition.

12. WAIT# input signal when using the Memory Controller

Design Issue:

The WAIT# input signal is not recognized by the IOP480 memory controller during external local bus master transactions. Therefore, when WAIT# is asserted by the external local bus master during such a transaction, the memory controller will continue to carry out the transaction, ignoring the WAIT# input signal.

Recommendation:

The following solution should be implemented with external glue logic:

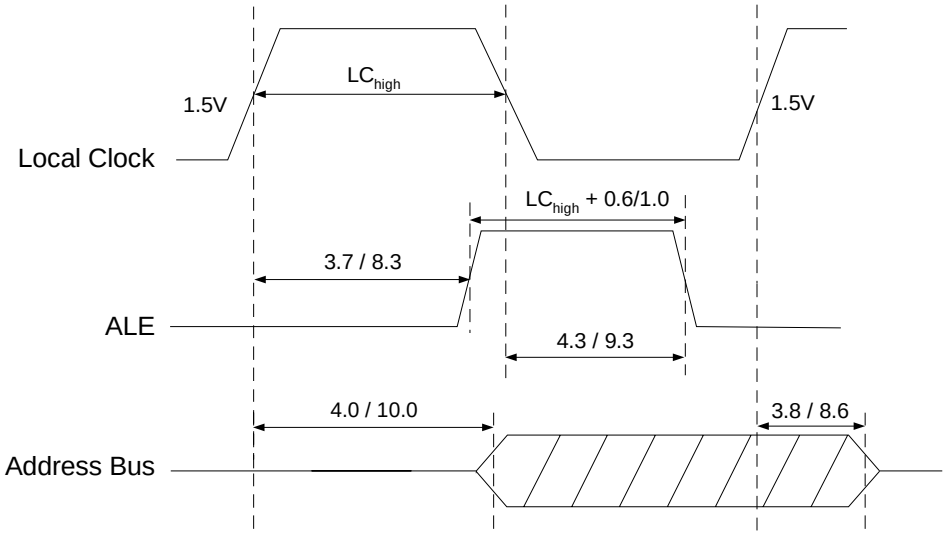
a) Monitor the local bus address and WAIT#.
b) If WAIT# is asserted to the IOP 480 while the IOP 480 memory controller is performing a transaction initiated by an external local bus master, assert BLAST# (to the IOP480) and assert a BOFF# (to the external master).

13. ALE Output Timing

Data Book Change:

Figure 19-1 in the IOP 480 Data Book r1.0 and r2.0 shows a Timing Diagram for the ALE signal that is incorrect. ALE timing is dependent on the Local Clock period, which was not shown in the existing diagram.

1. The following diagram correctly shows the ALE timing specifications:



14. PCI Delayed Read Mode bit (PCICTL[25])

Data Book Change:

The name for the PCI Bus Control register bit 25 (PCICTL[25]) is changed from “PCI Delayed Read Mode” to “PCI r2.1 Features Enable”. IOP 480 Data Book section 4.5, and the PCICTL[25] register bit description, are revised:

Register 17-63. (PCICTL; PCI:98h, LOC:98h) PCI Bus Control

Bit	Description	Read	Write	Value after Reset
25	***PCI r2.1* Features Enable.** When set to 1, the IOP 480 performs all PCI Read and Write transactions in compliance with PCI r2.1. Setting this bit enables Delayed Reads, 2^{15} PCI Clock timeout on Retries, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write Mode (Retries for writes) (bit [25]) and/or PCI Read with Write Flush Mode (bit [26]). Refer to Section 4.5 for additional information. Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. If Read data is not available before the PCI Target Retry Delay Clocks counter (LBRD0[31:28]) expires, a PCI Retry is issued.	P, L	P, L, E	1

4.5 PCI r2.1 Features Enable

The IOP 480 can be programmed through the PCI r2.1 Features Enable bit (PCICTL[25]) to perform all PCI Read/Write transactions in compliance to PCI r2.1 (and PCI r2.2). The following IOP 480 behavior occurs when PCICTL[25] = 1.

4.5.1 Direct Slave Delayed Read Mode

PCI Bus single cycle aligned or unaligned 32-bit Direct Slave Read transactions always result in a 1-Lword single cycle transfer on the Local Bus, with corresponding Local Address and Byte Enables (LBE[3:0]#) asserted to reflect the PCI Byte Enables (C/BE[3:0]#), unless the PCI Read Ahead Mode bit is enabled (PCICTL[22] = 1) (refer to Section 4.6). This causes the IOP 480 to Retry all PCI Bus Read requests that follow, until the original PCI Address and Byte Enables (C/BE[3:0]#) are matched.

4.5.2 2^{15} PCI Clock Timeout

If a PCI Master does not complete its originally requested Direct Slave Delayed Read transfer, the IOP 480 flushes the Direct Slave Read FIFO after 2^{15} PCI clocks and will grant an access to a new Direct Slave Read access. The IOP 480 Retries all other Direct Slave Read accesses that occur before the 2^{15} PCI clock timeout.

4.5.3 PCI r2.1 16- and 8- clock rule

The IOP 480 guarantees that if the first Direct Slave Write data cannot be accepted by the IOP 480 and/or the first Direct Slave Read data cannot be returned by the IOP 480 within 16 PCI clocks from the beginning of the Direct Slave cycle (FRAME# asserted), the IOP 480 issues a Retry (STOP# asserted) to the PCI Bus. During successful Direct Slave Read and/or Direct Slave Write accesses, the subsequent data after the first access is accepted for writes or returned for reads in 8 PCI clocks (TRDY# asserted). Otherwise, the IOP 480 issues a PCI disconnect (STOP# asserted) to the PCI Master.

In addition, setting the PCI r2.1 Features Enable bit (PCICTL[25] = 1) allows optional enabling of the following PCI r2.1 functions:

- Retry PCI Writes During Pending Reads (PCICTL[24])
- Flush Pending Reads on PCI Writes (PCICTL[23])

15. Power Management Interface Specification version support

Design Issue:

The IOP 480 Data Book indicates compliance with the PCI Power Management Interface Specification revision 1.1, however the PMC register description is compliant with revision 1.0. The IOP 480 can support either revision. The only differences between these revisions, with respect to IOP 480 support, are the Version bits [2:0] value (programmable by EEPROM or by local bus processor), and the descriptions for bits [8:6, 4] for which the values are read-only and return a value of 0 regardless of revision. The Version bits value (001b or 010b), which has no effect on IOP 480 operation, is used by software to determine PMC register format.

Recommendation:

PMC register descriptions for revisions 1.0 and 1.1 are listed below. If revision 1.1 rather than revision 1.0 is to be supported, program the PMC register (via EEPROM or local bus processor) with the Version value (010b) to overwrite the PMC register default value, by changing the 32-bit value at EEPROM offset E8h or Local Bus offset 340h, from 00015401h to 00025401h.

Register 10-27. (PMC; PCI:42h, LOC:342) Power Management Capabilities
(PCI Power Mgmt. r1.0)

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The value 001 indicates compliance with PCI Power Mgmt. r1.0.	Yes	L, E	001
3	**PCI Clock Required for PME# Signal.** Value of 1 indicates a function relies on PCI clock presence for PME# operation. The IOP480 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	L, E	0
4	**Auxiliary Power Source.** Because the IOP 480 does not support PME# while in a D3cold state, this bit is always set to 0.	Yes	No	0
5	**Device-Specific Initialization (DSI).** Value of 1indicates the IOP 480 requires special initialization following a transition to a D0 uninitialized state before a generic class device driver is able to use it.	Yes	L, E	0
8:6	***Reserved.***	Yes	No	000
9	**D1_Support.** Value of 1 indicates the IOP 480 supports the D1 power state.	Yes	No	0
10	**D2_Support.** Value of 1 indicates the IOP 480 supports the D2 power state.	Yes	No	0
15:11	**PME Support.** Indicates power states in which the IOP 480 may assert PME#. Values: XXXX1 = PME# can be asserted from D0 XXX1X = PME# can be asserted from D1 XX1XX = PME# can be asserted from D2 X1XXX = PME# can be asserted from D3hot XXXXX = PME# cannot be asserted from D3cold	Yes	[14:11]: L, E [15]: No	00000

Register 10-27. (PMC; PCI:42h, LOC:342) Power Management Capabilities
(PCI Power Mgmt. r1.1)

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The default value 001 indicates compliance with PCI Power Mgmt. r1.1. To instead indicate PMC register format compliance with Revision 1.1, this value should be set to 010.	Yes	Local	001
3	**PCI Clock Required for PME# Signal.** Value of 1 indicates a function relies on PCI clock presence for PME# operation. The IOP 480 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Local	0
4	***Reserved.***	Yes	No	0
5	**Device-Specific Initialization (DSI).** Value of 1 indicates the IOP 480 requires special initialization following a transition to a D0 un-initialized state before a generic class device driver is able to use it.	Yes	L, E	0
8:6	**Aux_Current.** Supported by way of the PMDATA register per PCI Power Mgmt. r1.1.	Yes	No	000
9	**D1_Support.** Value of 1 indicates the IOP 480 supports the D1 power state.	Yes	L, E	0
10	**D2_Support.** Value of 1 indicates the IOP 480 supports the D1 power state.	Yes	L, E	0
15:11	**PME Support.** Indicates power states in which the IOP 480 may assert PME#. Values: XXXX1 = PME# can be asserted from D0 XXX1X = PME# can be asserted from D1 XX1XX = PME# can be asserted from D2 X1XXX = PME# can be asserted from D3hot XXXXX = PME# cannot be asserted from D3cold	Yes	[14:11]: L, E [15]: No	00000