

## Features

- Higher speed up to 55 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- Ultra low active power
  - Typical active current: 2 mA at  $f = 1$  MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-Pin shrunk thin small outline package (STSOP) package

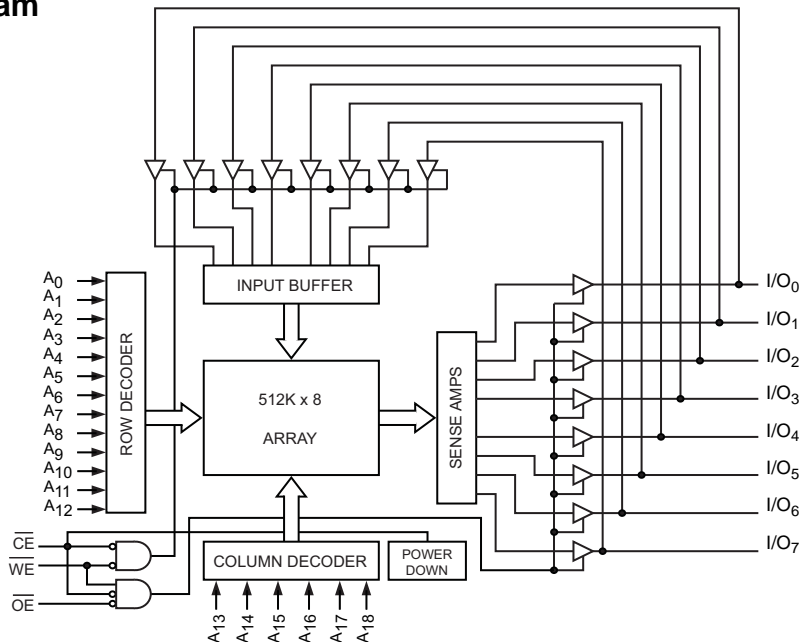
## Functional Description

The CY62148ESL is a high performance CMOS static RAM organized as 512 K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ( $\overline{CE}$  HIGH). The eight input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

## Logic Block Diagram

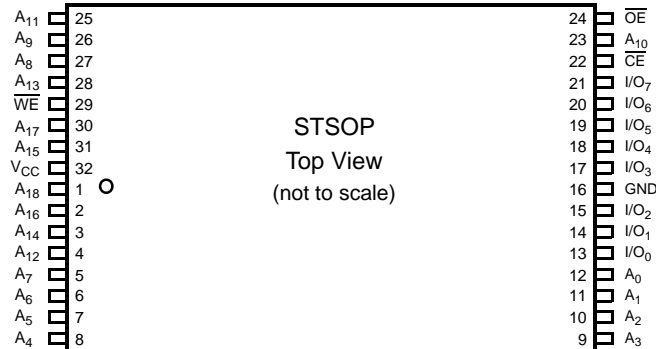


## Contents

<b>Features</b> .....	<b>1</b>	<b>Truth Table</b> .....	<b>9</b>
<b>Functional Description</b> .....	<b>1</b>	<b>Ordering Information</b> .....	<b>10</b>
<b>Pin Configuration</b> .....	<b>3</b>	<b>Ordering Code Definitions</b> .....	<b>10</b>
<b>Product Portfolio</b> .....	<b>3</b>	<b>Package Diagram</b> .....	<b>11</b>
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>12</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>12</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	Units of Measure .....	12
<b>Capacitance</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>13</b>
<b>Thermal Resistance</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>14</b>
<b>Data Retention Characteristics</b> .....	<b>6</b>	Worldwide Sales and Design Support .....	14
<b>Switching Characteristics</b> .....	<b>7</b>	Products .....	14
<b>Switching Waveforms</b> .....	<b>8</b>	PSoC Solutions .....	14

## Pin Configuration

Figure 1. 32-Pin STSOP (Top View)



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V) <sup>[1]</sup>	Speed (ns)	Power Dissipation					
				Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> (μA)	
				f = 1 MHz		f = f <sub>max</sub>			
				Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62148ESL	Industrial/ Automotive-A	2.2 V to 3.6 V and 4.5 V to 5.5 V	55	2	2.5	15	20	1	7

### Notes

- Datasheet specifications are not guaranteed for V<sub>CC</sub> in the range of 3.6 V to 4.5 V.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied.... 55 °C to +125 °C

Supply voltage to ground potential..... -0.5 V to 6.0 V

DC voltage applied to outputs in high Z state<sup>[3, 4]</sup> ..... -0.5 V to 6.0 V

DC input voltage<sup>[3, 4]</sup> ..... -0.5 V to 6.0 V

Output current into outputs (low)..... 20 mA

Static discharge voltage ..... > 2001 V (MIL-STD-883, Method 3015)

Latch-up current..... > 200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[5]</sup>
CY62148ESL	Industrial/ Automotive-A	-40 °C to +85 °C	2.2 V to 3.6 V, and 4.5 V to 5.5 V

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		55 ns (Industrial/Automotive-A)			Unit
				Min	Typ <sup>[6]</sup>	Max	
V <sub>OH</sub>	Output HIGH voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0	-	-	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
V <sub>OL</sub>	Output LOW voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
V <sub>IH</sub>	Input HIGH voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8	-	V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2	-	V <sub>CC</sub> + 0.3	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		2.2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub> <sup>[7]</sup>	Input LOW voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3	-	0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		-0.3	-	0.6	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		-0.5	-	0.6	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , output disabled		-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub>	-	15	20	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA, CMOS levels	-	2	2.5	
I <sub>SB1</sub> <sup>[8]</sup>	Automatic CE power-down current — CMOS inputs	CE ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = f <sub>max</sub> (address and data only), f = 0 (OE and WE), V <sub>CC</sub> = V <sub>CC(max)</sub>		-	1	7	μA
				-			
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE power-down current — CMOS inputs	CE ≥ V <sub>CC</sub> - 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>		-	1	7	μA
				-			

### Notes

- V<sub>IL</sub>(min) = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25 °C.
- Under DC conditions the device meets a V<sub>IL</sub> of 0.8 V (for V<sub>CC</sub> range of 2.7 V to 3.6 V and 4.5 V to 5.5 V) and 0.6 V (for V<sub>CC</sub> range of 2.2 V to 2.7 V). However, in dynamic conditions Input LOW voltage applied to the device must not be higher than 0.6 V and 0.4 V for the above ranges. Refer to AN13470 for details.
- Chip enable (CE) must be HIGH at CMOS level to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

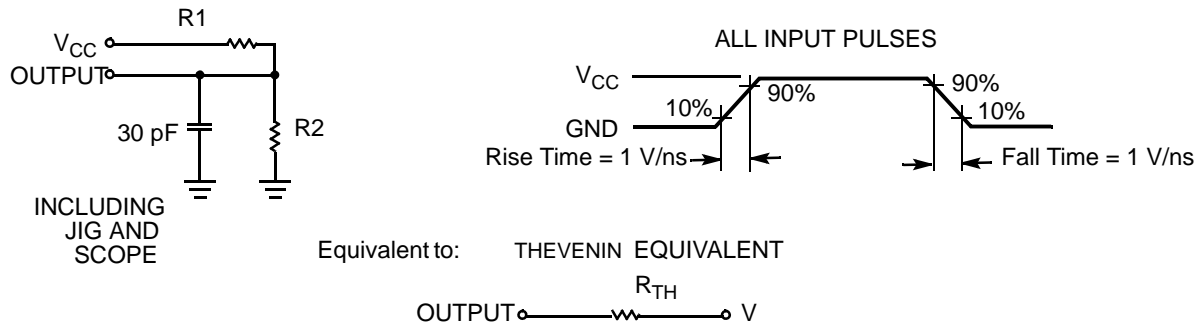
### Capacitance

Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (Typ)	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[9]</sup>	Description	Test Conditions	STSOP	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	49.02	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		14.07	°C/W

Figure 2. AC Test Loads and Waveforms



Parameter	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R <sub>TH</sub>	8000	645	639	Ω
V <sub>TH</sub>	1.20	1.75	1.77	V

**Notes**

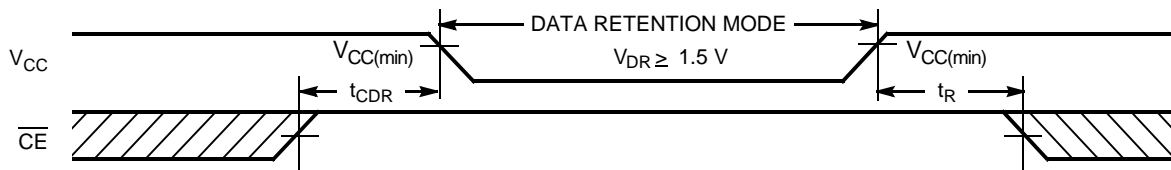
9. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.5	–	–	V
$I_{CCDR}$ <sup>[11]</sup>	Data retention current	$\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $V_{CC} = 1.5$ V	–	1	7	$\mu$ A
$t_{CDR}$	Chip deselect to data retention time		0	–	–	ns
$t_R$ <sup>[12]</sup>	Operation recovery time		55	–	–	ns

**Figure 3. Data Retention Waveform**



### Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ)}$ ,  $T_A = 25$  °C.
11. Chip enable ( $\overline{CE}$ ) must be HIGH at CMOS level to meet the  $I_{SB1}$  /  $I_{SB2}$  /  $I_{CCDR}$  spec. Other inputs can be left floating.
12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100$   $\mu$ s or stable at  $V_{CC(min)} \geq 100$   $\mu$ s.

## Switching Characteristics

Over the operating range

Parameter <sup>[13]</sup>	Description	55 ns (Industrial/Automotive-A)		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid	–	55	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[14]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[14, 15]</sup>	–	20	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[14]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[14, 15]</sup>	–	20	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-up	–	55	ns
<b>Write Cycle <sup>[16]</sup></b>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	40	–	ns
$t_{AW}$	Address setup to write end	40	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	40	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[14, 15]</sup>	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[14]</sup>	10	–	ns

### Notes

13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in [AC Test Loads and Waveforms on page 5](#).

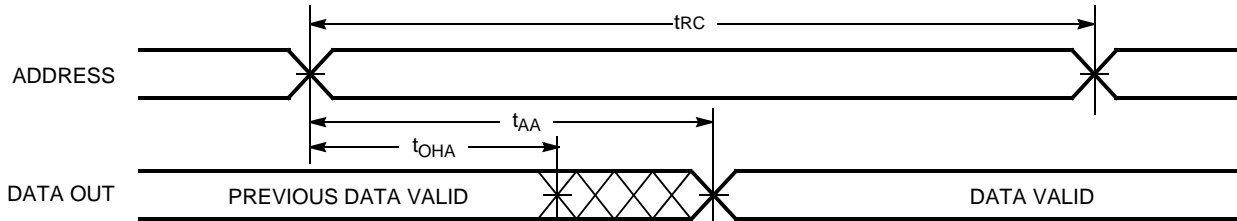
14. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

15.  $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  transitions are measured when the output enter a high impedance state.

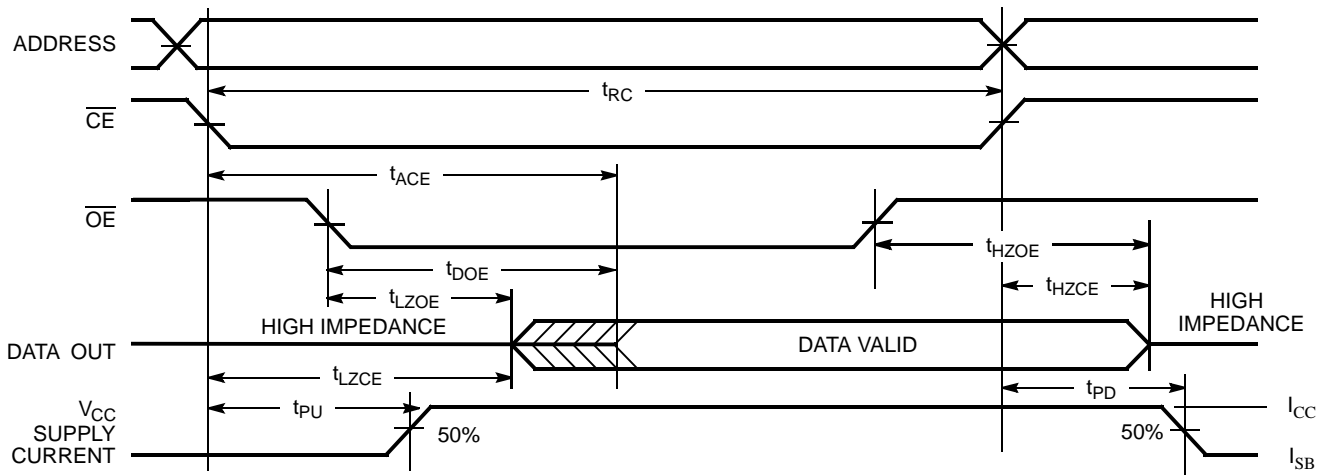
16. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

### Switching Waveforms

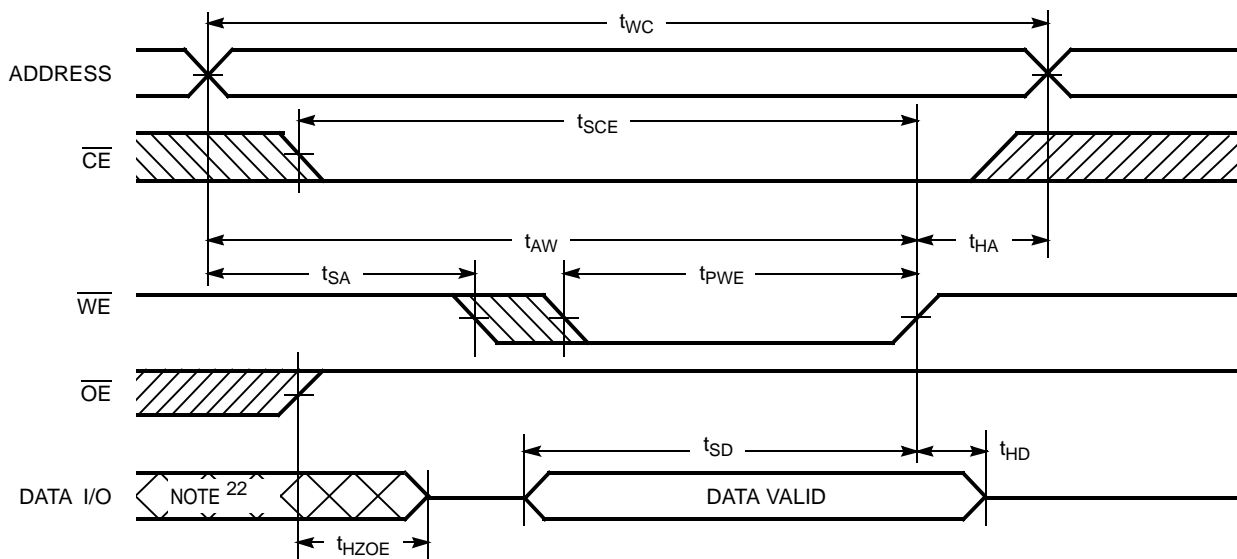
**Figure 4. Read Cycle No. 1 (Address Transition Controlled)** [17, 18]



**Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [18, 19]



**Figure 6. Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)** [20, 21]



**Notes**

- 17. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .
- 18.  $\overline{WE}$  is HIGH for read cycles.
- 19. Address valid before or similar to  $\overline{CE}$  transition LOW.
- 20. Data I/O is high impedance if  $\overline{OE}$  =  $V_{IH}$ .
- 21. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
- 22. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled) [23, 24]

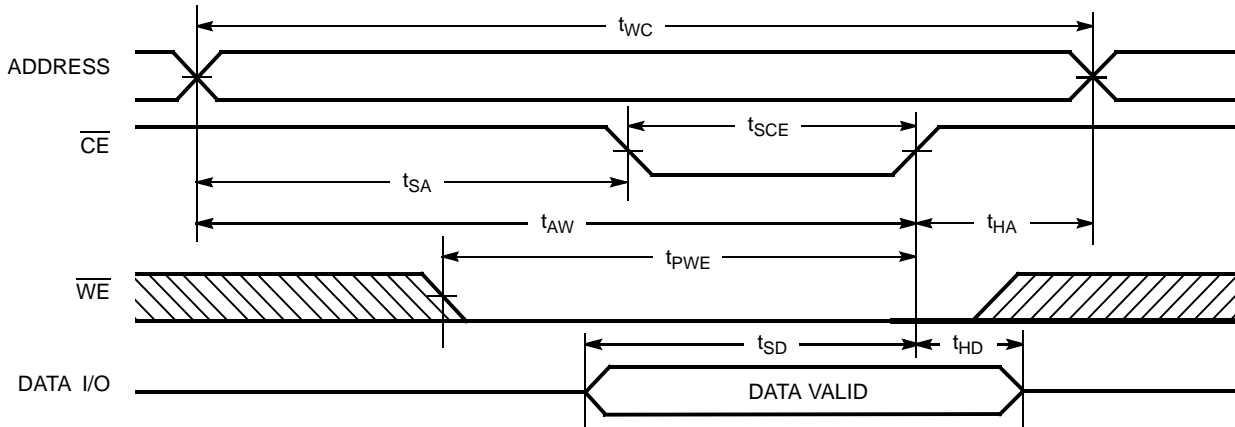
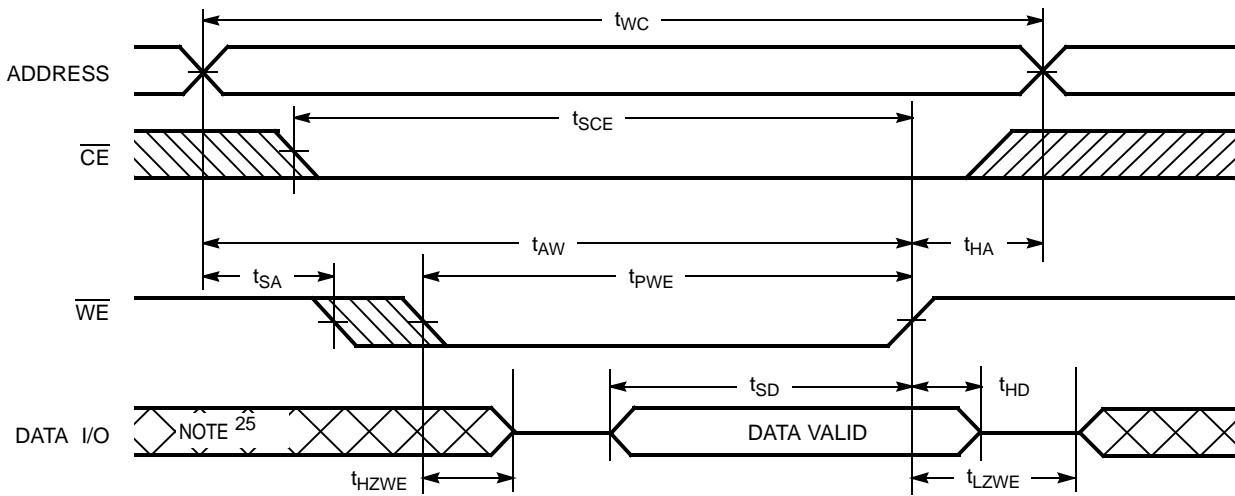


Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [24]



Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Mode	Power
H <sup>[26]</sup>	X	X	High Z	Deselect/power-down	Standby ( $I_{\text{SB}}$ )
L	H	L	Data out	Read	Active ( $I_{\text{CC}}$ )
L	H	H	High Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	L	X	Data in	Write	Active ( $I_{\text{CC}}$ )

Notes

- 23. Data I/O is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
- 24. If CE goes HIGH simultaneously with WE HIGH, the output remains in high impedance state.
- 25. During this period, the I/Os are in output state. Do not apply input signals.
- 26. Chip enable (CE) must be HIGH at CMOS level to meet the  $I_{\text{SB1}} / I_{\text{SB2}} / I_{\text{CCDR}}$  spec. Other inputs can be left floating.

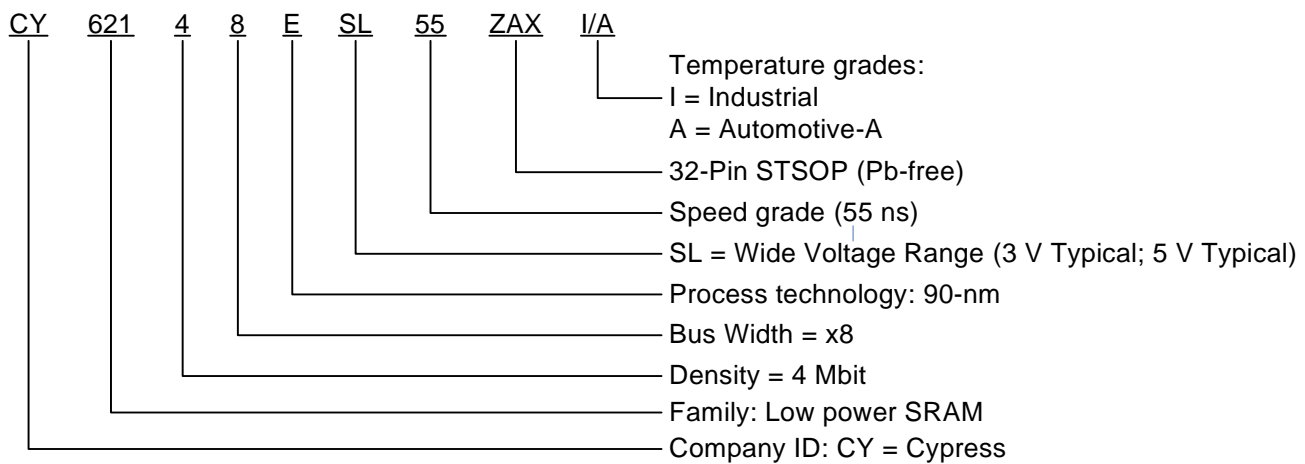
## Ordering Information

Table 1 lists the CY62148ESL MoBL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>.

**Table 1. Key features and Ordering Information**

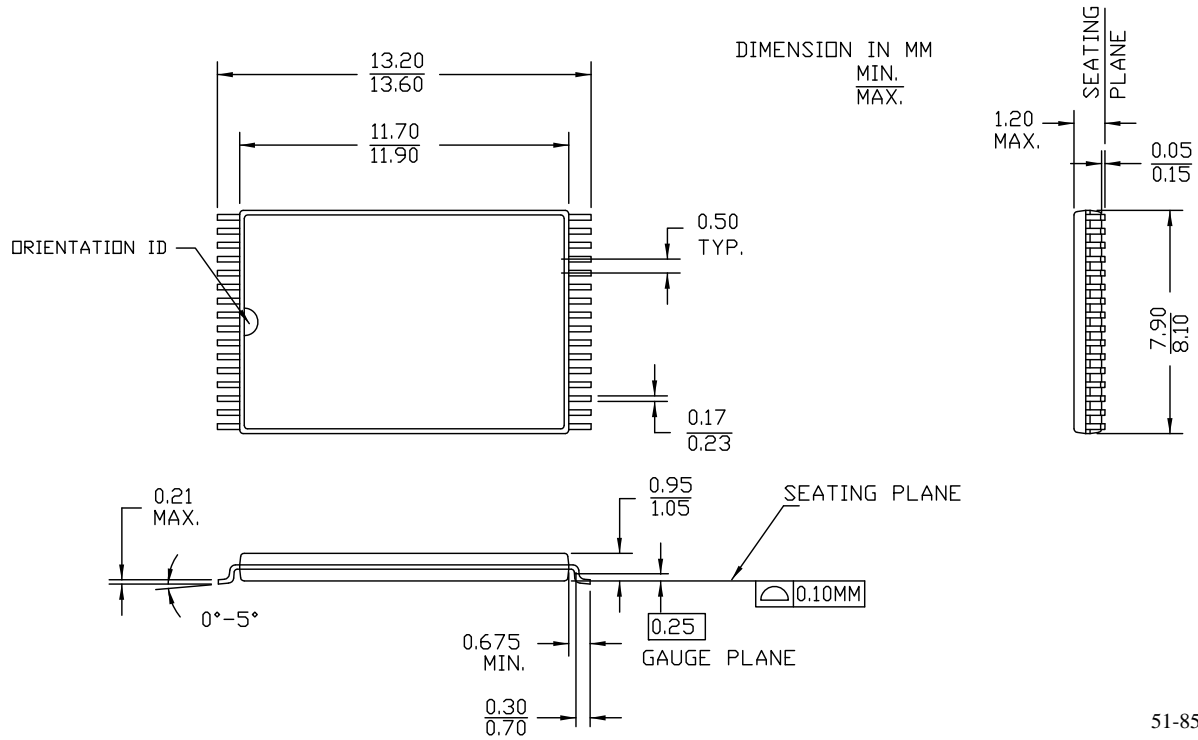
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62148ESL-55ZAXI	51-85094	32-Pin STSOP (Pb-free)	Industrial
	CY62148ESL-55ZAXA	51-85094	32-Pin STSOP (Pb-free)	Automotive-A

## Ordering Code Definitions



Package Diagram

Figure 9. 32-Pin Shrinked Thin Small Outline Package (8 mm x 13.4 mm), 51-85094



## Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball grid array
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62148ESL MoBL <sup>®</sup> 4-Mbit (512 K × 8) Static RAM				
Document Number: 001-50045				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2612938	VKN/PYRS	01/21/09	New datasheet
*A	2800124	VKN	11/06/2009	Included Automotive-A information
*B	2947039	VKN	06/10/2010	Added footnote related to chip enable in <a href="#">Truth Table</a> Added footnote for the I <sub>SB2</sub> parameter in <a href="#">Electrical Characteristics</a> Updated <a href="#">Package Diagram</a> Updated links in <a href="#">Sales, Solutions, and Legal Information</a>
*C	3006318	AJU	08/23/10	Template update. Updated table of contents. Added acronyms, units of measure and ordering code definitions. Added reference to note 8 to parameter I <sub>SB1</sub> on page 4 under Electrical characteristics table. Added reference to note 11 to parameter I <sub>CCDR</sub> on page 6 under data retention characteristics table.
*D	3296704	RAME	06/29/11	Removed reference to AN1064 SRAM system guidelines. Updated <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> to latest revision.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

<a href="#">Automotive</a>	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
<a href="#">Memory</a>	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
<a href="#">Optical &amp; Image Sensing</a>	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
<a href="#">PSoC</a>	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

---

© Cypress Semiconductor Corporation, 2009-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.