Consumer Microcircuits Limited
COMMUNICATION SEMICONDUCTORS

CMX969
RD-LAP/MDC4800 Motient/ARDIS

D/969/5 April 2001 Provisional Information

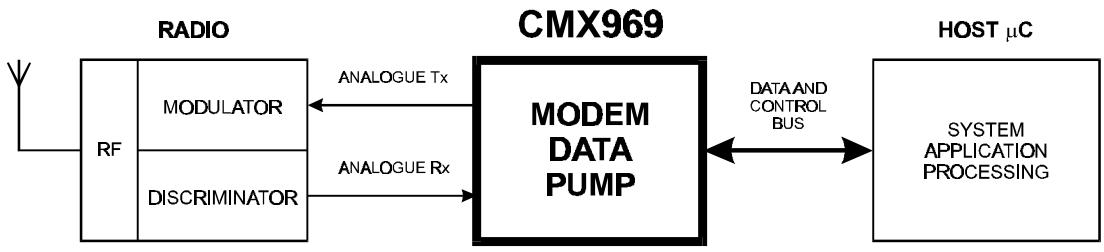
Features

- **Autonomous Frame Sync Detection for SFR operation**
- **Full Packet Data Framing**
- **Low Power, 3.0 to 5.5V operation**
- **Powersave Option**

Applications

- **DataTAC*, Motient/ARDIS*, Dual Mode RD-LAP* and MDC 4800**
- **Two-Way Paging Equipment**
- **Mobile Data Systems**
- **Wireless Telemetry**
- **DataTAC* Terminals**

*Radio Data-Link Access Procedure (RD-LAP) is a data communications air interface protocol developed by Motorola Inc.
*Motient is a registered service mark of the Motient Company operating the Motient Network. (Formerly known as American Mobile operating the ARDIS Network).
*DataTAC is a registered trademark of Motorola Inc.



1.1 Brief Description

The CMX969 is a CMOS integrated circuit that contains all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance DataTAC dual mode (RD-LAP 19200 bps and MDC 4800 bps) FSK Wireless Packet Data Modem suitable for use with the Motient/ARDIS network. It interfaces with the modem host processor and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over the wireless link.

The CMX969 assembles application data received from the host processor, adds forward error correction (FEC) and error detection (CRC) information and interleaves the result for burst-error protection. After adding symbol and frame synchronisation codewords and channel status symbols, it converts the packet into a filtered analogue baseband signal for modulating the radio transmitter.

In receive mode, the CMX969 performs the reverse function using the analogue baseband signals from the receiver frequency discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host processor. Any residual uncorrected errors in the data will be flagged. A readout of the received signal quality is also provided.

An optional Autonomous Frame Sync Detection function is provided for use in Motient/ARDIS systems employing Single Frequency Re-use operation.

The CMX969 uses signal filtering, data block formats and FEC/CRC algorithms compatible with the MDC and RD-LAP over-air standards. The device is programmable to operate from a wide choice of Xtal frequencies and is available in 24 pin DIP, SSOP and TSSOP packages.

CONTENTS

1.2 Block Diagram

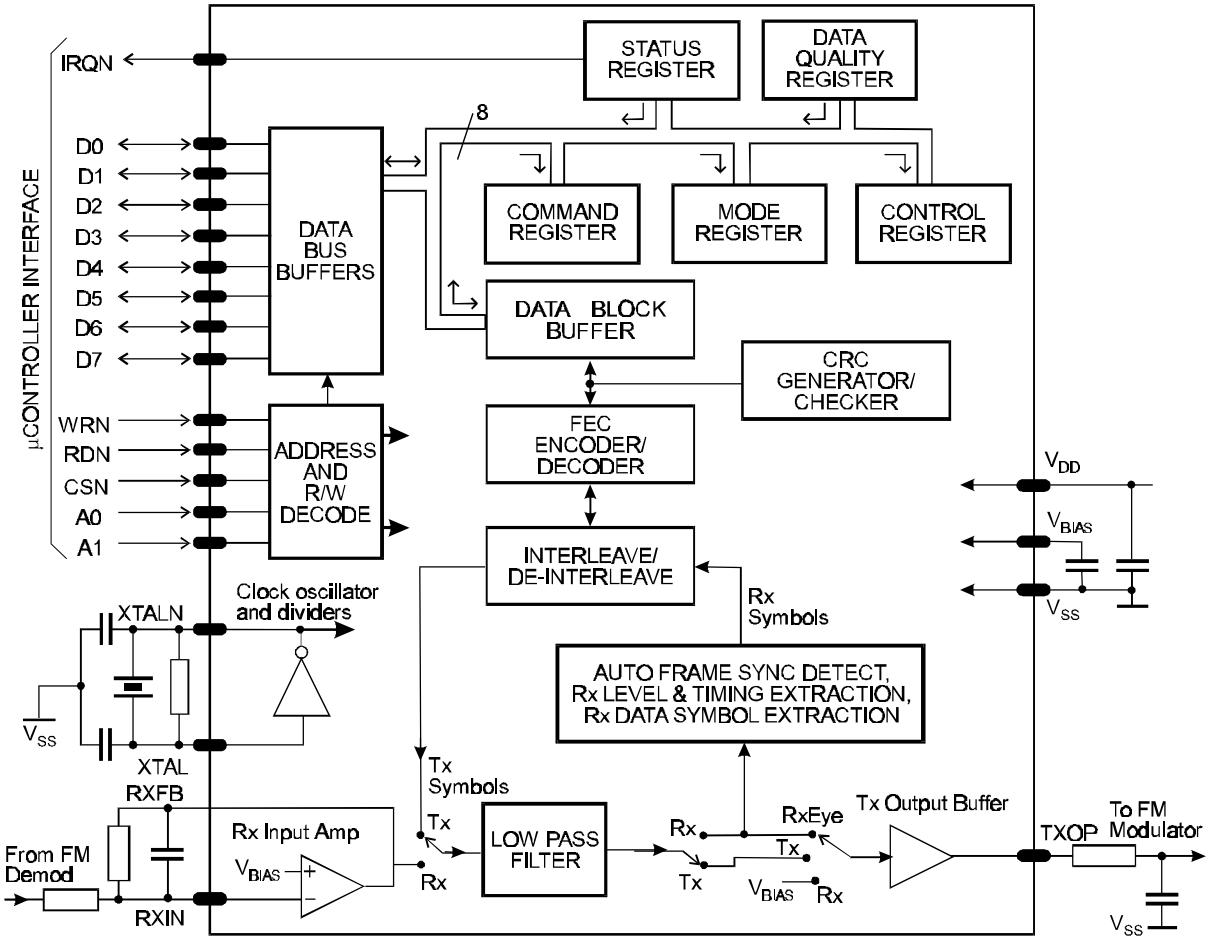


Figure 1 Block Diagram

1.3 Signal List

Package P4/E2/D5	Signal		Description
Pin No.	**Name**	**Type**	
1	IRQN	O/P	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. This output has a low impedance pull down to V_{SS} when active and is high impedance when inactive. An external pull up resistor of about 100k ohm to V_{DD} is required.
2	D7	BI	)
3	D6	BI	)
4	D5	BI	)
5	D4	BI	) 8-bit bidirectional 3-state µC interface data
6	D3	BI	) lines.
7	D2	BI	)
8	D1	BI	)
9	D0	BI	)
10	RDN	I/P	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	WRN	I/P	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	Power	The negative supply rail (ground).
13	CSN	I/P	Chip Select. An active low logic level input to the modem, used to enable a data read or write operation.
14	A0	I/P	) Two logic level modem register select
15	A1	I/P	) inputs.
16	XTALN	O/P	The output of the on-chip oscillator.
17	XTAL	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
18,19		NC	No connection should be made to these pins (reserved for possible future use)
20	TXOP	O/P	The Tx signal output from the modem.
21	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. This pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	I/P	The input to the Rx input amplifier.

Package P4/E2/D5	Signal		Description
Pin No.	**Name**	**Type**	
23	RXFB	O/P	The output of the Rx input amplifier .
24	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes: I/P = Input O/P = Output BI = Bidirectional NC = No connection
Internal protection diodes are connected from each signal pin to V_{DD} and V_{SS}.

1.4 External Components

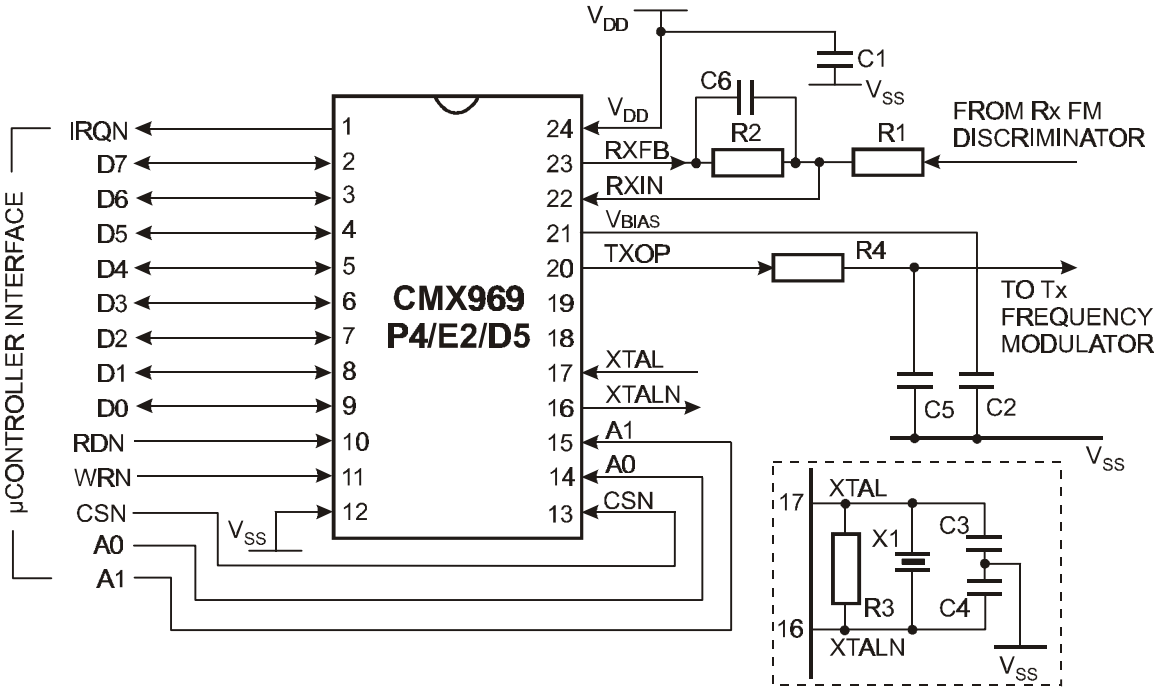


Figure 2 Recommended External Components

R1	See Section 1.5.1	C1	0.1 µF ± 20%	C4	± 20%, see Note 1
R2	100k ohm ± 5%	C2	0.1 µF ± 20%	C5	100pF ± 5%
R3	1M ohm ± 20%	C3	± 20%, see Note 1	C6	100pF ± 5%
R4	100k ohm ± 5%				
X1	4.9152, 7.3728 or 9.8304 MHz ±100ppm. See Section 1.5.5.2				

Note 1: The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitances) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable.

1.5 General Description

1.5.1 Description of Blocks

Refer to Figure 1.

Data Bus Buffers
Eight bidirectional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

Address and R/W Decode
This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs (WRN and RDN), the Chip Select input (CSN) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

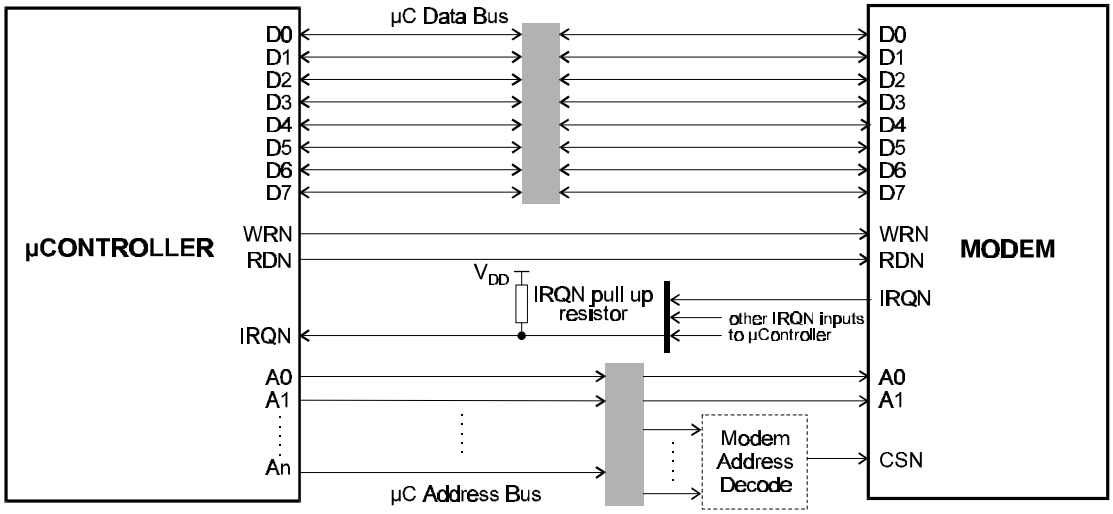


Figure 3 Typical Modem µC Connections

Status and Data Quality Registers
Two 8-bit registers which the µC can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers
The values written by the µC to these 8-bit registers control the operation of the modem.

Data Buffer
A 12-byte buffer used to hold receive or transmit data to or from the µC.

CRC Generator/Checker
A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which are included in transmitted data blocks so that the receive modem can detect transmission errors.

FEC Encoder/Decoder
In transmit mode, this circuit adds Forward Error Correction information to the transmitted data. In RD-LAP mode it also converts the binary data to 4-level symbols. In receive mode, this block translates received symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

Interleave/De-interleave Buffer
This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

Auto Frame Sync Detect, Rx Level & Timing Extraction, Rx Data Symbol Extraction
This block, which is only active in receive mode, is used to look for the Frame Synchronisation pattern which is transmitted to mark the start of every frame and to extract the received symbols from the received signal using extracted signal level and timing information.

Rx Input Amp
This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The dc level of the received signal should be adjusted so that the signal at the modem's RXFB pin is centred around V_{BIAS} (½ V_{DD}). See section 1.7.1.3 for details of the optimum levels.

Low Pass Filter
This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter having a frequency response automatically switched to suit RD-LAP or MDC operation.

In transmit mode, the data symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

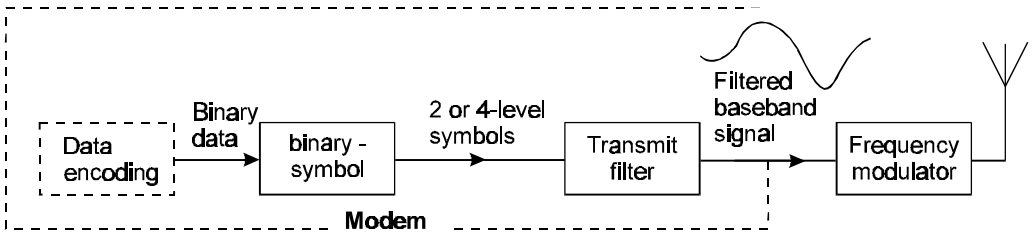


Figure 4 Generation of Filtered Tx Baseband Signal

In receive mode, the filter is used to reject HF noise and to equalise the received signal to a form suitable for extracting the received data.

Tx Output Buffer
This is a unity gain amplifier used in transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS} unless the RXEYE bit of the Control Register is '1', when it is connected to the received signal. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 8 symbol times in RD-LAP mode, 2 symbol times in MDC mode while the low pass filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOP pin and the input to the radio's frequency modulator forms an important part of the transmit out of band spurious signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. C5 should be positioned to give maximum attenuation of high frequency noise into the modulator.

Clock Oscillator and Dividers
These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL input pin, the XTALN pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

1.5.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message formats handled by the modem are given in Section 1.5.4 and Figures 5a and 5b.

To reduce the processing load on the associated µC, the CMX969 modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronising onto the Frame Preamble. In normal operation the modem will only require servicing by the µC once per received or transmitted block.

Thus, to transmit a block, the controlling µC has only to load the - unformatted - 'raw' binary data into the modem's Data Block Buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 2 or 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary - using the FEC coding to correct as many errors as possible - and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also transmit and receive un-formatted data using the T4S, T24S, R4S, T8B, T40B and R8B tasks described in section 1.5.5.4 These are normally used for the transmission of Symbol and Frame Synchronisation sequences. They may also be used for the transmission and reception of special test patterns.

1.5.3 Binary to RD-LAP 4-Level Symbol Translation

Although the over-air signal, and hence the signals at the modem TXOP and RXIN pins, consists of 4-level symbols in RD-LAP mode, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

Direct: the simplest form, which converts between 2 binary bits and a single symbol, such as the 'S' Channel Status symbol.

symbol	ms bit	ls bit
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This is expanded so that an 8-bit byte translates to four symbols for the T4S, T24S and R4S tasks described in Section 1.5.5.2.

	msb							lsb
Bits:	7	6	5	4	3	2	1	0
Symbols:	a		b		c		d	
	sent first						sent last	

With FEC: This is more complicated, but essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, TSID, RHB, RILB and RSID described in Section 1.5.5.4.

1.5.4 Frame Structure

In both RD-LAP and MDC modes the CMX969 performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figures 5a and 5b.

1.5.4.1 MDC Mode

The CMX969 Frame Structure in MDC mode is illustrated in Figure 5a, and consists of a Frame Synchronisation pattern followed by one or more 'Header' blocks, one or more 'Intermediate' blocks and a 'Last' block. Channel Status bits are included at regular intervals. The first Frame of any transmission is preceded by a Bit Synchronisation pattern.

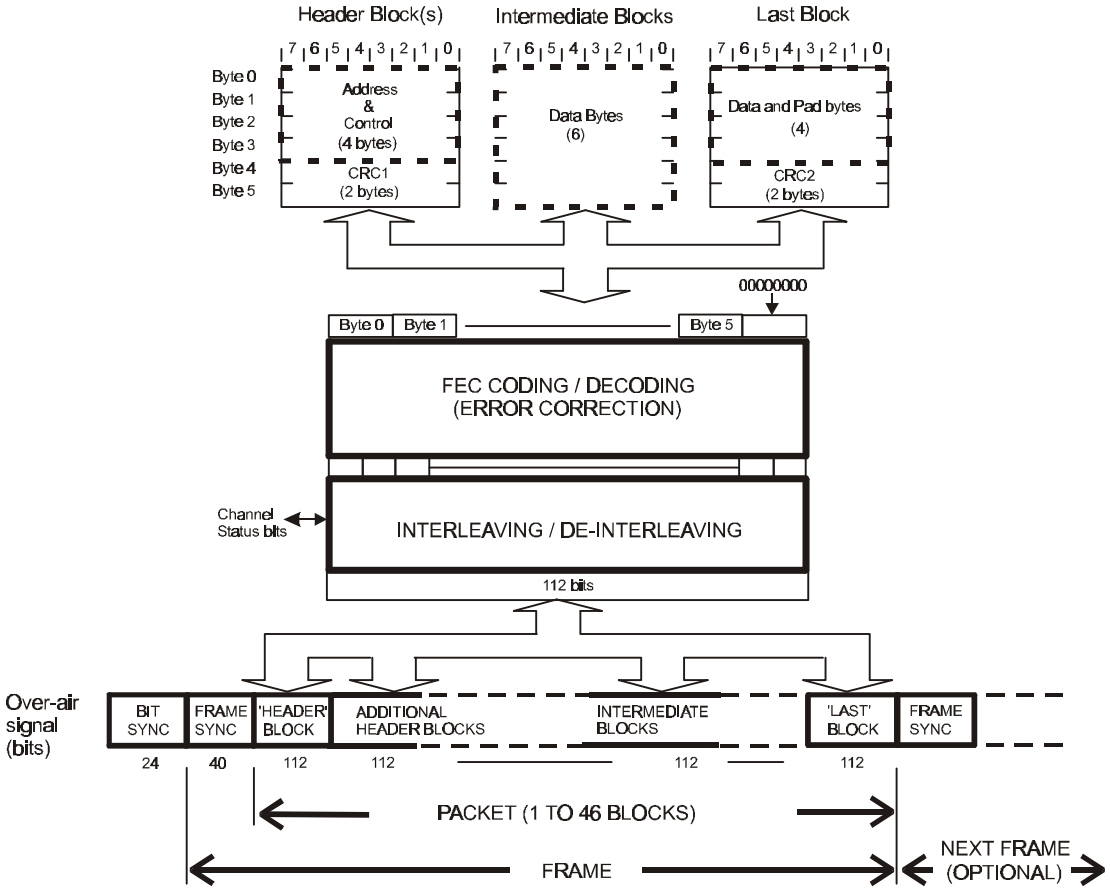


Figure 5a MDC Over Air Signal Format

The MDC bit synchronisation pattern consists of alternating 1's and 0's. The normal MDC Frame Synchronisation (SYNC1) pattern is 07092A446F Hex (msb transmitted first). SYNC2 is the 1's complement of SYNC1.

1.5.4.2 RD-LAP Mode

The CMX969 Frame Structure in RD-LAP mode is illustrated in Figure 5b, and consists of a Frame Preamble (comprising a 24-symbol Frame Synchronisation pattern and Station ID block) followed by one or more 'Header' blocks, one or more 'Intermediate' blocks and a 'Last' block. Channel Status (S) symbols are included at regular intervals. The first Frame of any transmission is preceded by a Symbol Synchronisation pattern.

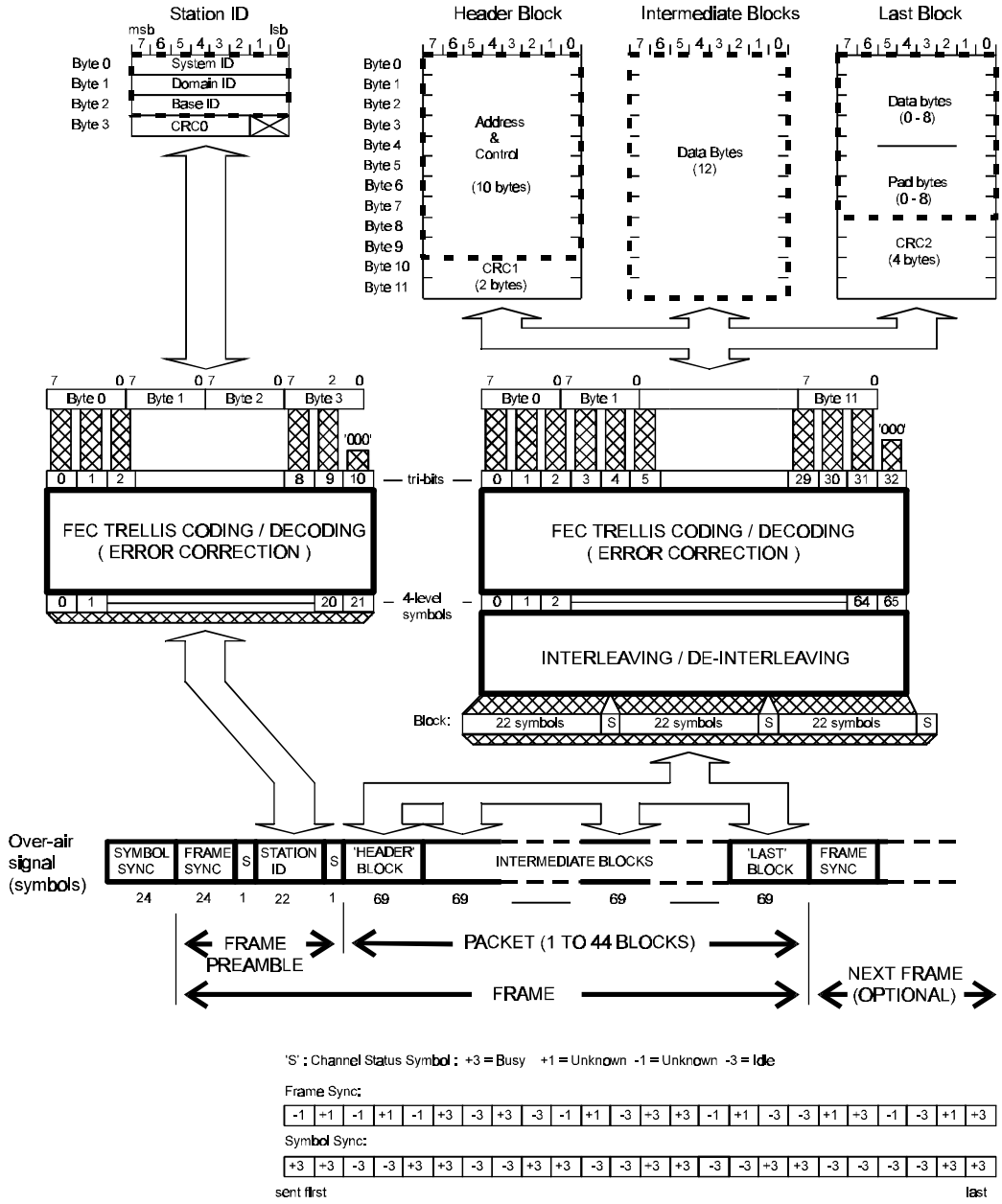


Figure 5b RD-LAP Over Air Signal Format

1.5.5 The Programmer's View

The modem appears to the programmer as 4 write only 8-bit registers shadowed by 3 read only registers, individual registers being selected by the A0 and A1 chip inputs: Note that there is a minimum allowable time between accesses of the modem's registers, see Section 1.7.1 for details.

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	Reserved for other uses.

1.5.5.1 Data Block Buffer

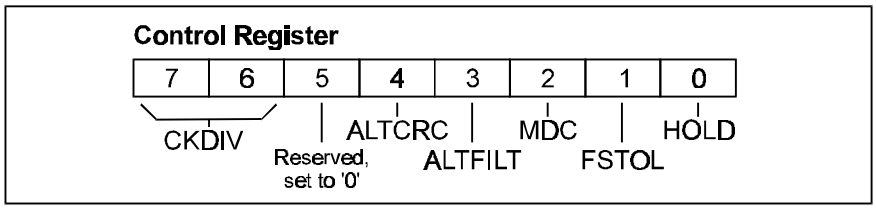
This is a 12-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC. It appears to the µC as a single 8-bit register; the modem ensuring that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode. Note that in receive mode the modem will function correctly even if the µC does not read the received data from the Data Buffer.

1.5.5.2 Control Register

This 8-bit write-only register controls the modem's operating mode (RD-LAP or MDC), symbol rate and the response times of the receive clock extraction and signal level measurement circuits.



Control Register B7, B6: CKDIV - Clock Division Ratio
These bits control a frequency divider driven from the clock signal present at the XTALN pin, and hence determine the nominal symbol and bit rates. The following table shows the settings of B7 and B6 needed for 19200bps RD-LAP and 4800bps MDC4800 operation.

B7	B6	Xtal Frequency	Division ratio:	
			Xtal frequency / RD-LAP Symbol Rate	Xtal frequency / MDC4800 Symbol Rate
0	0	4.9152 MHz	512	1024
0	1	7.3728 MHz	768	1536
1	0	9.8304 MHz	1024	2048
1	1	See note	1536	3072

Note: The setting B7 = 1 and B6 = 1 cannot be used with 19200bps RD-LAP / 4800bps MDC4800 as this would require a Xtal frequency above the oscillator operating range.

The CMX969 may also be used with a 9600bps RD-LAP system if the Xtal frequency is 4.9152 or 7.3728MHz and Control register bits 7-6 set to ‘1 0’ or ‘1 1’

Control Register B5: Reserved for future use.
This bit should always be set to ‘0’.

Control Register B4: ALTCRC - Alternative CRC
This bit should always be set to ‘0’ for standard RD-LAP and MDC systems. Setting it to ‘1’ in RD-LAP mode selects an alternative CRC generation/checking algorithm.

Control Register B3: ALTFILT - Alternative Filtering
This bit should always be set to ‘0’ for standard RD-LAP and MDC systems. Setting it to ‘1’ in RD-LAP mode selects slightly different transmit and receive lowpass filter characteristics more suitable for some non-standard systems.

Control Register B2: MDC - MDC Mode
If this bit is ‘0’ the CMX969 operates in RD-LAP mode, setting this bit to ‘1’ selects MDC mode. Changing between RD-LAP and MDC modes will cancel any current task.

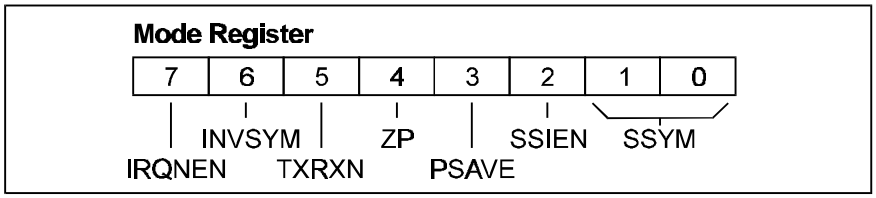
Control Register B1: FSTOL - Frame Sync Detect Tolerance
In RD-LAP mode this bit affects the number of errors tolerated by the Frame Sync detector when running SFS or SFP tasks or AFSD. Approximately 3 bit errors are allowed when FSTOL = 0, 7 when FSTOL = 1.

In MDC mode this bit has no effect and the Frame Sync detector will accept up to 5 incorrect bits in a received Frame Sync pattern when running the SFS task or AFSD.

Control Register B0: HOLD - Freeze Rx Level and Timing Corrections
Setting this bit to 1 disables the receive level and symbol timing error correction circuits.

1.5.5.3 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



Mode Register B7: IRQNEN - IRQN Output Enable
When this bit is set to '1', the IRQN chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

Mode Register B6: INVSYM - Invert Symbols
This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOP	Signal at RXFB
0	'+3 or +1'	Above V_{BIAS}	Below V_{BIAS}
	'-3 or -1'	Below V_{BIAS}	Above V_{BIAS}
1	'+3 or +1'	Below V_{BIAS}	Above V_{BIAS}
	'-3 or -1'	Above V_{BIAS}	Below V_{BIAS}

Mode Register B5: TXRXN - Tx/Rx Mode
Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. Note that changing between receive and transmit modes will cancel any current task.

Mode Register B4: ZP - Zero Power
Setting this bit to '1' removes power from all of the CMX969's circuitry, including the Xtal oscillator, the Vbias supply and the Tx o/p buffer. The µC interface will continue to operate except for the Command Register which will not recognise or execute commands when ZP is '1' as it relies on a clock source for correct operation.

To obtain the lowest power consumption in Zero Power mode, the Mode Register TXRXN bit (B5) should be set to 0 when the ZP bit (B4) is set to 1.

Mode Register B3: PSAVE - Powersave
When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx Symbol and Clock extraction circuits and the Tx o/p buffer will be disabled, and the TxOp pin will be connected to Vbias through a high value resistance. The Xtal Clock oscillator, Rx i/p amplifier and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' when the ZP bit is '0' restores power to all of the chip circuitry. Note that the internal filters - and hence the TxOp pin in transmit mode - will take about 20 symbol-times to settle after the PSAVE bit is taken from '1' to '0'.

Mode Register B2: SSIEN - 'S' Symbol IRQ Enable
In receive mode, setting this bit to '1' causes the IRQ bit of the status register to be set to '1' whenever a new channel status 'S' symbol has been received. (The SRDY bit of the Status Register will also be set to '1' at the same time, and the SVAL bits updated to reflect the received 'S' symbol.)

In transmit mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a 'S' symbol or channel status bit has been transmitted. (The SRDY bit of the Status Register will also be set to '1' at the same time.)

In MDC mode no interrupt is generated for the unused '94th bit' in each block.

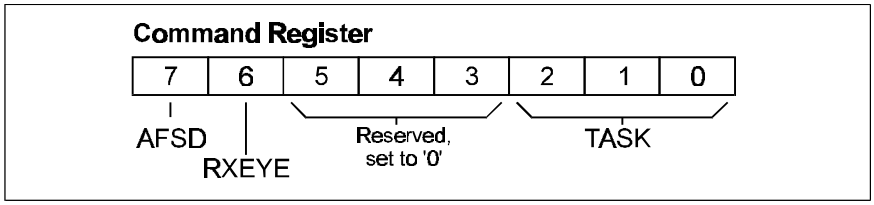
Mode Register B1, 0: SSYM - 'S' Symbol To Be Transmitted
In transmit mode these two bits define the next 'S' symbol or channel status bit to be transmitted. These bits have no effect in receive mode.

B1	B0	RD-LAP	MDC
1	1	'+3'	'+1'
1	0	'+1'	'+1'
0	0	'-1'	'-1'
0	1	'-3'	'-1'

1.5.5.4 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the AFSD and TASK bits, and controls the RxEye function.

Note that the Command Register uses internal clocks derived from the XTAL input to decode and carry out any task written to it, so it is advisable to postpone writing to the Command Register until about 20 msec after power is applied to the CMX969 or the Mode Register ZP bit is changed from ‘1’ to ‘0’, to allow time for the Xtal oscillator to start up.



When it has no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, but will otherwise ignore the received data.

Command Register B7: AFSD - Autonomous Frame Sync Detect
Setting this bit to ‘1’ in receive mode enables the Autonomous Frame Sync Detect function. It has no effect in transmit mode.

Command Register B6: RXEYE - Show Rx Eye
This bit should normally be set to '0'.

Setting it to '1' when the modem is in receive mode connects the input of the Tx o/p buffer to the Rx filter output (see Figure 1). This allows the filtered and equalised receive signal monitored with an oscilloscope (at the TXOP pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator. In transmit mode this bit has no effect.

In RD-LAP mode the resulting eye diagram (for reasonably random data) should ideally be as shown in Figure 6a, with 4 'crisp' and equally spaced crossing points.

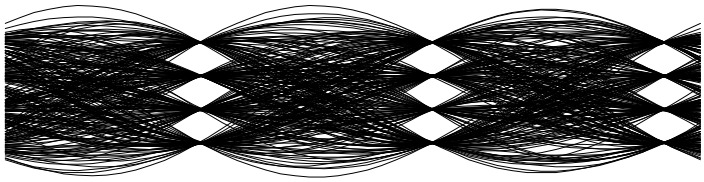


Figure 6a Ideal 'RXEYE' Signal: RD-LAP Mode

In MDC mode the eye diagram should be as Figure 6b

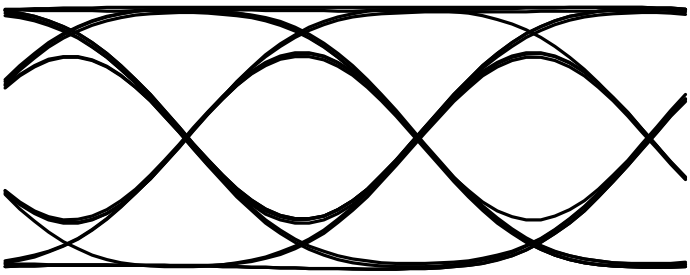


Figure 6b Ideal 'RXEYE' Signal: MDC Mode

Command Register B5-3
These bits are reserved for future use and should always be set to ‘0’.

Command Register B2, B1, B0: TASK
Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in RD-LAP and MDC receive and transmit modes.

CMX969 Modem Tasks, Transmit Mode:

B2	B1	B0	RD-LAP		MDC	
0	0	0	NULL		NULL	
0	0	1	T24S	Transmit 24 symbols	T40B	Transmit 40 bits
0	1	0	THB	Transmit Header Block	THB	Transmit Header Block
0	1	1	TIB	Transmit Intermediate Block	TIB	Transmit Intermediate Block
1	0	0	TLB	Transmit Last Block	TLB	Transmit Last Block
1	0	1	T4S	Transmit 4 symbols	T8B	Transmit 8 bits
1	1	0	TSID	Transmit Station ID	-	Unused
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip IRQN output to go low if the IRQNEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write a task and the associated data to the modem while the modem is still transmitting the data from the previous task.

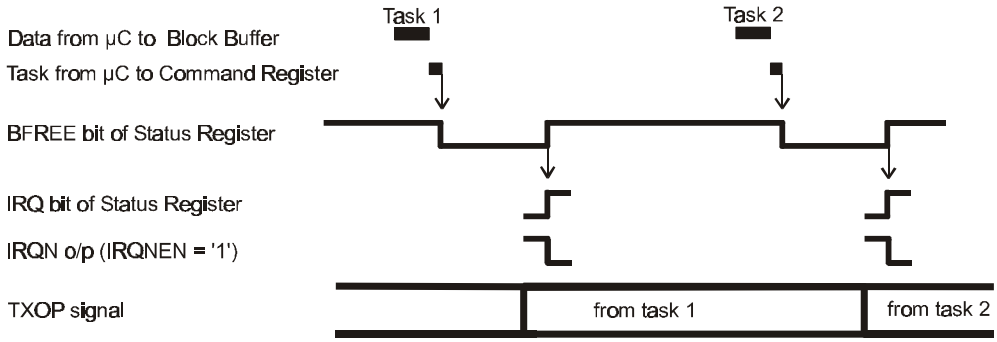


Figure 7 Transmit Task Overlapping

T24S: Transmit 24 Symbols (RD-LAP only)
This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC, FEC, interleaving or adding any 'S' symbols.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The following tables show what data has to be written to the Data Block Buffer to transmit the CMX969 Symbol and Frame Sync sequences:

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
-3	-3	+3	+3	Byte 5 :	01011111	5F

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

NULL:
This 'task' has no effect in transmit mode.

T40B: Transmit 40 Bits (MDC only)
This task is similar to the RD-LAP mode T24S task, but transmits 40 bits taken from the first 5 bytes in the Data Block Buffer. Data block buffer byte 0 is transmitted first, byte 4 last, within each byte the msb is transmitted first, lsb last.

THB: Transmit Header Block (RD-LAP and MDC)
In RD-LAP mode this task takes 10 bytes of data from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block , inserting 'S' symbols at 22-symbol intervals.

In MDC mode this task takes 4 bytes of data from the Data Block Buffer, calculates and appends the 2-byte checksum, adds FEC bits, interleaves the result, inserts channel status bits and transmits the result as a formatted 'Header' Block..

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

TIB: Transmit Intermediate Block (RD-LAP and MDC)
In RD-LAP mode this task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block , inserting 'S' symbols at 22-symbol intervals.

In MDC mode this task takes 6 bytes of data from the Data Block Buffer, updates the 2-byte CRC checksum for inclusion in the 'Last' block, adds FEC bits, interleaves the result, inserts channel status bits and transmits the result as a formatted 'Intermediate' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

TLB: Transmit Last Block (RD-LAP and MDC)

In RD-LAP mode this task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block , inserting 'S' symbols at 22-symbol intervals.

In MDC mode this task takes 4 bytes of data from the Data Block Buffer, updates and appends the 2-byte checksum, adds FEC bits, interleaves the result, inserts channel status bits and transmits the result as a formatted 'Last' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

T4S: Transmit 4 Symbols (RD-LAP only)
This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols most significant bit first.

T8B: Transmit 8 Bits (MDC only)
This task is similar to T40B but takes only one byte from the Data Block Buffer, transmitting it as 8 bits.

TSID: Transmit Station ID (RD-LAP only)
This task takes 3 ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

RESET: Stop any current action
This 'task' takes effect immediately, and terminates any current task the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used (after a delay to allow the Xtal oscillator to start up) when V_{DD} is applied or the ZP bit of the Mode Register changed from ‘1’ to ‘0’ to set the modem into a known state.

Note that due to delays in the transmit low pass filter, it will take several symbol times for any change to appear at the TXOP pin.

CMX969 Modem Tasks, Receive Mode:

B2	B1	B0	RD-LAP		MDC	
0	0	0	NULL		NULL	
0	0	1	SFP	Search for Frame Preamble	-	Unused
0	1	0	RHB	Read Header Block	RHB	Read Header Block
0	1	1	RILB	Read Intermediate or Last Block	RILB	Read Intermediate or Last Block
1	0	0	SFS	Search for Frame Sync	SFS	Search for Frame Sync
1	0	1	R4S	Read 4 symbols	R8B	Read 8 bits
1	1	0	RSID	Read Station ID	-	Unused
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed, and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the IRQN output to go low if the IRQNEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

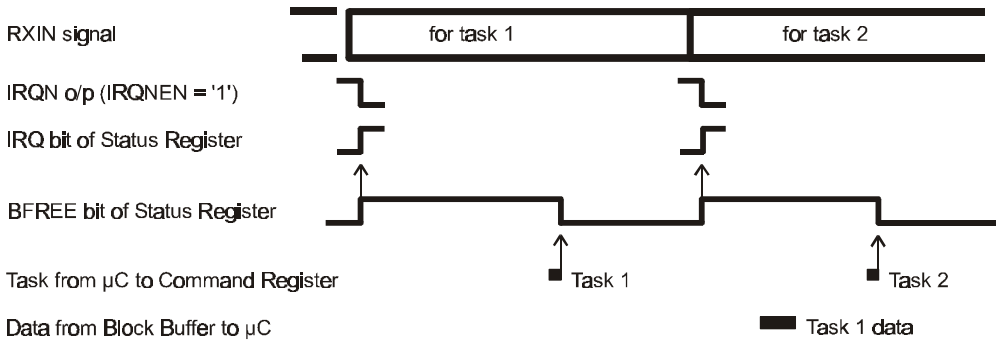


Figure 8 Receive Task Overlapping

Detailed timings for the various tasks are given in Figures 10 and 11.

NULL:
This 'task' allows the AFSD or RXEYE bits to be changed without any other effect.

SFP: Search for Frame Preamble (RD-LAP only)
This task causes the modem to search the received signal for a valid Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID data which has a correct CRC0 checksum.

The task continues until a valid Frame Preamble has been found.

The search consists of four stages:

First of all the modem will attempt to match the incoming symbols against the Frame Synchronisation pattern

Once a match has been found, the modem will read in the following 'S' symbol, place it in the SVAL bits of the Status Register then set the SRDY bit to '1'. (The IRQ bit of the Status Register will also be set to '1' at this time if the SSIEN bit of the Mode Register is '1').

The modem will then read the next 22 symbols as station ID data. They will be decoded and the CRC0 checked. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.

If the received CRC0 is correct, the following 'S' symbol will be read into the SVAL bits of the Status Register and the SRDY, BFREE and IRQ bits set to '1', the CRCERR bit cleared to '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

On detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the 3 Station ID bytes from the Data Block Buffer then write the next task to the modem's Command Register.

RHB: Read Header Block (RD-LAP and MDC)
In RD-LAP mode this task causes the modem to read the next 69 symbols as a 'Header' Block. It will strip out the 'S' symbols then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

In MDC mode this task causes the modem to read the next 112 bits as a 'Header' Block. It will strip out the channel status bits then de-interleave and decode the remaining bits, placing the resulting 4 data bytes and the 2 received CRC bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

In both cases the CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC checksum bytes.

As each of the 'S' symbols or channel status bits of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received in RD-LAP mode the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

RILB: Read 'Intermediate' or 'Last' Block (RD-LAP and MDC)
This task causes the modem to read the next 69 symbols (RD-LAP) or 112 bits (MDC) as an 'Intermediate' or 'Last' block (the µC can tell from the 'Header' block how many blocks are in the frame, and hence when to expect the 'Last' block).

In each case, it will strip out the 'S' symbols or channel status bits, de-interleave and decode the remaining symbols and place the resulting 12 (RD-LAP) or 6 (MDC) bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received then the µC should read out all 12 or 6 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 or 4 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received checksum.

As each of the 'S' symbols or channel status bits of the block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received in RD-LAP mode the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

SFS: Search for Frame Sync (RD-LAP and MDC)
This task causes the modem to search the received signal for a 24-symbol (RD-LAP) or 40-bit (MDC) sequence which matches the required Frame Synchronisation pattern(s) allowing 5 bits in error for MDC mode. In RD-LAP mode the allowable errors are approximately 3 bits when FSTOL = 0, 7 bits when FSTOL = 1.

In RD-LAP mode when a match is found the modem will read in the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to '1' and update the SVAL bits. The µC may then write the next task to the Command Register.

In MDC mode when a match is found the modem will set the BFREE, IRQ bits of the Status Register to ‘1’ and set the FSTYPE bit according to the type of Frame Synchronisation pattern received. The µC may then write the next task to the Command Register.

R4S: Read 4 Symbols (RD-LAP only)
This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by SFS task.

Note that although it is possible to construct message formats which do not rely on the block formatting of the THB, TIB and TLB tasks by using T4S or T24S tasks to transmit and R4S to receive the user’s data, anyone attempting this should be aware that the receive level and timing measurement circuits need to see a reasonably ‘random’ distribution of all four possible symbols in the received signal to operate correctly, and should therefore ‘scramble’ the binary data before transmission.

R8B: Read 8 Bits (MDC only)
This task reads the next 8 received bits and places the resulting 8-bit byte directly (without any attempt to de-interleave, remove channel status bits or apply FEC) into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

RSID: Read Station ID (RD-LAP only)
This task causes the modem to read in and decode the following 23 symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of a SFP task except that it will not re-start if the received CRC0 is incorrect. It would normally follow a SFS task.

The 3 decoded bytes will be placed into the Data Block Buffer, and the CRCERR bit of the Status Register set to '1' if the received CRC0 was incorrect, otherwise it will be cleared to '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY and IRQ bits set to '1' to indicate that the µC may read the 3 received bytes from the Data Block Buffer and write the next task to the modem's Command Register.

RESET: Stop any current action.
This 'task' is similar to the Transmit mode RESET task. It takes effect immediately, and terminates any current task the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. Writing a RESET task to the CMX969 also resets an internal received signal buffer memory used by AFSD function, so that if a RESET task is written while the CMX969 is receiving a Frame Sync pattern then that pattern will not be recognised by the AFSD function.

Task Timings

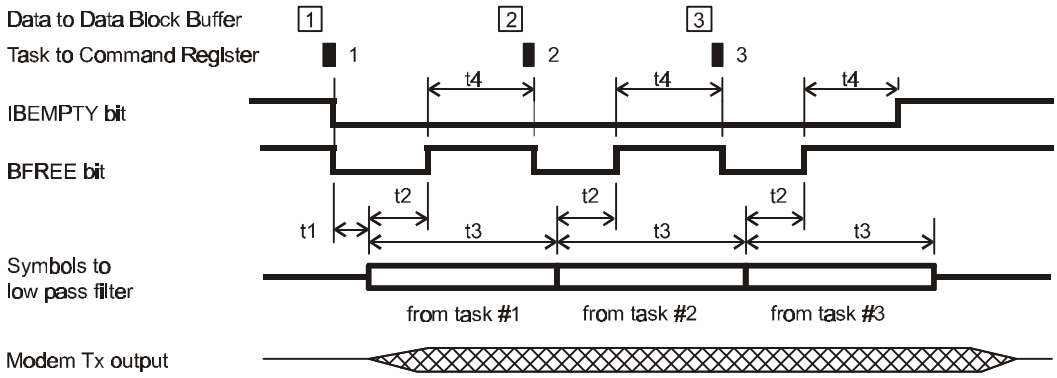


Figure 9 Transmit Task Timing Diagram

	RD-LAP Transmit Task Timings	Task	Time (symbol times)
t1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx filter	Any	1 to 2
t2	Time from application of first symbol of the task to the Tx filter until BFREE goes to a logic '1' (high).	T24S	5
		TSID	6
		THB/TIB/TLB	16
		T4S	0
t3	Time to transmit all symbols of the task	T24S/TSID	24
		THB/TIB/TLB	69
		T4S	4
t4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T24S	18
		TSID	17
		THB/TIB/TLB	52
		T4S	3

	MDC Transmit Task Timings	Task	Time (bit times)
t1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx filter	Any	0 to 1
t2	Time from application of first symbol of the task to the Tx filter until BFREE goes to a logic '1' (high).	T40B	0.5
		THB/TIB/TLB	0.5
		T8B	0.5
t3	Time to transmit all symbols of the task	T40B	40
		THB/TIB/TLB	112
		T8B	8
t4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T40B	38
		THB/TIB/TLB	110
		T8B	6

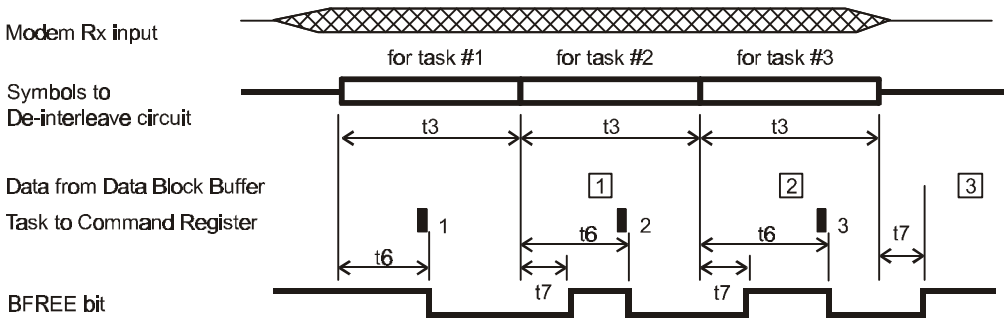


Figure 10 Receive Task Timing Diagram

RD-LAP Receive Task Timings		Task	Time (symbol times)
t3	Time to receive all symbols of block or Frame Sync pattern	SFS/AFSD	25
		SFP	48
		RSID	23
		RHB/RILB	69
		R4S	4
t6	Maximum time between first symbol of the Block or Frrame Sync pattern entering the de-interleave circuit and the task or AFSD being written to the modem's Command Register.	SFS	21
		SFP	21
		RSID	15
		RHB/RILB	51
		R4S	3
t7	Maximum time from the last bit of the block or Frame Sync pattern entering the de-interleave circuit to BFREE or AFSDET going to logic '1' (high)	Any	1

MDC Receive Task Timings		Task	Time (symbol times)
t3	Time to receive all symbols of block or Frame Sync pattern	SFS/AFSD	40
		RHB/RILB	112
		R8B	8
t6	Maximum time between first symbol of the Block or Frame Sync pattern entering the de- interleave circuit and the task or AFSD being written to the modem's Command Register	SFS/AFSD	38
		RHB/RILB	13
		R8B	7
t7	Maximum time from the last bit of the block or Frame Sync pattern entering the de-Interleave circuit to BFREE or AFSDET Going to a logic '1' (high).	SFS/AFSD	2
		RHB/RILB	3
		R8B	2

Lowpass Filter Delay

The previous task timing figures are based on the signal at the input to the low pass filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). In RD-LAP mode there is an additional delay of about 8 symbol times through to the RRC filter in both transmit and receive modes, as illustrated below: The corresponding delay in MDC mode is about 3 symbol times.

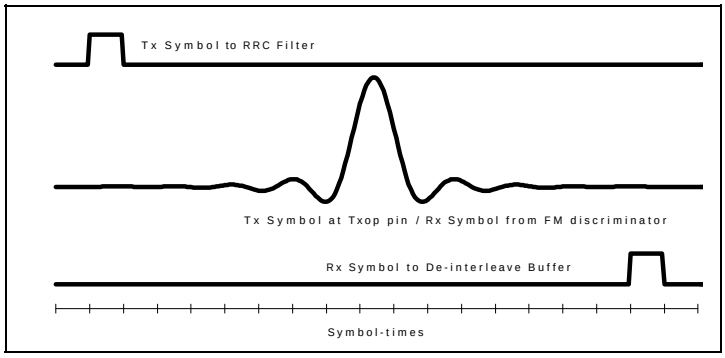
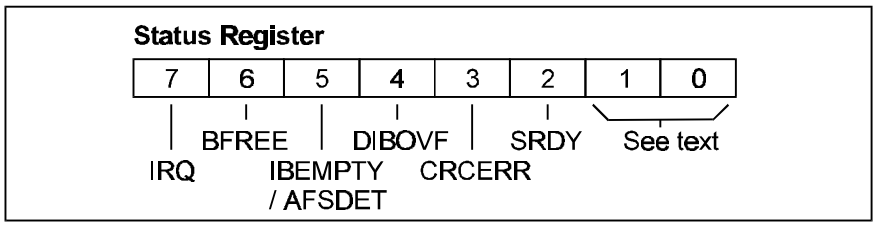


Figure 11 RRC Low Pass Filter Delay (RD-LAP mode)

1.5.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



Status Register B7: IRQ - Interrupt Request
This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register TXRXN, ZP or PSAVE bits.

or The Status Register IBEMPTY/AFSDET bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register TXRXN, ZP or PSAVE bits.

or The Status Register DIBOVF bit going from '0' to '1'.

or The Status Register SRDY bit being set to '1' (due to a 'S' symbol or channel status bit being received or transmitted) if the Mode Register SSIEN bit is '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQNEN bit of the Mode Register is '1', then the chip IRQN output will be pulled low (to V_{SS}) whenever the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

Status Register B6: BFREE - Data Block Buffer Free
This bit reflects the availability of the Data Block Buffer and is cleared to '0' whenever a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register TXRXN, ZP or PSAVE bits are changed.

Status Register B5: IBEMPTY - Interleave Buffer Empty / AFSDET - Autonomous Frame Sync Detect
In transmit mode, this bit signals 'Interleave Buffer Empty' and will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

In transmit mode this bit is also set to '1' by a RESET task or by a change of the Mode Register TXRXN, ZP or PSAVE bits, but in these cases the IRQ bit will not be set.

In transmit mode this bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid level (half-way between '+1' and '-1') signal will be sent to the low pass filter.

In receive mode this bit is set to '1' - also setting the IRQ bit - when the Autonomous Frame Sync circuit is enabled (by setting b7 of the Command Register) and a received Frame Sync pattern is detected. The bit is cleared to '0' immediately after reading the Status Register. To avoid confusion this bit is not set when Frame Sync is detected as part of a RD-LAP SFP task.

In receive mode this bit is also cleared to '0' by a RESET task or by a change of the Mode Register TXRXN, ZP or PSAVE bits.

Status Register B4: DIBOVF - De-Interleave Buffer Overflow
In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB, RSID, R8B or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the TXRXN, ZP or PSAVE bits of the Mode Register.

In transmit mode this bit is '0'.

Status Register B3: CRCERR - CRC Checksum Error
In receive mode this bit will be updated at the end of a SFP, RHB, RILB or RSID task (when BFREE goes high) to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error. In transmit mode this bit will be '0'.

Note that this bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task, or by changing the TXRXN, ZP or PSAVE bits of the Mode Register.

Status Register B2: SRDY - 'S' Symbol Ready
In receive mode this bit is set to '1' whenever an 'S' symbol or channel status bit (other than the 94th bit) has been received. In RD-LAP mode the µC may then read the value of the symbol from the SVAL field of the Status Register. In MDC mode the value of the received channel status bit will be in bit 0 of the Status Register.

In transmit mode this bit is set to '1' whenever an 'S' symbol or channel status bit (other than the 94th bit) has been transmitted.

The bit is cleared to '0' immediately after a read of the Status Register, by a RESET task or by changing the TXRXN, ZP or PSAVE bits of the Mode Register.

Status Register B1, B0: RD-LAP Mode: SVAL - Received 'S' Symbol Value
In receive RD-LAP mode these two bits reflect the value of the latest received 'S' symbol. In transmit mode, these two bits will be '0'.

Status Register B1: MDC Mode: Received Frame Sync Type
In receive MDC mode this bit reflects the type of Frame Synchronisation pattern received:
'0' indicates Frame Sync SYNC1 ($07092A446F, msb first)
'1' indicates Frame Sync SYNC2 (logical inverse of SYNC1)

Status Register B0: MDC Mode: SBIT - Received Channel Status Bit
In receive MDC mode this bit reflect the value of the latest received channel status bit. In transmit mode, this bit will be '0'.

1.5.5.6 Data Quality Register

In receive mode, the CMX969 continually measures the 'quality' of the received signal, by comparing the actual received waveform against an internally generated 'ideal' 2 or 4-level FSK baseband signal.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 12 shows how the value (0-255) read from the Data Quality Register varies with received raw (uncorrected) bit error rate:

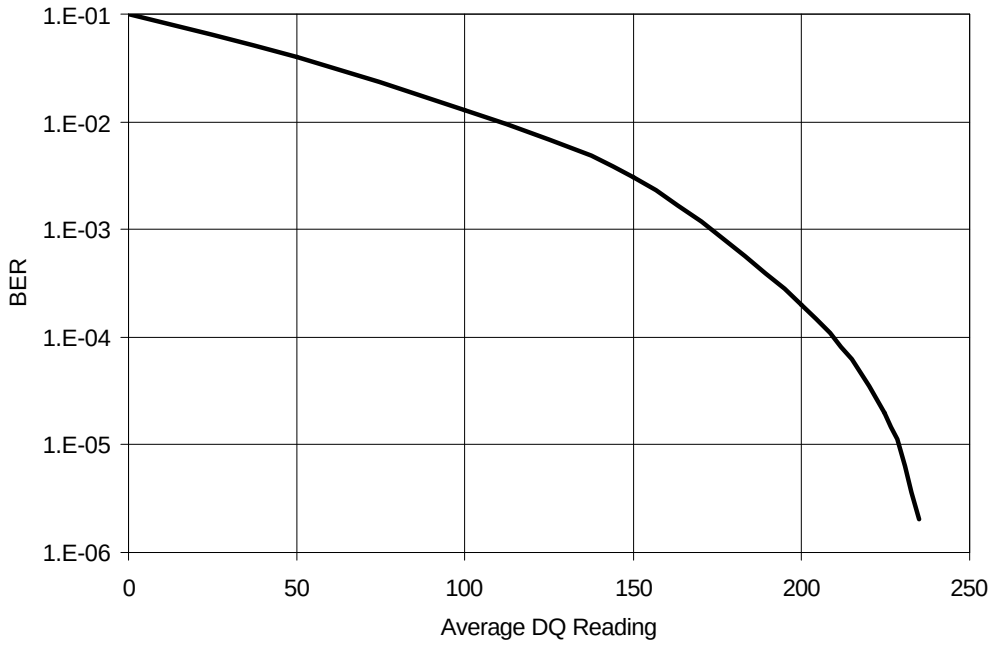


Figure 12 Typical Data Quality Reading vs BER (uncorrected)

The Data Quality readings are only valid when the modem has successfully acquired signal level and timing lock for at least 64 symbol times. A low reading will be obtained if the received signal waveform is distorted in any significant way.

1.6 Application Notes

1.6.1 Autonomous Frame Sync Detect Function

In receive mode the CMX969 needs to know the received signal levels and symbol timing in order to successfully extract the received data from the incoming signal. This can be done by using the AFSD function to establish the levels and timing from the Frame Sync pattern at the start of a received message.

The AFSD function is enabled whenever bit 7 of the Command Register is 1 and operates in parallel with any other receive task that may be running. It monitors the received signal for the presence of a Frame Sync pattern without regard for any preconceived idea of the symbol timing or levels. When a Frame Sync pattern is found the AFSD function then uses it to establish the optimum timing and levels for extracting the following data.

This contrasts with the SFS and SFP (Search for Frame Sync and Search for Frame Preamble) tasks that rely on previously established timing and level information and - when a Frame Sync pattern is detected - do not change these timing and level settings.

On detecting a Frame Sync pattern the AFSD function sets the AFSDET and IRQ bits of the Status Register and terminates any other current task.

AFSD should be enabled to look for a Frame Sync pattern whenever the CMX969 is switched to receive mode or the radio is switched to a new receive channel or when the transmitter may have been switched off - in fact in any circumstance where the correct levels and timing need to be re-established.

Once Frame Sync has been detected the AFSD function may be switched off if it is known that the transmitter is sending continuous concatenated frames, in which case SFS or SFP tasks should be used to find subsequent Frame Sync patterns. Alternatively, the AFSD function may be used instead of SFS to find all received Frame Sync patterns.

If the system is operating in SFR (Single Frequency Re-use) mode and so has to be able to detect the start of a new (stronger) transmission then AFSD should be left running so that it can detect the new transmitter and automatically abort any current task and adjust the timing and level settings to suit the new signal.

1.6.2 Rx Control Procedure

The following procedure illustrates how the CMX969 can be controlled to receive one or more messages in MDC mode. RD-LAP mode is similar except that the first block of each message will be a Station ID block.

Step	Action	Notes
0	Switch radio onto receive channel. CMX969 Mode Register IRQNEN, INVSYM and SSIEN bits should be set as required, other bits 0. Control Register should have CKDIV bits set as required, MDC bit = 1, all other bits 0.	
1	Write RESET + AFSD (87h) to Command Register	Reset the device and start searching for a Frame Sync pattern using AFSD. AFSD should always be used instead of SFS to look for the fist Frame Sync when switching into Rx mode or when the Rx channel is changed.
2	Wait for Status Register AFSDET bit to go to 1	AFSDET will go to 1 when Frame Sync is detected.
3	Write RHB + AFSD (82h) to Command Register.	Tell the CMX969 to receive and decode the first Header block. Keep AFSD function running in case a false Frame Sync had been detected or in case a new transmitter starts up on this radio channel.
4	Wait for Status Register AFSDET or BFREE bits to go to 1. If AFSDET bit = 1 then a new Frame Sync has been detected so go to step 3. If AFSDET = 0 and BFREE = 1 the previous Rx task (RHB or RILB) has completed. Read Rx data from Data Buffer. Check the Status Register CRCERR bit if it was a Header block or the 'last' Data block.	Wait for the CMX969 to finish the current task or for the AFSD function to recognise a new Frame Sync. If a new Frame Sync has been detected then it is the start of a new message to abandon the 'old' one and start to receive and decode the 'new' one. CMX969 has received and decoded a Header Intermediate or Last block. Read the data and check the CRC if the block contained one.

5	To receive and decode the next block from this Rx message write AFSD + RHB or RILB (82h or 83h) to the Command Register and go to step 4. If we have received all of the blocks in the message or wish to ignore any following blocks in this message then write AFSD (80h) to the Command Register and go to step 2.	If we want to continue receiving the rest of this Rx message then tell the CMX969 to receive and decode the next block. Keep the AFSD function running in case a new transmitter starts up on this channel (SFR). AFSD will detect the next Fram Sync pattern. See note.

Note: Once a Frame Sync pattern has been detected with AFSD then if the radio is receiving concatenated messages and if the system does not employ Single Frequency Reuse techniques subsequent Frame Sync patterns may be detected by using a SFS task (04h) instead of AFSD. Using SFS will reduce the, very small, chance of a false Frame Sync detection. Note that the SFS task signals that it has found a Frame Sync pattern by setting the Status Register BFREE bit to 1, whereas AFSD sets the AFSDET bit.

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

P4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

E2 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		400	mW
... Derating		5.3	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D5 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.
Correct operation for supply voltages less than 3.0V is subject to a restricted temperature range.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C
Symbol Rate		2000	9700	Symbols/sec
Xtal Frequency		1.0	10.0	MHz

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152MHz.
Symbol Rate = RD-LAP mode 9600 symbols/sec, MDC mode 4800 symbols/sec.
V_{DD} = 3.0V to 5.5V, Tamb = - 40°C to +85°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (V_{DD} = 5.0V)	1		4.0	9.0	mA
I_{DD} (V_{DD} = 3.0V)	1		2.5	5.0	mA
I_{DD} (Powersave Mode, V_{DD} = 5.0V)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.8		mA
I_{DD} (Zero Power Mode, V_{DD} = 5.0V)	1, 1a			10.0	µA
AC Parameters					
Tx Output					
TXOP Impedance	2		1.0	2.5	kΩ
Signal Level RD-LAP	3	1.6	2.0	2.4	V p-p
Signal Level MDC	3	0.71	0.89	1.07	V p-p
Output DC Offset wrt V_{DD}/2	4	-0.25		+0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (I/P = 1mVrms at 100Hz)			300		V/V
Input Signal Level RD-LAP	5	1.0		2.5	V p-p
Input Signal Level MDC	5	0.5		1.2	V p-p
Input DC Offset wrt V_{DD}/2	5	-1.0		+1.0	V
Xtal Input					
'High' Pulse Width	6	40.0			ns
'Low' Pulse Width	6	40.0			ns
Input Impedance (at 100Hz)		10.0			MΩ
Inverter Gain (I/P = 1mVrms at 100Hz)		20.0			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (Vin = 0 to V_{DD})	7, 8	-5.0		+5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (Vout = V_{DD})	9			10.0	µA

Notes:
1. At 25°C. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
1a Mode Register TXRXN bit set to 0.
2. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C.
3. For a "+3 +3 -3 -3...." symbol sequence in RD-LAP mode, “+1 -1 ..” in MDC mode, at V_{DD} = 5.0V and Tamb = 25°C (Tx output level is proportional to V_{DD}).
4. Measured at the TXOP pin with the modem in Rx or Tx idle mode.

5. For optimum performance, measured at RXFB pin, for a "...+3 +3 -3 -3..." symbol sequence in RD-LAP mode, "+1 -1 " in MDC mode, at V_{DD} = 5.0V and Tamb = 25°C. The optimum input level and DC offset values are proportional to V_{DD}. Signal peaks should not go outside the range of (V_{SS} + 0.25V) to (V_{DD} – 0.25V).
6. Timing for an external input to the XTAL pin.
7. WRN, RDN, CSN, A0 and A1 pins.
8. D0 - D7 pins.
9. IRQN pin.

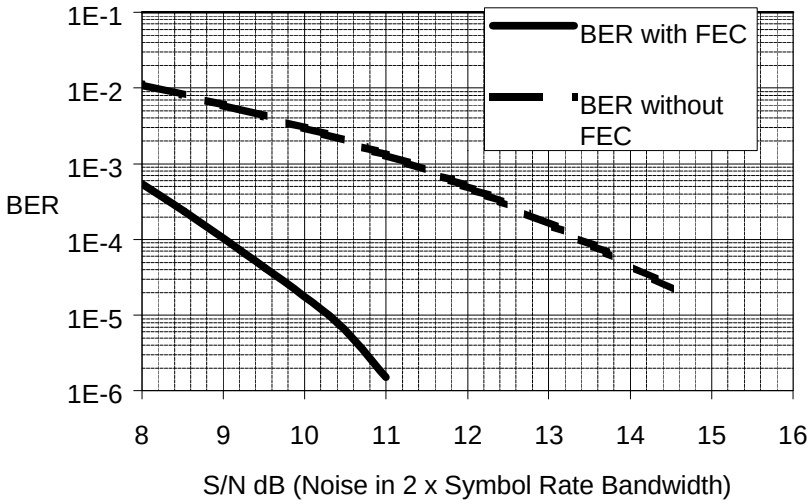


Figure 13a Typical Bit Error Rate With and Without FEC: RD-LAP Mode

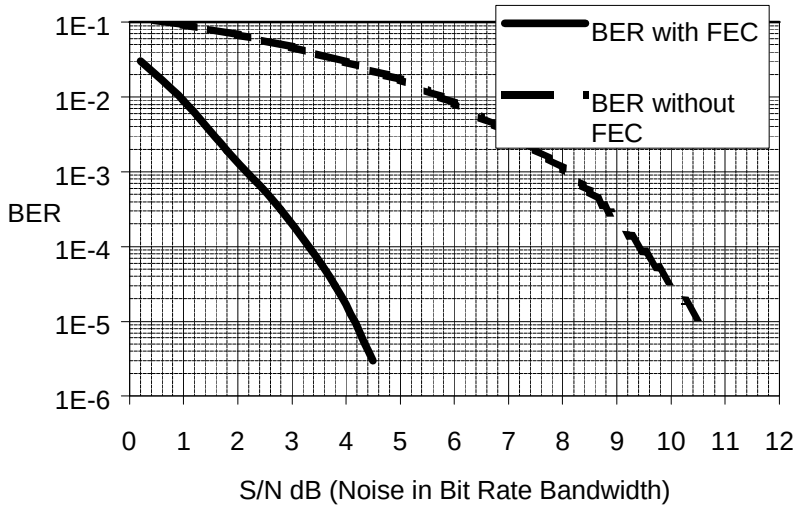


Figure 13b Typical Bit Error Rate With and Without FEC: MDC Mode

Note: BER vs. S/N measured under nominal working conditions, after a Frame Sync has been detected using AFSD, with pseudo-random data.

		Notes	Min.	Typ.	Max.	Units
µC Parallel Interface Timings (ref. Figure 14)						
t_{ACSL}	Address valid to CSN low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	CSN hold time		0			ns
t_{CSHI}	CSN high time	10	6.0			clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90.0			ns
t_{RHCSL}	RDN high to CSN low time (write)		0			ns
t_{RACL}	Read access time from CSN low	11			175	ns
t_{RARL}	Read access time from RDN low	11			145	ns
t_{RL}	RDN low time		200			ns
t_{RX}	RDN high to D0-D7 3-state time				50.0	ns
t_{WHCSL}	WRN high to CSN low time (read)		0			ns
t_{WL}	WRN low time		200			ns

Notes: 10. Xtal clock cycles at the XTAL pin.
11. With 30pF max to V_{SS} on D0 - D7 pins.

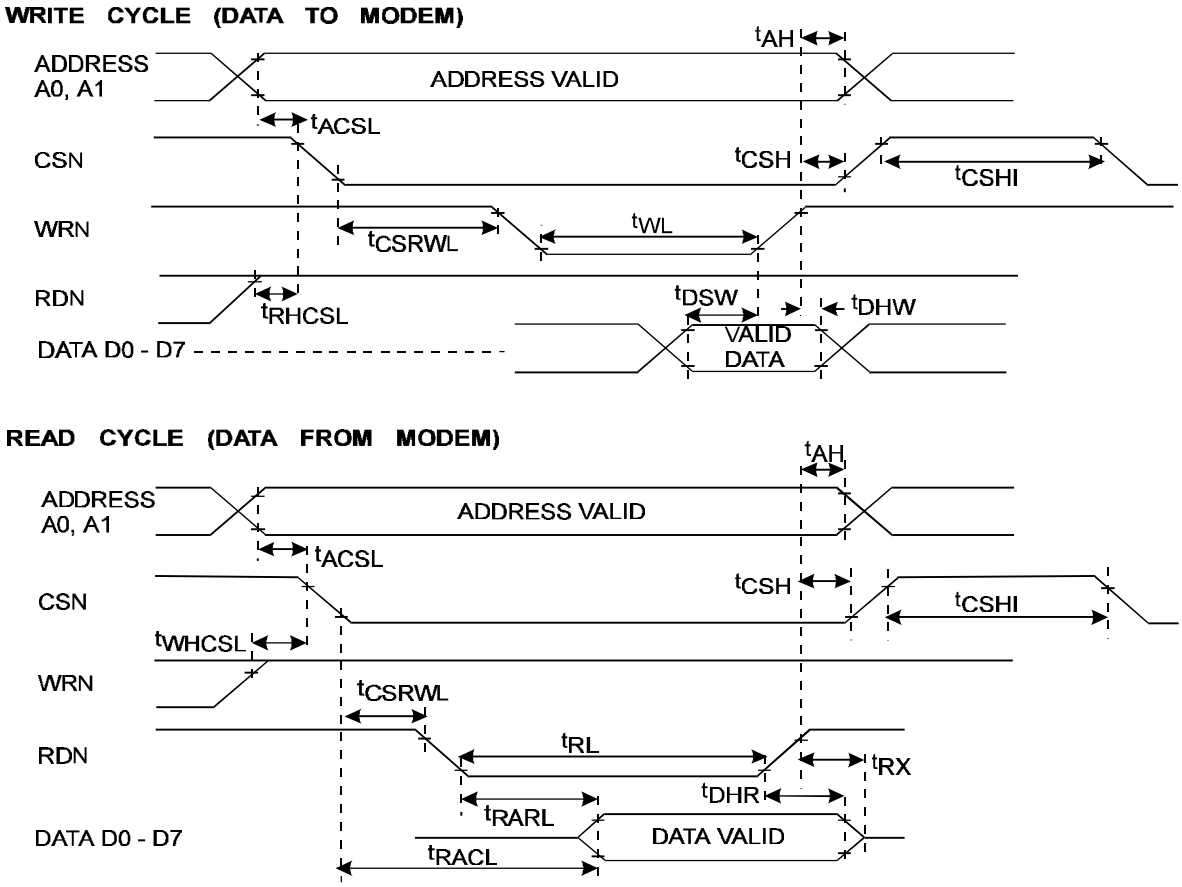
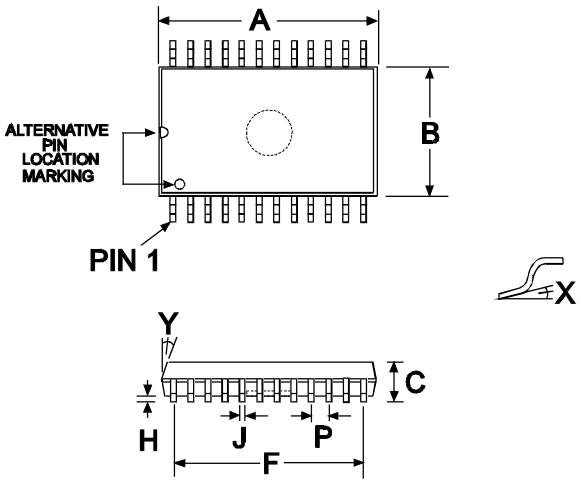


Figure 14 µC Parallel Interface Timings

1.7.2 Packaging



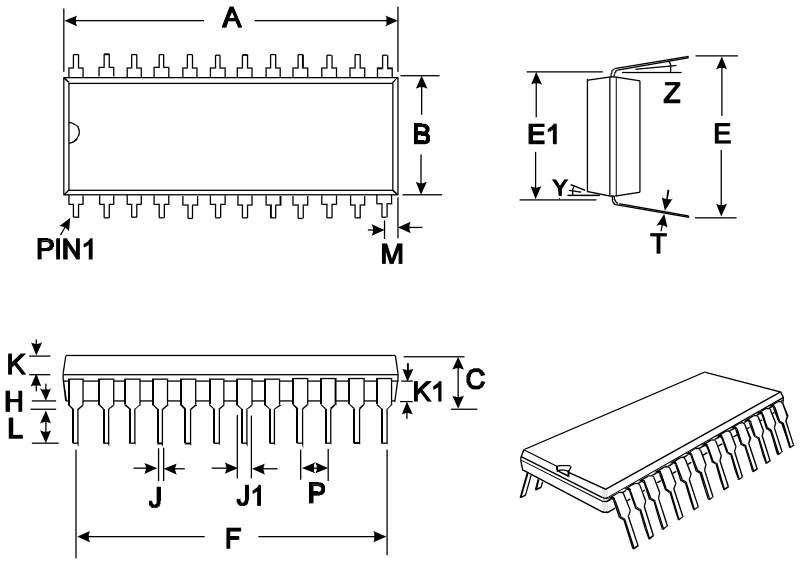
DIM.	MIN.	TYP.	MAX.
* A	0.303 (7.70)		0.311 (7.90)
* B	0.169 (4.30)		0.177 (4.50)
C	-----		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.286 (7.15)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 15 E2 Mechanical Outline: *Order as part no. CMX969E2*



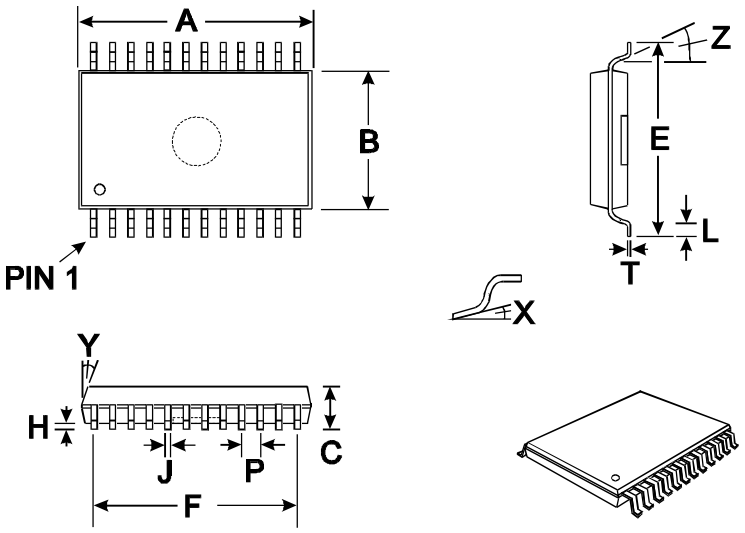
DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 16 P4 Mechanical Outline: *Order as part no. CMX969P4*



	DIM.	MIN.	TYP.	MAX.
*	A	0.318 (8.08)		0.328 (8.33)
*	B	0.205 (5.21)		0.213 (5.39)
	C	0.066 (1.67)		0.079 (2.00)
	E	0.301 (7.65)		0.312 (7.90)
	F		0.281 (7.15)	
	H	0.002 (0.05)		0.008 (0.21)
	J	0.010 (0.25)		0.015 (0.38)
	L	0.022 (0.56)		0.037 (0.94)
	P		0.026 (0.65)	
	T	0.005 (0.13)		0.009 (0.23)
	X	0°		8°
	Y	7°		9°
	Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 17 D5 Mechanical Outline: *Order as part no. CMX969D5*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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