Advance Information

Advanced Continuous Gate* Technology 1.5-Micron CMOS Gate Array Series

Features:

- *Continuous Gate architecture offers maximum layout efficiency with 30% gate utilization for random logic netlists*
- *Available in 13 sizes from 960 to 54,000 usable gates (3,200 to 180,000 available gates)*
- *Proven 1.5-micron (drawn) silicon-gate double-level-metal CMOS technology*
- *High performance with balanced drive-0.56 ns typical for a 2-input NAND gate with a fanout of 2 (0.21-pF load)*
- *TTL, CMOS, and Schmitt Trigger I/O compatibility*
- *Flip-flop toggle frequency 250 MHz*
- *Selectable output drive from 2 to 16 mA*
- *Separate I/O and core power bus capability for noise reduction*
- *Extensive portable Macro libary*
- *Workstation support for schematic capture and simulation*
- *Fully supported by Harris integrated CAE tools*
- *High reliability-with 2000 V ESD and 400 mA at 125°C*

The CGA200 Series is an advanced, high-performance, CMOS gate-array family using the Harris proprietary Continuous Gate technology in which high transistor densities are achieved by means of a special array architecture. Continuous Gate technology along with a unique global routing scheme enable the CGA200 Series to offer high speed, very high gate counts, and maximum layout efficiency in which 30% of the total gates can be used. With its extremely high performance, high gate count, and high layout efficiency, the CGA200 Series is ideally suited to meet the user's design requirements for complex system integration and low power dissipation.

Designed with true 1.5-micron silicon-gate design rules, the CGA200 Series is fabricated on an advanced, double-level-metal, planarized, fully-implanted CMOS process. With typical effective channel lengths of 1.2 microns and reduced junction area capacitance, the CGA200 Series allows system clock speeds of up to 60 MHz. An internal 2-input NAND gate, with a fanout of 2 exhibits a typical propagation delay of just 0.56 ns. Operating from a single 5-volt power supply, the CGA200 Series of gate arrays exhibits extremely low power dissipation, typically 15 μW/gate/MHz.

In addition to standard commercial product, the CGA200 Series of gate arrays are available with Class B-type screening for applications requiring high reliability and -55°C to +125°C temperature-range operation.

CGA200 Gate-Array Series

DEVICE NUMBER	EQUIVALENT GATES[1]	ESTIMATED USABLE GATES[2]	MAXIMUM I/O PADS[3]
CGA200-003	3,200	960	48
CGA200-006	6,728	2,018	68
CGA200-010	10,952	3,285	88
CGA200-017	17,672	5,302	112
CGA200-024	24,200	7,260	128
CGA200-029	28,800	8,640	140
CGA200-033	33,800	10,140	152
CGA200-042	42,632	12,790	172
CGA200-056	56,448	16,934	196
CGA200-073	73,728	22,118	224
CGA200-109	109,512	32,854	272
CGA200-145[4]	145,800	43,740	312
CGA200-180[4]	180,000	54,000	348

1. An equivalent gate is defined as one 2-input NAND.
2. Estimated usable gates is 30% of the available gate count. The actual number of usable gates may vary, depending on the design. Typical usage is 75% of this number.
3. Eight additional pads are dedicated, four as V_{SS} pads and four as V_{DD} pads. All I/O pads are programmable to V_{DD} or V_{SS}.
4. Contact Harris Semiconductor Marketing.

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File Number **2228**

File No. 2228 **CGA200 Series**

T-42-11-09

MAXIMUM RATINGS, *Absolute-Maximum Values:*
(Voltages referenced to V_{SS} Terminal)

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... -0.5 to +6 V
RECOMMENDED DC OPERATING VOLTAGE RANGE (V_{DD}) ..... 3 to 5.5 V
DC INPUT VOLTAGE RANGE, ALL INPUTS, (V_{IN}) ..... -0.5 to V_{DD} +0.5 V
DC OUTPUT VOLTAGE RANGE, ALL OUTPUTS, (V_{OUT}) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±20 mA
POWER DISSIPATION PER PACKAGE (P_D):
For Industrial Temperature Range: -40 to +85°C
For T_A=-40 to +60°C ..... 500 mW
For T_A=+60 to +85°C ..... Derate Linearly at 12 mW/°C to 200 mW
For Extended Temperature Range: -55 to +125°C
For T_A=-55 to +100°C ..... 500 mW
For T_A=+100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
POWER DISSIPATION PER OUTPUT (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGE ..... -55 to +125°C
PLASTIC PACKAGE ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

DC CHARACTERISTICS, Specified at V_{DD} and Ambient Temperature over the Designated Range[1]

CHARACTERISTIC		TEST CONDITIONS	MIN.	MAX.	UNITS
Input HIGH Voltage	V_{IH}				
CMOS		Guaranteed Input HIGH Voltage	0.7 x V_{DD}	V_{DD}	V
TTL			2	V_{DD}	
Input LOW Voltage	V_{IL}				
CMOS		Guaranteed Input LOW Voltage	-0.5	0.3 x V_{DD}	V
TTL			-0.5	0.8	
Schmitt-Trigger Positive-Going Threshold	V_{T+}		2.5	—	V
Schmitt-Trigger Negative-Going Threshold	V_{T-}		—	2	V
Output HIGH Voltage	V_{OH}	I_{OH} = -1 µA	V_{DD} - 0.05	—	
PT6O01		I_{OH} = -2 mA	2.4	—	
PT6O02		I_{OH} = -4 mA	2.4	—	V
PT6O03		I_{OH} = -8 mA	2.4	—	
PT6O04		I_{OH} = -12 mA	2.4	—	
PT6O05		I_{OH} = -16 mA	2.4	—	
Output LOW Voltage	V_{OL}	I_{OL} = 1 µA	—	0.05	
PT6O01		I_{OL} = 2 mA	—	0.4	
PT6O02		I_{OL} = 4 mA	—	0.4	V
PT6O03		I_{OL} = 8 mA	—	0.4	
PT6O04		I_{OL} = 12 mA	—	0.4	
PT6O05		I_{OL} = 16 mA	—	0.4	
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} or Gnd	-10	10	µA
3-State Output Leakage Current	I_{OZ}	V_{OUT} = V_{DD} or Gnd	-10	10	µA

CAPACITANCE, Specified at V_{DD} and Ambient Temperature Over the Designated Range[1]

CHARACTERISTIC[2]		TEST CONDITIONS	MIN.	MAX.	UNITS
Input Pad Capacitance	C_{IN}	Excluding Package	—	5	pF
Output Pad Capacitance	C_{OUT}				
Transceiver Pad Capacitance	$C_{I/O}$				

1. Extended temperature range is -55°C to +125°C, ± 10% power supply; industrial temperature range is -40°C to +85°C, ± 5% power supply; commercial temperature range is 0°C to +70°C, ± 5% power supply.
2. For cell pads only.

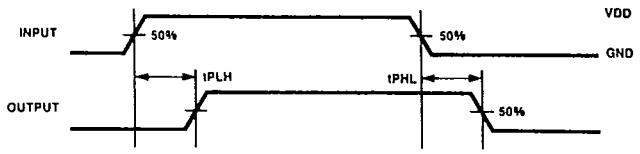
AC CHARACTERISTICS FOR SELECTED MACROS, T_J = 27° C, V_{DD} = 5 V, Process Model = Typical

MACRO	DESCRIPTION	SYMBOL	PROPAGATION DELAY (ns)[1] - FANOUT				
			1	2	3	4	6
Logic Gates							
IN01D1	1X Inverting Buffer	t_{PLH}	0.46	0.61	0.77	0.92	1.17
		t_{PHL}	0.26	0.31	0.36	0.46	0.56
IN01D2	2X Inverting Buffer	t_{PLH}	0.31	0.36	0.46	0.51	0.66
		t_{PHL}	0.15	0.20	0.20	0.26	0.31
ND02D1	2-Input NAND	t_{PLH}	0.56	0.71	0.87	1.02	1.33
		t_{PHL}	0.36	0.46	0.56	0.71	0.92
ND04D1	4-Input NAND	t_{PLH}	0.71	0.87	1.02	1.17	1.48
		t_{PHL}	0.82	1.02	1.26	1.48	1.89
NR02D1	2-Input NOR	t_{PLH}	0.82	1.07	1.38	1.68	2.25
		t_{PHL}	0.31	0.36	0.46	0.51	0.66
NR04D1	4-Input NOR	t_{PLH}	1.53	1.68	1.84	1.99	2.30
		t_{PHL}	0.97	1.02	1.07	1.12	1.26
XN02D1	2-Input Exclusive-NOR	t_{PLH}	0.77	0.92	1.07	1.17	1.48
		t_{PHL}	0.41	0.51	0.61	0.66	0.82
Flip-Flops & Latches							
DFBTNB	Buffered D Flip-Flop (Clock → Q)	t_{PLH}	2.09	2.24	2.40	2.55	2.86
		t_{PHL}	2.35	2.45	2.50	2.55	2.70
		t_S	0.90	0.90	0.90	0.90	0.90
		t_H	0	0	0	0	0
LANFNB	Buffered Latch (D → Q)	t_{PLH}	1.02	1.17	1.33	1.48	1.79
		t_{PHL}	1.68	1.79	1.84	1.89	2.04
		t_S	1.30	1.30	1.30	1.30	1.30
		t_H	0	0	0	0	0
Input Buffers							
LSTC00	TTL Input Buffer	t_{PLH}	0.51	0.56	0.61	0.66	0.71
		t_{PHL}	1.02	1.02	1.02	1.02	1.07
LSCC00	CMOS Input Buffer	t_{PLH}	0.56	0.56	0.56	0.61	0.66
		t_{PHL}	0.66	0.71	0.71	0.71	0.77
Output Buffers							
			CAPACITIVE LOAD (pF)				
			15	50	85	100	
PC6O05	Output Buffer with 16-mA Drive	t_{PLH}	2.35	4.18	5.97	6.73	
		t_{PHL}	1.94	2.70	3.52	3.83	

2

TIMING DIAGRAM

PROPAGATION DELAY



Note:
1. Delays through interconnect are not included.

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AC Performance

AC performance for a given operating condition is a function of several factors including: fanout, interconnect, supply voltage, junction temperature, and process variability.

The AC characteristics table shows the propagation delay (TDNOM) on a number of commonly used macros for a typical process model, 5-volt operation, and 27° C junction temperature.

The effect of supply voltage can be determined from Fig. 1 by extracting the factor KV. Fig. 2 is used to determine the temperature factor KT. A worst-case process factor (KPMAX) of 1.45, and a best-case process factor (KPMIN) of 0.67. as shown in Fig. 3, are used to determine the effects of process variability.

The worst-case propagation delay can be calculated as follows:

TDMAX = KV x KT x KPMAX x TDNOM

and the best-case delay is calculated:

TDMIN = KV x KT x KPMIN x TDNOM

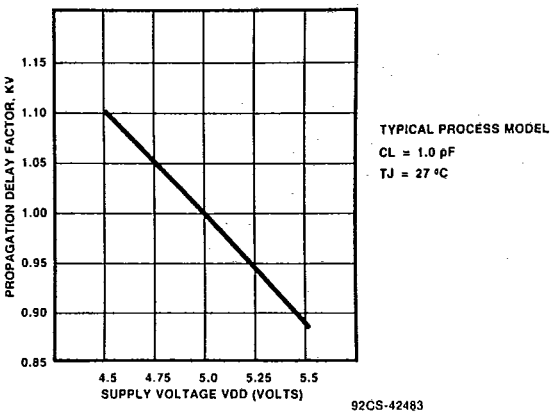

Fig. 1. - Performance vs. voltage.

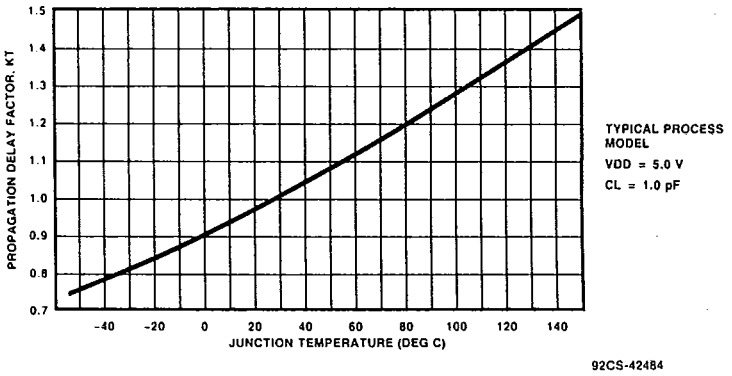

Fig. 2 - Performance vs. temperature.

Process Model	Factor KP
Slow	1.40
Typical	1
Fast	0.71

Fig. 3 - Performance vs. process.

Array Organization

The general layout of the CGA200 Series consists of electrical components that are organized as structures of continuous arrays of transistor pairs. Macrocells, which are the basic building blocks of logic design, are comprised of one or more transistor pairs in the arrays.

All of the CGA200 Series gate arrays use the same transistor array and I/O cell structure. Thus, the same macros can be used throughout the CGA200 Series. The power busing structure of the CGA200 Series can isolate the I/O cells from the internal array. Both the V_{DD} and the V_{SS} buses surround the array in the second-level metal and are brought into the internal array via a power rail structure. The power bus structure also allows any pad to be programmed as V_{DD} or V_{SS}.

Internal Array Description

The CGA200 Series, using Continuous Gate technology, consists internally of rows of uncommitted p and n transistors laid out at continuous regular intervals. Key features of the Continuous Gate technology are:

1. Bent gate technology which allows the poly gate of a device to be in alignment with the source and drain area of the transistor.
2. High gate density arising from special array architectural features.
3. A unique global routing scheme that maximizes gate utilization, and allows for faster place and route.

The bent gate feature allows transistors to be placed two times closer than the traditional channelless architecture. This compaction not only minimizes the source and drain areas but also greatly reduces stray diffusion capacitance.

Other unique architectural features include the use of gate isolation, specially contoured poly nodes, and metal-one strapping of source-drain diffusion areas. In the traditional approaches, active regions are isolated from one another by a thick field oxide. This is referred to as oxide isolation and may consume 20% of the total core area. In comparison, the gate isolation technique employed in Continuous Gate technology turns off transistors to isolate active regions from one another. These isolation transistors are placed only where needed, therefore achieving higher silicon efficiency.

Specially contoured poly nodes are used throughout the array to minimize the vertical metal routing required to connect each of the nodes. This, in turn, allows for more horizontal metal routing tracks to be available, thus increasing routing efficiency and silicon utilization.

The global routing scheme for gate arrays built on the Continuous Gate technology architecture is quite unique. Rather than having open areas for routing channels, as in the traditional approach, the routing channels actually run over the utilized cells. Furthermore, local routing for macrocells does not compete with global routing for the required routing resources, thus allowing greater ease in routing.

I/O Buffers

Output Portion:

The output portion of the I/O buffer contains pre-drive logic, as well as programmable output drive. The output buffers have been designed to source or sink 2, 4, 8, 12, or 16 mA.

Input Portion:

Each input location may be programmed as TTL, CMOS, or Schmitt Trigger.

General:

The I/O incorporates a dual power bus structure which may be used to isolate the output buffer power supply from that of the array core, thus achieving high noise immunity. Any I/O location may also be programmed as Power or Ground. All I/Os are protected against latch-up and static discharge. In addition, pull-up and pull-down resistors are available for use in combination with each I/O. Typical performance features are shown in the AC Characteristics table.

Workstations

Harris gate-array designs may be developed on workstations supported by Harris. Designers using such workstations are provided with a macro library containing the symbols, simulation models and software for design verification, ERCs, timing calculations and netlist generation. The design is transferred to a Harris design center where placement and routing are performed. The final interconnect capacitances are annotated back to the workstation for verification of circuit performance.

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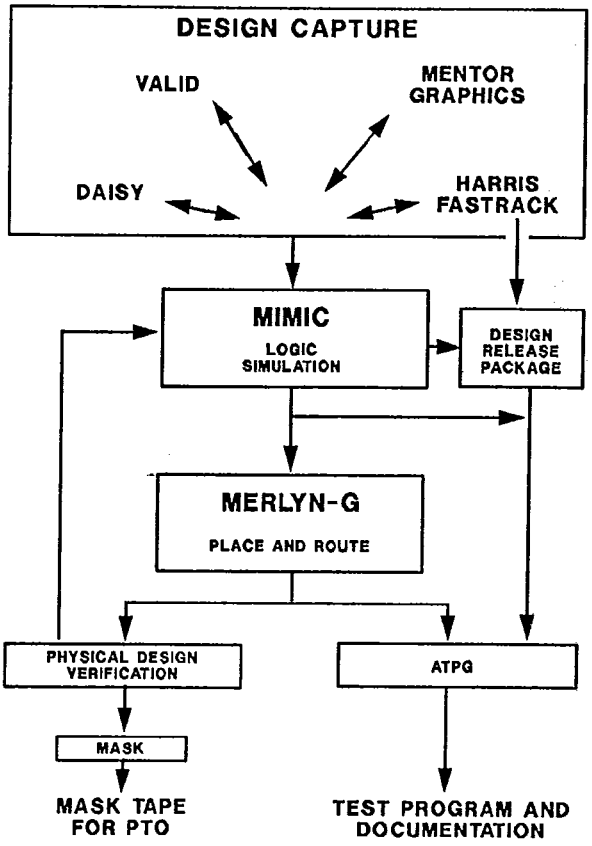
ASIC Design Flow

The Harris CGA200 Series is supported by a complete set of design automation tools. The design flow and the highlights of the design tools that are utilized with the standard-cell library are as follows:

- **MIMIC, The Harris Software Simulation Program**—A powerful software simulation program allows designers of ASIC circuits to model the logical operation of the circuits before device fabrication. Through the program, designers can discover logical flaws; race, hazard, or spike conditions; and timing uncertainties.



FASTRACK uses the logic descriptions of MIMIC to implement the layout and control the connectivity verification and mask-generation routines.

Fig. 4 - FASTRACK ASIC design system.