T-52-33-15

ADS4360A

Streaming

Tape Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

1.1 FEATURES

- Single chip QIC-36 tape controller
- QIC-24 and QIC-11 media formats
- Separate microprocessor and tape data busses
- Synchronous or asynchronous tape data bus transfers
- Generic CPU bus interface with interrupts
- Built-in crystal driver
- NRZ serial input/output
- Data compare
- 68-pin PLCC package

1.2 GENERAL DESCRIPTION

The ADS-4360A is a VLSI 68-pin leaded plastic chip which interfaces with standard quarter-inch streaming tape drives. It provides the necessary logic to build a tape controller utilizing minimal number of chips. In addition, the ADS-4360A provides a wide range of uses due to its highly flexible interfaces.

The ADS-4360A handles all operations involving serial-to-parallel and parallel-to-serial data conversion. For write operations, the ADS-4360A takes 8-bit bytes and converts them into the correct 10-bit GCR bit streams for recording. Similarly, for read operations, the ADS-4360A receives serial GCR data and converts it to 8-bit bytes. Higher bandwidth systems can easily use the ADS-4360A because the tape data bus and microprocessor data bus are separate.

Depending upon the type of buffer controller selected for a particular application, ADS-4360A operates in either synchronous or asynchronous mode.

The ADS-4360A provides a data verification option which performs a bit-by-bit data comparison.

In addition to the data read/write sequencers, the ADS-4360A has ten microprocessor controlled output bits and six input bits. These I/O lines control the mechanical operation of the tape drives, such as motor direction and track selection.

2.0 ARCHITECTURE

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The ADS-4360A is comprised of seven functional blocks (See Figure 1):

1. The MICROPROCESSOR INTERFACE block interfaces with any 8-bit microprocessor having a multiplexed address/data bus. It also accommodates microprocessors having separate address and data busses. The ADS-4360A generates all necessary strobes for reading or writing data to the microprocessor. It works with microprocessors that use strobed addresses (8085,8088) or unstrobed addresses (Z80).

2. The TAPE I/O INTERFACE block consists of all control signals necessary to interface to a streaming tape drive. These programmed I/O signals control items such as motor direction, write enabling and track selection.

3. The WRITE SEQUENCER block takes 8-bit parallel data, serializes it, converts it to GCR and sends it out in blocks of 512 bytes. The ADS-4360A appends a 16-bit cyclical redundancy check polynomial (CRC) and identifying block number after the data is sent out. The WRITE SEQUENCER provides an interrupt signal for microprocessor timing.

4. The READ SEQUENCER operates in the same fashion as the WRITE SEQUENCER except it receives serial GCR data and converts it to 8-bit bytes. The READ SEQUENCER provides an interrupt signal for microprocessor timing. When operating simultaneously with the WRITE SEQUENCER, it performs read-after-write, data verify and data recovery operations.

5. The BLOCK REGISTER consists of four 8-bit registers used for block identification during read and write operations. The controlling microprocessor loads and unloads the block register as necessary.

6. The TAPE DATA INTERFACE transfers data required by the WRITE SEQUENCER or generated by the READ SEQUENCER. It is an 8-bit bus that is separate from the microprocessor data bus. It operates in synchronous or asynchronous mode.

7. The DATA COMPARE LOGIC block compares data written into the ADS-4360A, while it simultaneously reads data from the tape for a bit-by-bit comparison between the two data streams.

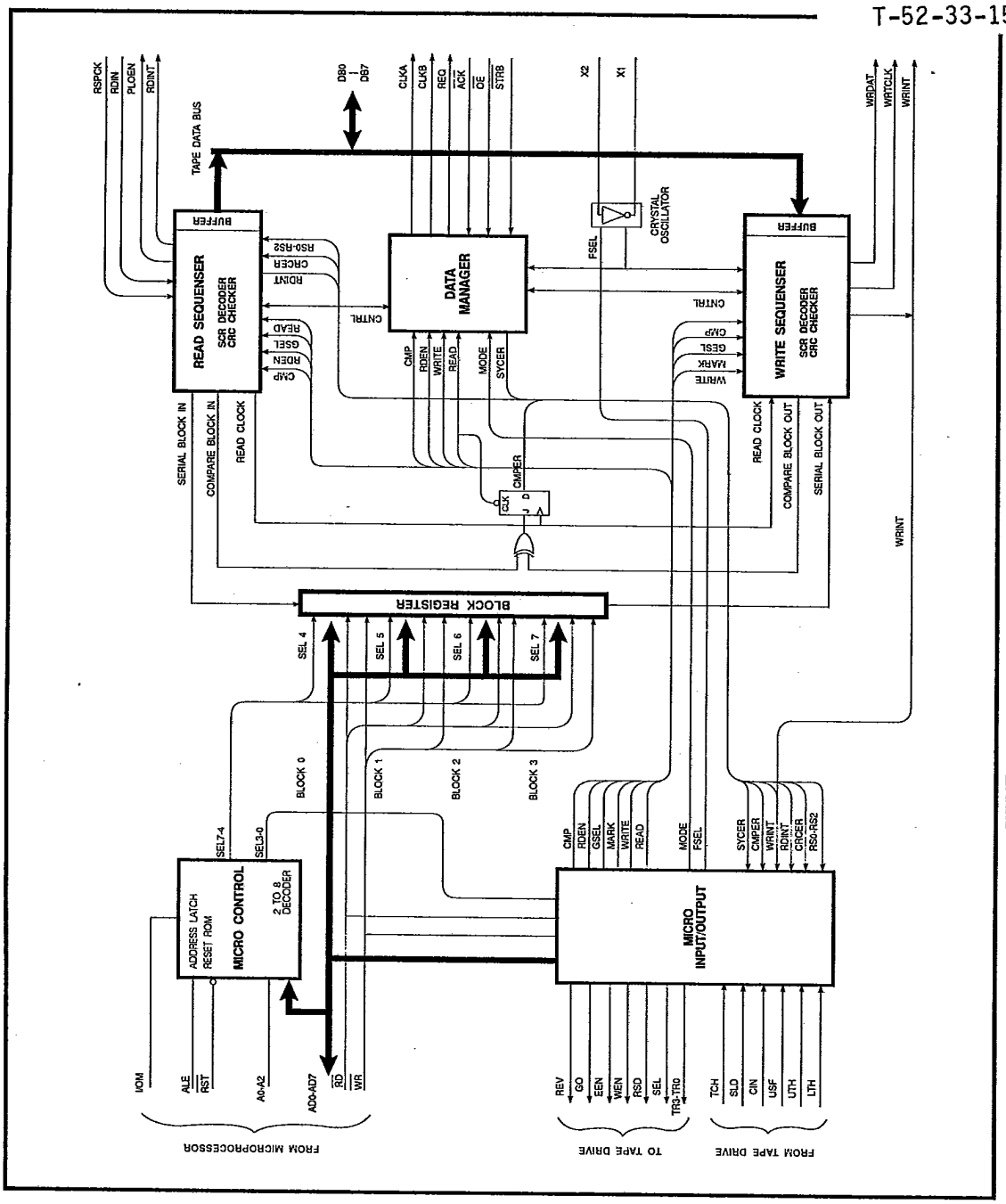

FIGURE 1. ADS-4360A BLOCK DIAGRAM

3.0 PIN DESCRIPTION

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Figure 2 is a pinout drawing of the ADS-4360A.

Table 1 provides signal-to-pin descriptions for the ADS-4360A. Table 1 uses the following conventions:

I indicates that a signal is an input to the ADS-4360A.

O indicates that a signal is an output from the ADS-4360A.

I/O indicates that a signal is bidirectional.

** Dual function signal, used for test mode

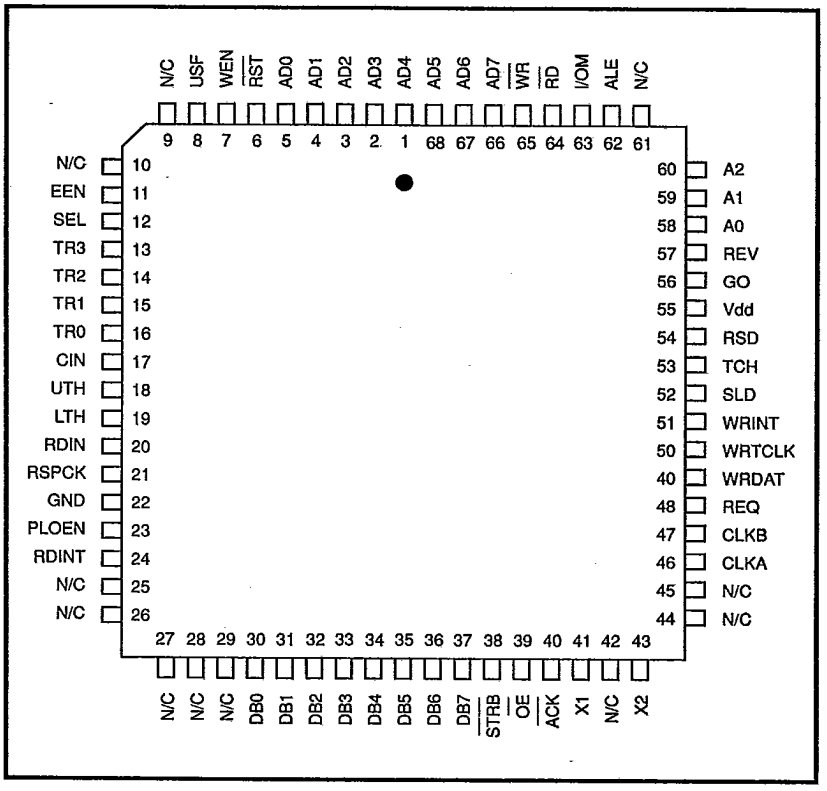

FIGURE 2. 68-PIN PLCC - SIGNAL/PIN ASSIGNMENT

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PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
1-5 66-68	AD4-0 AD5-7	I/O	Microprocessor data bus. Data may be multiplexed with address or sent separately.
6	$\overline{RST}$	I	Reset. Activation causes all output ports to reset and stops read and write sequencers. It does not reset the block register or TCHD flip-flop.
7	WEN	O	Write Enable. Controls the tape drive write enable.
8	USF	I	Unsafe. Input bit from tape drive which indicates that a cartridge is write protected.
9, 10			NOT USED
11	EEN	O	Erase Enable. Controls the tape drive erase enable.
12	SEL/TR4	O	Drive Select/Track Select. Selects the tape drive or may be used as a fifth track select bit.
13-16	TR3-TR0	O	Track Select. Selects tape drive tracks.
17	CIN	I	Cartridge In. Input bit indicates that cartridge is in place.
18	UTH	I	Upper Tape Hole. Input bit indicates detection of upper tape hole.
19	LTH	I	Lower Tape Hole. Input bit indicates detection of lower tape hole.
20	RDIN	I	Read Data In. NRZ data input from tape phase-locked loop. Must be clocked by RSPCK.
21	RSPCK	I	Read Sequencer Processing Clock. Derived from reading the Phase Locked Loop (PLL).
22	VSS	I	Ground.
23	PLOEN	O	Phase Locked Loop Enable. Controls whether the PLL is free-running or locked.
24	RDINT	O	Read Channel Interrupt. Sets at the end of every read sequence. Clears when the microprocessor resets the read sequencer.
25-29			NOT USED
30-37	DB0-DB7	I/O	Bidirectional Tape Data Bus. Supplies the read and write sequencers with an 8-bit data path.
38	$\overline{STRB}$	I	Tape Data Bus Strobe. In asynchronous mode, $\overline{STRB}$ causes data to be loaded into the write sequencer buffer.

TABLE 1. PIN DESCRIPTION

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PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
39	$\overline{OE}$	I	Tape Data Bus Output Enable. In asynchronous mode, $\overline{OE}$ causes data from the read sequencer to be output to the DB bus.
40	$\overline{ACK}$	I	Tape Data Bus Acknowledge. In asynchronous mode, $\overline{ACK}$ qualifies both $\overline{STRB}$ and $\overline{OE}$ and resets REQ.
41	X1	O	Crystal Driver Output. Output from crystal driver oscillator.
42			NOT USED
43	X2	I	Crystal Driver Input.
44, 45			NOT USED
46	CLKA	O	Clock A. Derived from the crystal oscillator and used for synchronous bus transfers. Always present.
47	CLKB	O	Clock B. Synchronous with Clock A. Indicates a bus transfer will take place.
48	REQ	O	Tape Data Bus Request. Indicates when the ADS-4360A has data or needs data for its sequencers. Only valid in asynchronous mode.
49	WRDAT	O	Write Data. This serial NRZ GCR encoded output is synchronous with WRTCLK.
50	WRTCLK	O	Write Clock. Used to clock serial write data out of the Write Sequencer.
51	WRINT	O	Write Interrupt. Sets at the end of each write data block. Automatically resets at the end of a recorded block.
52	SLD	I	Selected Drive. Microprocessor input indicating tape drive has been selected.
53	TCH	I	Tachometer. Microprocessor input used to sample tape drive speed.
54	RSD	O	Reset Tape Drive. Microprocessor output used to reset tape drive.
55	VDD	I	+5 Volts
56	GO	O	Tape Motor Go. Controls tape drive motor
57	REV	O	Tape Motor Reverse. Controls the direction of the tape drive motor.

TABLE 1. PIN DESCRIPTION Cont.

PIN NUMBER	MNEMONIC	I/O	DESCRIPTION
58-60	A0-A2	I	Micro Address Lines. When not using a multiplexed micro bus, these lines address ADS-4360A registers.
62	ALE	I	Address Latch Enable. When using a multiplexed micro bus, causes the address to be latched into the ADS-4360A.
63	I/OM (CS)	I	Chip Select. Enables the ADS-4360A bus logic.
64	$\overline{RD}$	I	Micro Bus Read. When active, allows data from the ADS-4360A onto the AD bus.
65	$\overline{WR}$	O	Micro Bus Write. When active, allows data on the AD bus to be written into the ADS-4360A.

TABLE 1. PIN DESCRIPTION Cont.

4.0 REGISTER DESCRIPTION

The ADS-4360A has eight registers starting at address 20H when using a multiplexed address scheme, or at 0H when using a non-multiplexed address scheme. These registers control the read and write sequencers as well as provide tape drive I/O signals.

Register 20H - Write/Read

Bit	Dir	Name	Description
0	O	TR0	Track Select 0
1	O	TR1	Track Select 1
2	O	TR2	Track Select 2
3	O	TR3	Track Select 3
4	O	SEL/TR4	Drive Select/Track Select 4
5	O	RSTD	Reset Tape Drive
6	O	WEN	Write Enable
7	O	EEN	Erase Enable

Register 21H - Write/Read

Bit	Dir	Name	Description
0	I	READ	Read Sequence Enable - When first set to "1" and then "0", causes the read sequencer to reset. Sequencer must reset for each block of data.
1	I	WRITE	Write Sequence Enable - When set to "1", enables the write sequencer so that it converts parallel data from the DB bus into the correct tape format. Does not need to reset after each block.
2	I	MARK	Write File Mark - When set to "1", causes the write sequencer to send a filemark block instead of data. Also inhibits tape data transfers. Mark bit sets/resets only when write sequencer is writing GAP.
3	I	QSEL	QIC Format Select - Selects either the QIC-11 or the QIC-24 tape format. (QSEL = 0 selects QIC-11) QSEL should be set only when READ and WRITE are reset.
4	I	RDEN	Read Enable - Enables data from the read sequencer for transfer over the tape data bus. RDEN should be set prior to asserting READ and while reading data from the tape, but reset when writing data. Setting RDEN when WRITE is "1" will cause unpredictable results.
5	I	CMP	Compare Enable - Enables the data compare logic. Allows data to be read into the ADS-4360A while comparing it to data off the tape. CMP should set prior to enabling READ and must not set when WRITE or RDEN are set.
6	O	GO	Tape Motor Enable
7	O	REV	Motor Direction

Register 22H - Read

Bit	Dir	Name	Description
0	O	LTH	Lower Tape Hole
1	O	UTH	Upper Tape Hole
2	O	USF	Write Protect
3	O	CIN	Cartridge In
4	O	SLD	Drive Selected
5	O	TCH	Raw Tachometer
6	I	TCHD	Tachometer Delayed
7			Not Used

Register 23H - Read

Bit	Dir	Name	Description
0-2	I	RS0-2	Read Sequencer State Bits 0-2. These bits allow the microprocessor to determine the state of the read sequencer. Read and compare samples twice to eliminate false values.
3	I	CRCER	Read CRC Error - Output from read channel sequencer. When CRCER = 0, read data is valid if it occurs at read states 4 and 5.
4	I/O	RDINT	Read Interrupt - Sets at read states 5,6 and 7 and resets when READ = 0.
5	I/O	WRINT	Write Interrupt - Sets when write sequencer begins outputting the contents of the block register and CRC value. Automatically resets at the end of a block.
6	I	CMPER	Compare Error - Sets when data read from tape does not compare with data entering ADS-4360A.
7	I	SYCER	Sync Error - Sets only in asynchronous mode if the external buffer manager does not respond to a REQ. SYCER is valid only when MODE=1. It resets when READ=WRITE=0.

Registers 24H through 27H - Write/Read

Addr	Dir	Description
24H	I/O	Block Register 0
25H	I/O	Block Register 1
26H	I/O	Block Register 2
27H	I/O	Block Register 3

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The ADS-4360A also has two small registers:

1. The Reset TCHD Flip-Flop - used for tachometer time measurements.
2. The mode select register

Bit	Name	Description
0	FSEL	Crystal Divider Select
1	MODE	Tape Data Mode
2	TEST	Test Mode

Figure 3 illustrates a typical application for the ADS-4360A.

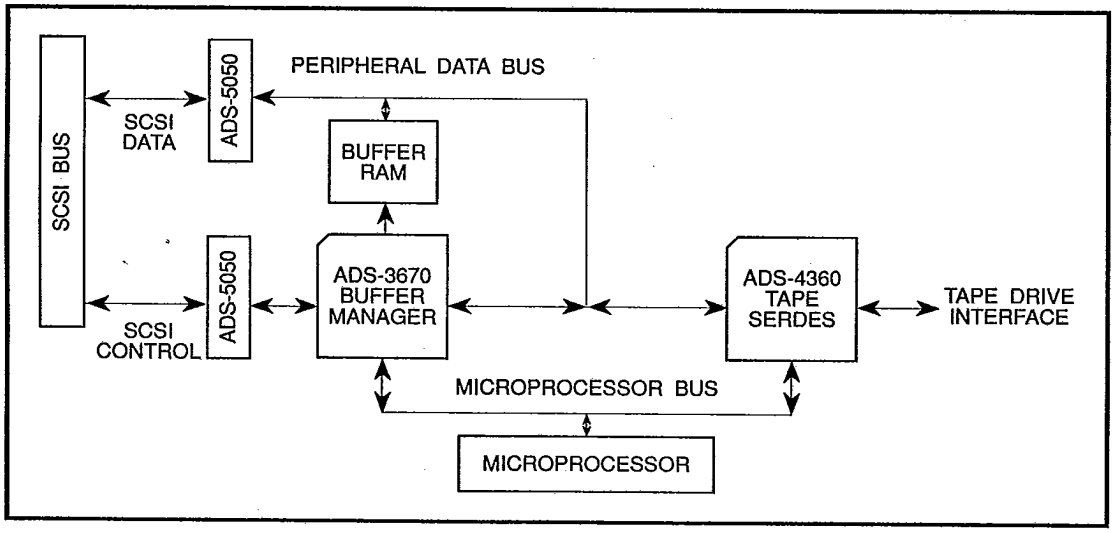

FIGURE 3. ADS-4360A TYPICAL APPLICATION

5.0 DC SPECIFICATIONS

	MIN	TYP	MAX	UNITS
Storage Temperature	-65		150	Degrees C
Voltage on any pin with respect to VSS	-0.5		7.0	Volts

TABLE 2. NON-OPERATIONAL SPECIFICATIONS

	MIN	TYP	MAX	UNITS
Ambient Air Temperature	0	25	70	Degrees C
VDD Supply Voltage with respect to VSS	4.75	5.0	5.3	Volts
ICC Supply Current			175	Milliamps
Power Dissipation			875	Milliwatts
Leakage Current on input pins			±10	Microamps
Input Voltages				
Logic 0	-0.5	0.2	0.8	Volts
Logic 1	2.0	5.0	5.5	Volts
Output Voltages				
Logic 0 (IOL = 2 mA)			0.45	Volts
Logic 1 (IOL = 400 µA)	2.4			Volts
Input Capacitances			10	Picofarads
Output Capacitance Loading				
All outputs except AD0-AD7 and DB0-DB7			20	Picofarads
Outputs AD0-AD7 and DB0-DB7			110	Picofarads

Electrostatic Discharge Protection:
All inputs are protected against electrostatic discharge voltages up to 1000 volts.

Humidity:
The ADS-4360A operates at 20% to 95% humidity (non-condensing).

TABLE 3. OPERATIONAL SPECIFICATIONS

6.0 AC TIMING SPECIFICATIONS

Timing relationships assume the maximum capacitive loading for both inputs and outputs of VDD = 4.75 volts to 5.3 volts.

Temperature = 0 to 70 degrees C.

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Timing voltage levels = .8 volts low, 2.0 volts high.

Clock inputs X1 and X2:
Maximum Crystal Frequency 6 MHz = FREQ (TCF=1/FREQ)
Minimum Crystal Frequency 0 MHz = FREQ

Non-crystal driven maximum frequency 6 MHz (TCF=1/FREQ)
Non-crystal driven minimum frequency 6 MHz (TCF=1/FREQ)
(Assuming active driver on the X2 input with 40 to 50% duty cycle and leakage not to exceed 400 μA)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t1	ALE width	60		nsec
t2	Address hold time	34		nsec
t3	ALE to valid address	50		nsec
t4	$\overline{RD}$ pulse width	200		nsec
t5	$\overline{RD}$ to data valid		150	nsec
t6	$\overline{RD}$ data hold time	10		nsec
t7	$\overline{WR}$ pulse width	210		nsec
t8	$\overline{WR}$ to data available	170		nsec
t9	$\overline{WR}$ data hold time	38		nsec
t10	CLKB active delay		70	nsec
t11	CLKB inactive delay		70	nsec
t12**	Data valid to $\overline{CLK}$		50	nsec
t13	$\overline{CLK}$ to data hold time		30	nsec
t14**	Write setup time to $\overline{CLK}$	70		nsec
t15	Write hold time after $\overline{CLK}$	0		nsec
t16**	$\overline{OE}$ to data valid		70	nsec
t17	$\overline{OE}$ inactive hold time	10		nsec
t18	Data valid to $\overline{STRB}$ inactive	40		nsec
t19**	Data hold time after $\overline{STRB}$	10		nsec
t20**	WRDAT valid		70	nsec

TABLE 4. TIMING

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t21**	Not defined			T-52-33-15
t22	I/OM to $\overline{WR}$ or $\overline{RD}$ setup	100		nsec
t23	$\overline{RD}$ or $\overline{WR}$ to I/OM hold	20		nsec
t24**	RDIN setup	50		nsec
t25**	RDIN hold	10		nsec
t26	RSPCK clock period This specification has several values depending upon the mode. The mode is determined by PLOEN.			
	MODE 0 (PLOEN=0)			
t26	RSPCK clock period	275	DC	nsec
t26a	RSPCK clock high phase	137	DC	nsec
	MODE 1 (PLOEN=1)			
	RSPCK clock period	1.5 TCF	2.5 TCF	
t27	$\overline{WR}$ inactive to TAPE I/O OUTPUT valid Note: TAPE I/O OUTPUTS should remain "glitchless" if a new value is written into the latch.		70	nsec
t28	TAPE I/O INPUTS to $\overline{RD}$	50		nsec
t29	RSPCK to PLOEN and RDINT		50	nsec
t30	$\overline{RST}$ pulse width	100		nsec
t31	$\overline{RST}$ inactive to TAPE I/O Interface outputs stable		120	nsec
t32	$\overline{ACK}$ to REQ false		50	nsec
t33	$\overline{ACK}$ active to $\overline{OE}$ active	0		nsec
t34	$\overline{OE}$ inactive to $\overline{ACK}$ inactive	0		nsec
t35	$\overline{ACK}$ active to $\overline{STRB}$ active	0		nsec
t36	$\overline{STRB}$ inactive to $\overline{ACK}$ inactive	0		nsec
t37	$\overline{CLK}$ High	.9 TCF	1.1 TCF	nsec
t38	$\overline{CLK}$ Low	.9 TCF	1.1 TCF	nsec
t39	WRCLK High	1.8 TCF	2.2 TCF	nsec
t40	WRCLK Low	1.8 TCF	2.2 TCF	nsec

Note: ** = Critical timing parameter TCF = 1/(Crystal FREQ)

TABLE 4. TIMING Cont.

Figures 4 through 13 illustrate the various timing relationships that exist for the ADS-4360A.

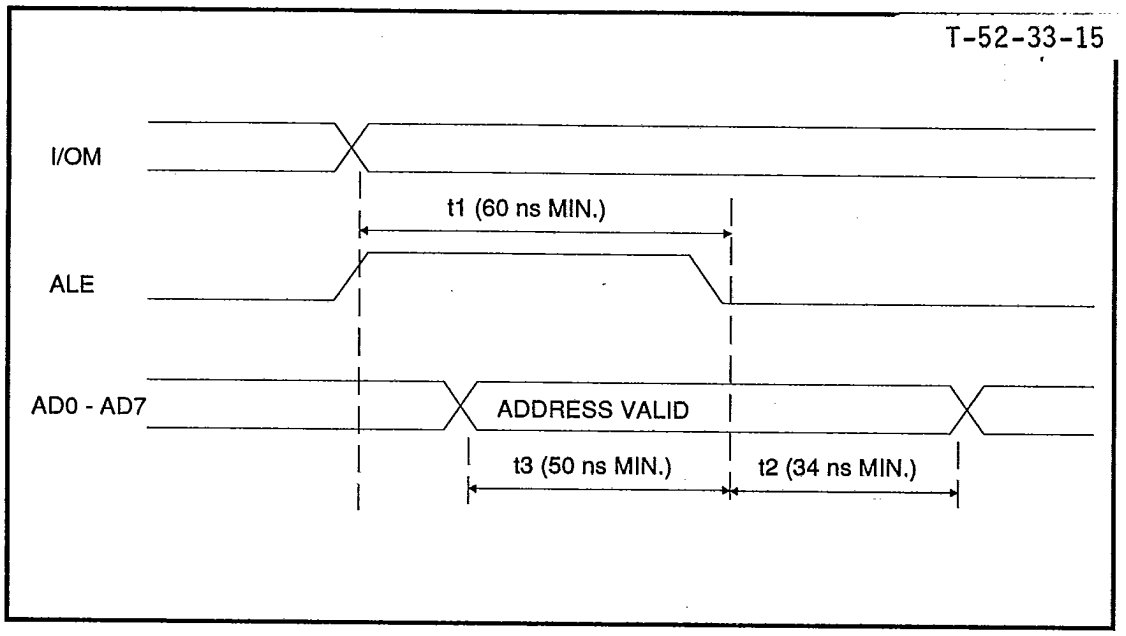


FIGURE 4. MICROPROCESSOR ALE TIMING

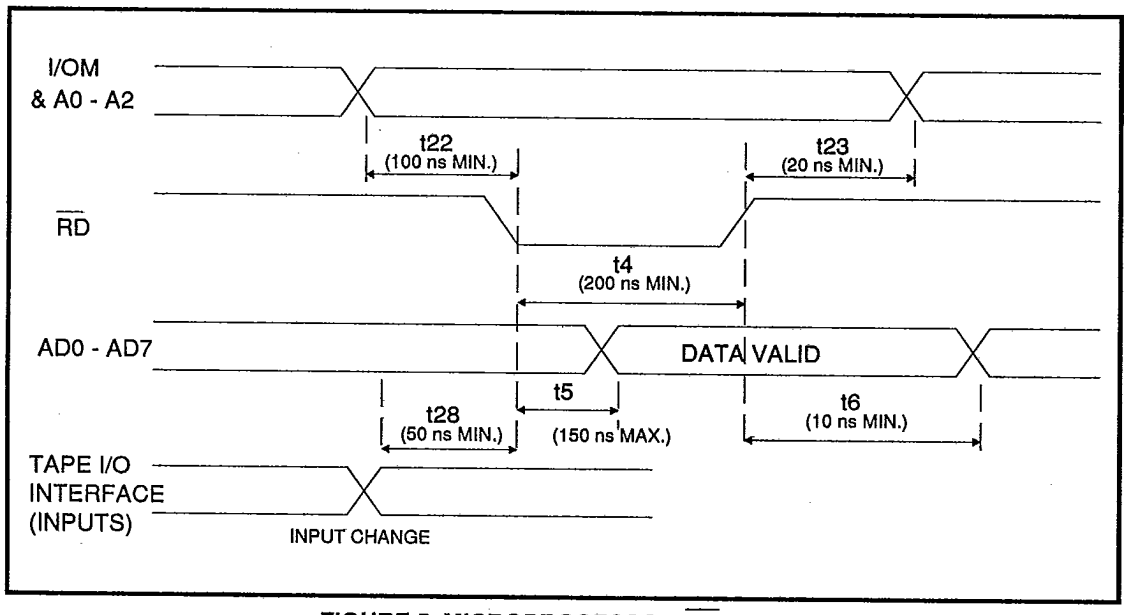


FIGURE 5. MICROPROCESSOR $\overline{RD}$ TIMING

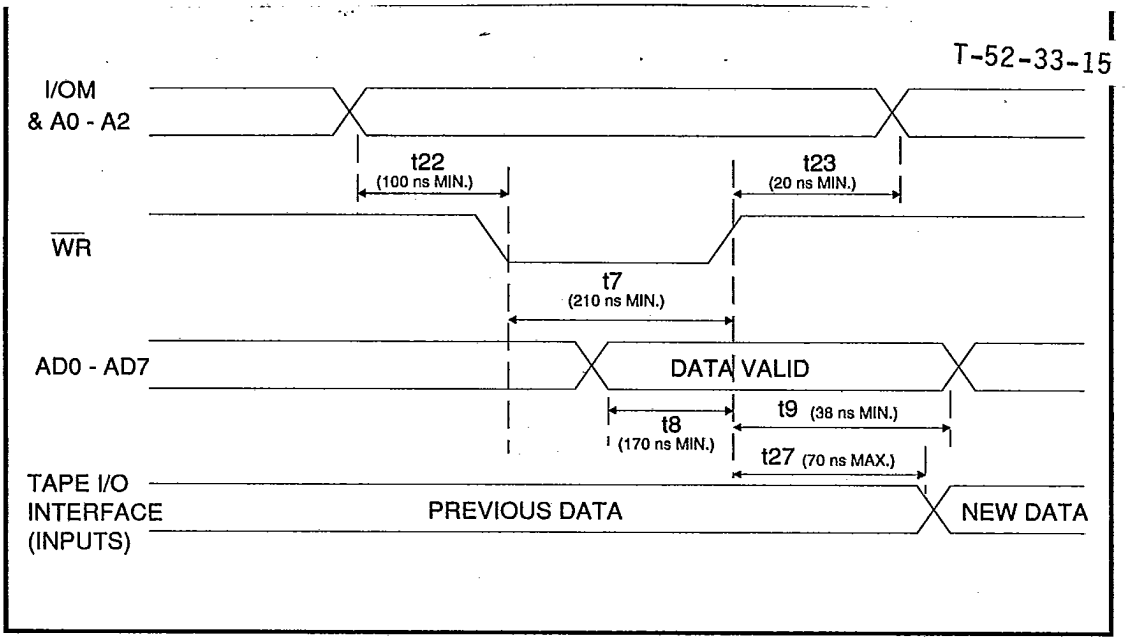
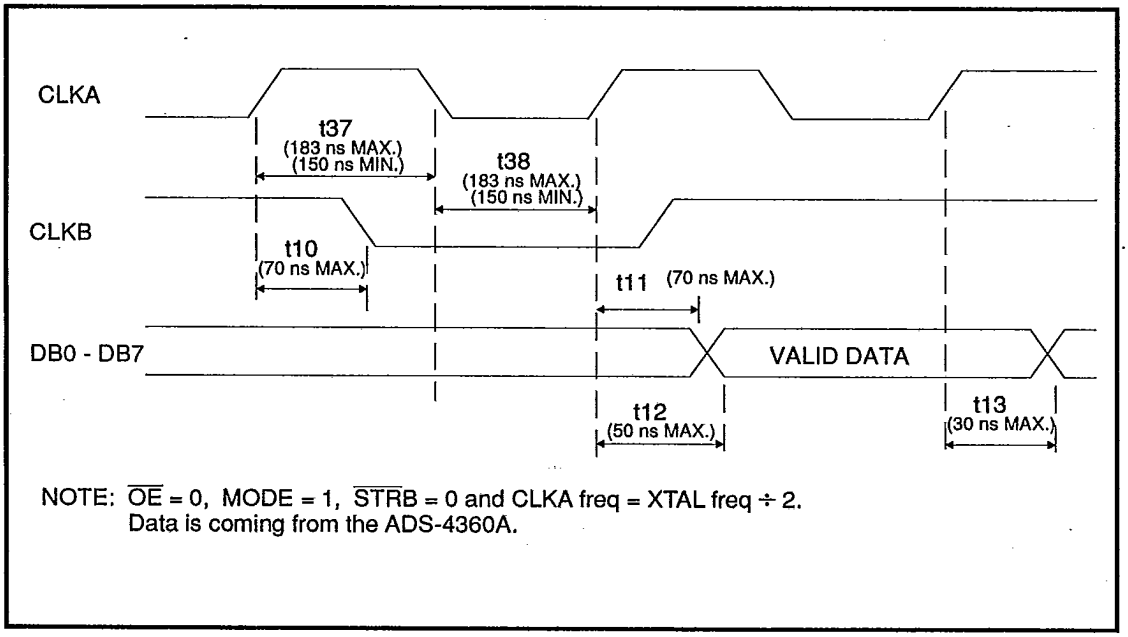
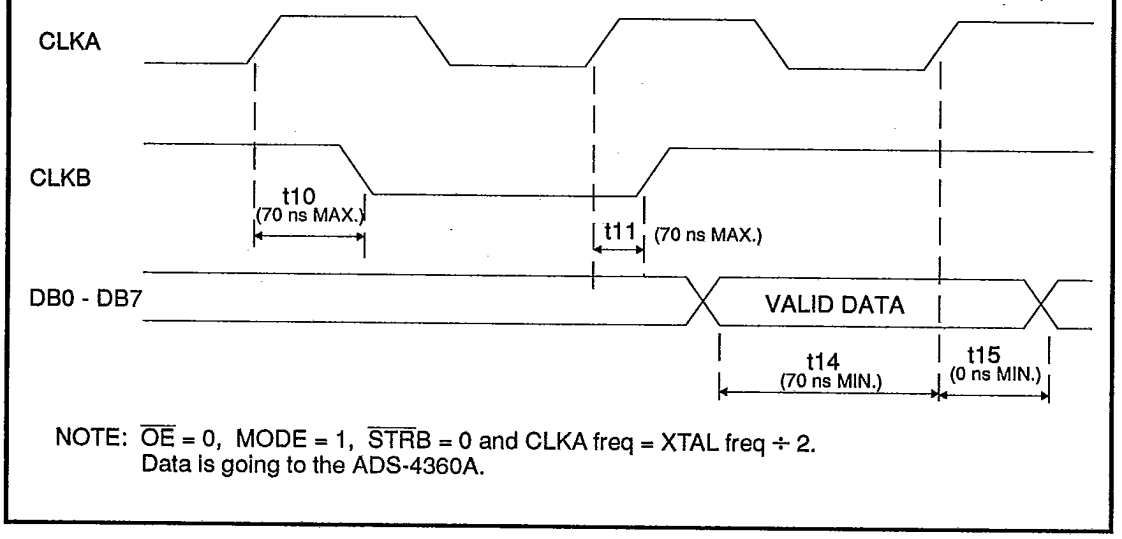


FIGURE 6. MICROPROCESSOR $\overline{WR}$ TIMING



NOTE: $\overline{OE}$ = 0, MODE = 1, $\overline{STRB}$ = 0 and CLKA freq = XTAL freq ÷ 2.
Data is coming from the ADS-4360A.

FIGURE 7. SYNCHRONOUS MODE DATA BUS READ TIMING



NOTE: $\overline{OE}$ = 0, MODE = 1, $\overline{STRB}$ = 0 and CLKA freq = XTAL freq ÷ 2.
Data is going to the ADS-4360A.

FIGURE 8. SYNCHRONOUS MODE DATA BUS WRITE TIMING

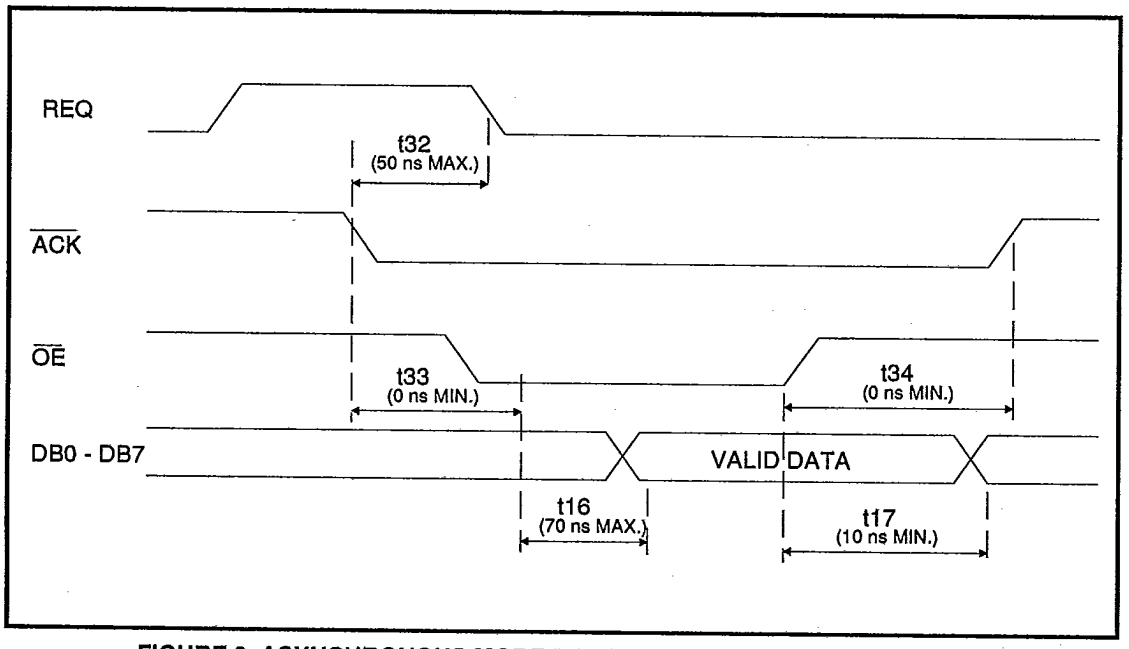


FIGURE 9. ASYNCHRONOUS MODE DATA BUS READ TIMING (DATA OUT)

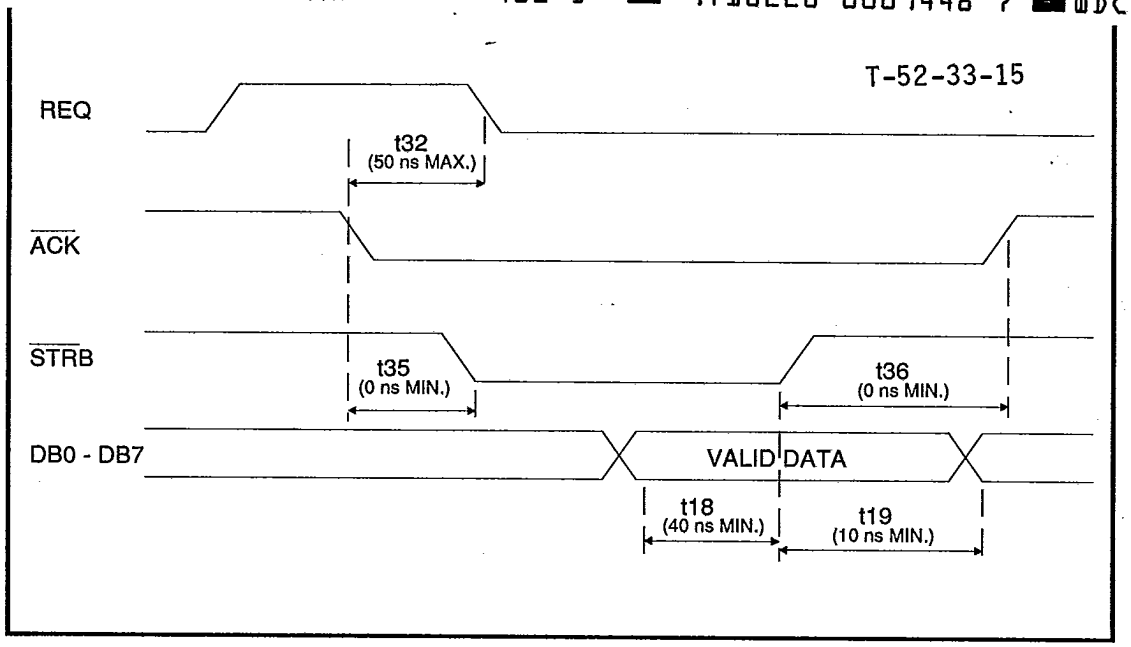


FIGURE 10. ASYNCHRONOUS MODE DATA BUS WRITE TIMING (DATA IN)

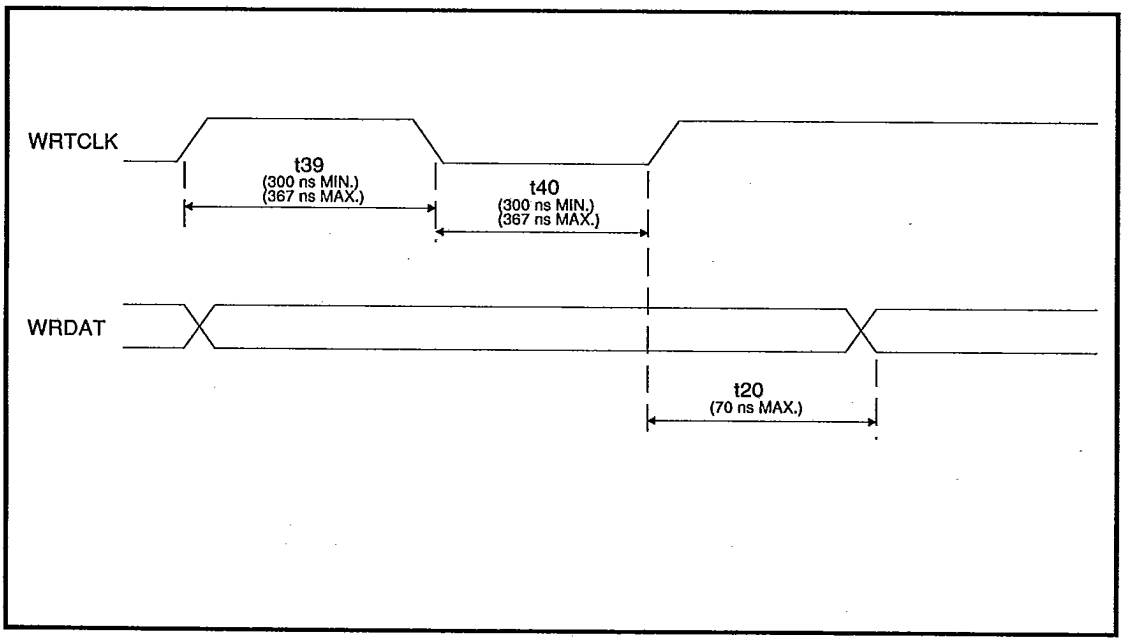


FIGURE 11. WRITE SERIALIZER OUTPUT TIMING

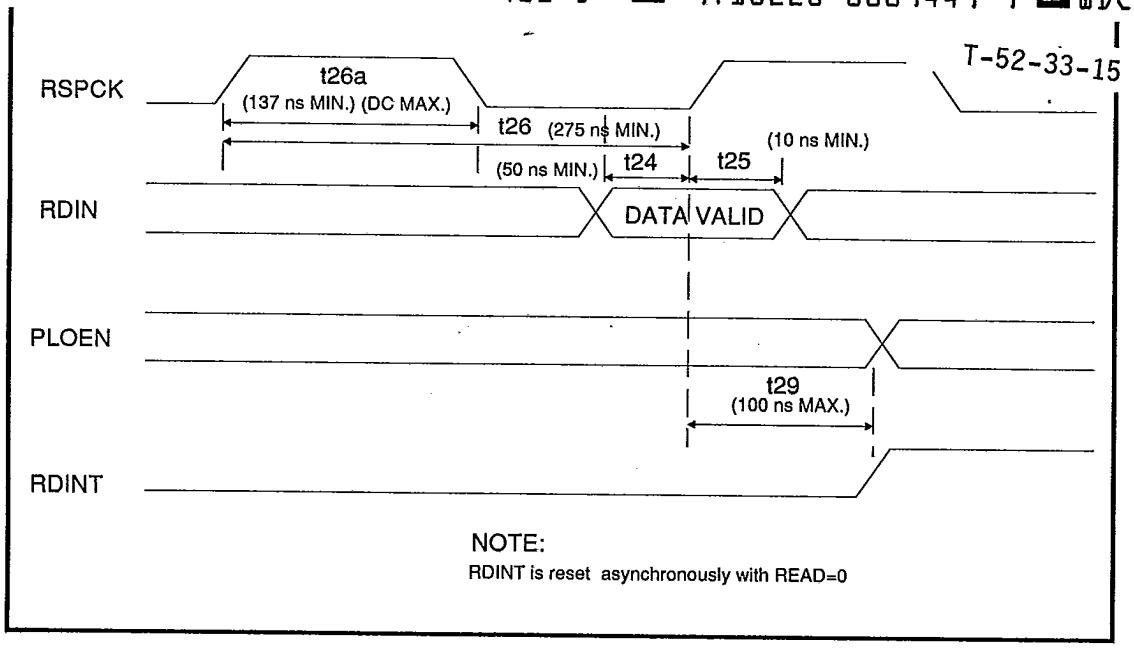


FIGURE 12. SERIAL DATA IN TIMING

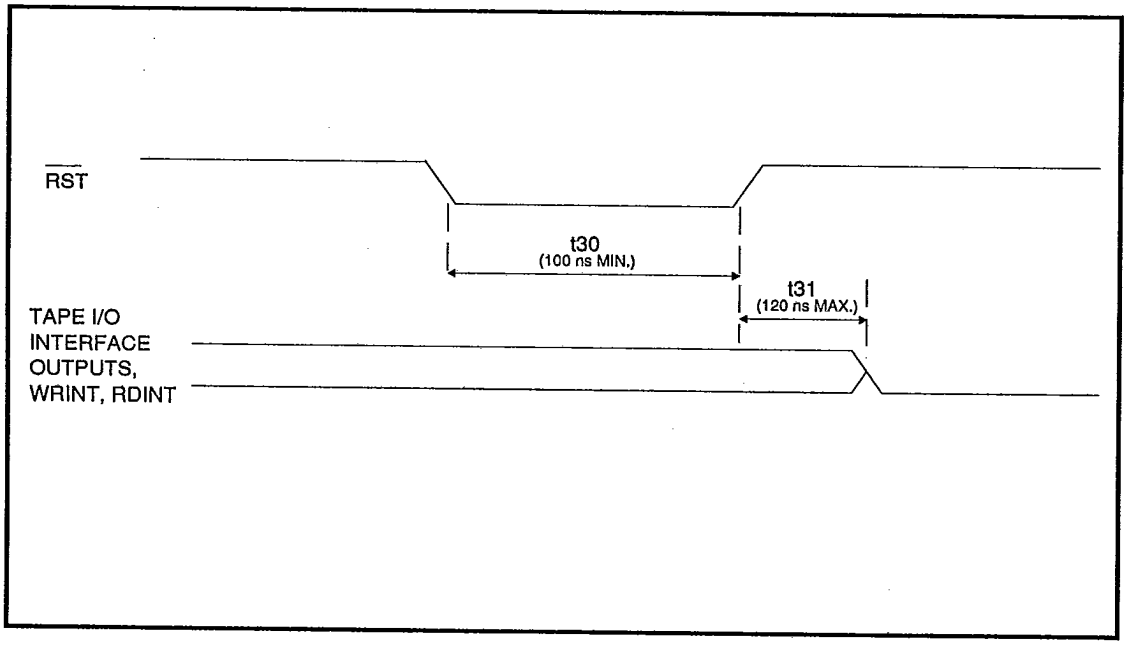


FIGURE 13. RESET TIMING