

**XPAK
850 nm Module
10 Gigabit Pluggable Transceiver
Compatible with XPAK MSA Rev. 2.3**

**V23833-G2005-A101
V23833-G6005-A101**

Preliminary Data Sheet

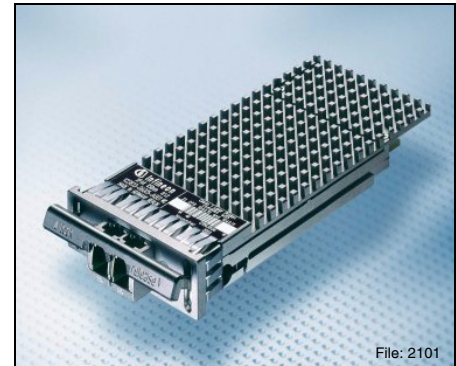
Features

Standards

- Compatible with IEEE 802.3ae™-2002
- Compatible with Fibre Channel 10GFC Draft 3.5
- Compatible with XPAK MSA Rev. 2.3

Optical

- IEEE Ethernet: Serial 850 nm 10GBASE-SR
- T11 Fibre Channel: Serial 850 nm 1200-M5-SN-I; 1200-M5E-SN-I; 1200-M6-SN-I
- 10 Gigabit Fibre Channel: 10.51875 Gbit/s (V23833-G2005-A101)
- 10 Gigabit Ethernet: 10.3125 Gbit/s (V23833-G6005-A101)
- Transmission distance
 - up to 82 m¹⁾ (50 µm MMF)
 - up to 300 m¹⁾ (on special MMF)
- Vertical Cavity Surface Emitting Laser at 850 nm (VCSEL)
- LC connector, multimode fiber (alternate product available with SC connector for single mode fiber applications)
- Full duplex transmission mode



File: 2101

¹⁾ Maximum reach as defined by IEEE. Longer reach possible depending upon link implementation.

Ordering Information

Part Number	Standard	Height	Connector	Laser Class
V23833-G2005-A101	Fibre Channel	Mezzanine	LC	1M
V23833-G6005-A101	Ethernet	Mezzanine	LC	1M

- DOM
 - Loss Of Signal from receiver
 - Laser safety alarm (with reset function)
 - Supply voltage monitor
 - Transmit power
 - Module temperature
 - Received power
 - Transmit bias current monitor

Mechanical

- Mezzanine profile: 2.68" L x 1.42" W x 0.38" H (68.07 mm x 35.99 mm x 9.8 mm)
- Mezzanine module height for PCI card applications mid-board mounting
- Belly-to-belly applications
- De-latch mechanism with low extraction force
- Built-in heat sink

Electrical

- Hot pluggable
- Power supply: +5.0 V, +3.3 V, Adaptable Power Supply (APS: +1.8 V)
- Total power consumption: 3.3 W typical
- XAUI electrical interface
- 10.3125 Gbit/s Ethernet serial data rate (V23833-G60xx-xxxx)
- 10.51875 Gbit/s Fibre Channel serial data rate (V23833-G20xx-xxxx)
- Management and control via MDIO 2-wire bus
- 70-pin connector

Applications

- 10 Gbit/s Ethernet and Fibre Channel transmission systems for Short Range (SR)
- Integration on PCI card
- Mid-board mounting
- Belly-to-belly for high density applications
- Enterprise and campus network applications
- Storage applications
- Backplane and switch applications
- Core and edge routers
- Aggregation point for lower data rate
- XPAK evaluation kit V23833-G9909-Z001 available upon request

Pin Configuration

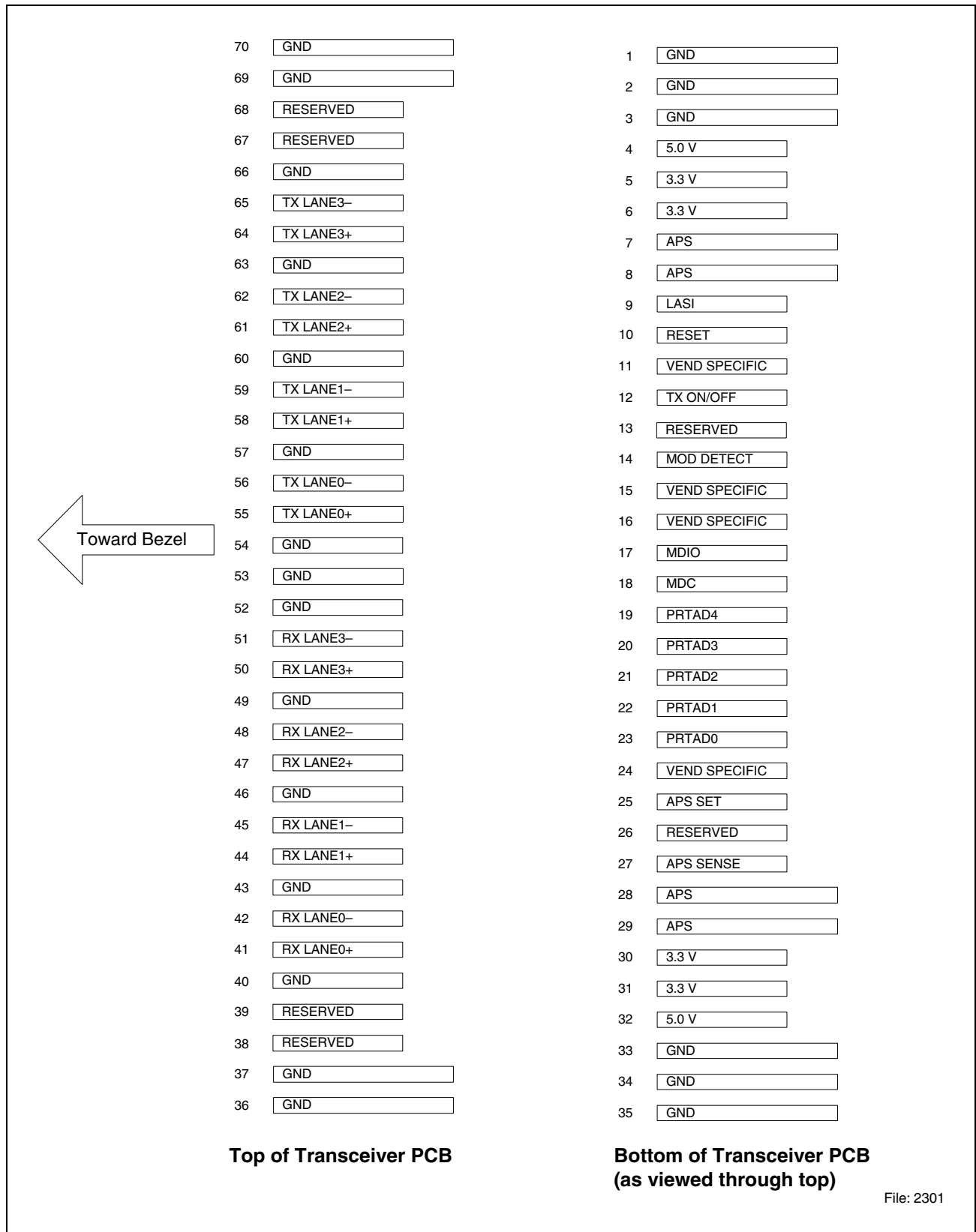


Figure 1 XPAK Transceiver Electrical Pad Layout

Pin Configuration

Connector Pin Assignments

Pin No.	Signal Name
1	GND
2	GND
3	GND
4	+5.0 V DC Power
5	+3.3 V DC Power
6	+3.3 V DC Power
7	APS
8	APS
9	LASI
10	RESET
11	Vendor Specific
12	TX ON/OFF
13	Reserved
14	MOD DETECT
15	Vendor Specific
16	Vendor Specific
17	MDIO
18	MDC
19	PRTAD4
20	PRTAD3
21	PRTAD2
22	PRTAD1
23	PRTAD0
24	Vendor Specific
25	APS SET
26	Reserved
27	APS SENSE
28	APS
29	APS
30	+3.3 V DC Power
31	+3.3 V DC Power
32	+5.0 V DC Power
33	GND
34	GND
35	GND

Pin No.	Signal Name
70	GND
69	GND
68	Reserved
67	Reserved
66	GND
65	TX LANE3-
64	TX LANE3+
63	GND
62	TX LANE2-
61	TX LANE2+
60	GND
59	TX LANE1-
58	TX LANE1+
57	GND
56	TX LANE0-
55	TX LANE0+
54	GND
53	GND
52	GND
51	RX LANE3-
50	RX LANE3+
49	GND
48	RX LANE2-
47	RX LANE2+
46	GND
45	RX LANE1-
44	RX LANE1+
43	GND
42	RX LANE0-
41	RX LANE0+
40	GND
39	Reserved
38	Reserved
37	GND
36	GND

Pin Configuration
Pin Description

Signal Name	Level	I/O	Pin No.	Description
Management and Monitoring Ports				
MDIO	Open Drain	I/O	17	Management Data I/O. Requires external 10 - 22 k Ω pull-up to 1.8 V on host.
MDC	1.2 V CMOS	I	18	Management Data Clock Input
PRTAD4	1.2 V CMOS	I	19	Port Address Input bit 4
PRTAD3	1.2 V CMOS	I	20	Port Address Input bit 3
PRTAD2	1.2 V CMOS	I	21	Port Address Input bit 2
PRTAD1	1.2 V CMOS	I	22	Port Address Input bit 1
PRTAD0	1.2 V CMOS	I	23	Port Address Input bit 0
LASI	Open Drain	O	9	Link Alarm Status Interrupt Output. Open Drain Compatible Output with 10 - 20 k Ω pull-up on host. Logic high = Normal Operation Logic low = Status Flag Triggered
RESET	Open Drain	I	10	Reset Input. Open Drain Compatible Input with 10 k Ω pull-up to APS internal to transceiver. Logic high = Normal Operation Logic low = RESET Note: 1.8 V is APS
Vendor Specific			11,15,16,24	Vendor Specific Pins. Leave unconnected when not used.
TX ON/OFF	Open Drain	I	12	TX ON/OFF Input. Open Drain Compatible Input with 10 k Ω pull-up to APS internal to transceiver. Logic high = Transmitter On Logic low = Transmitter Off Note: 1.8 V is APS
MOD DETECT		O	14	Pulled low inside transceiver through a 1 k Ω resistor to Ground

Pin Configuration
Pin Description (cont'd)

Signal Name	Level	I/O	Pin No.	Description
Transmit Functions				
Reserved		I	68	Reserved For Future Use
Reserved		I	67	Reserved For Future Use
TX LANE 3–	AC-coupled, Internally biased differential XAUI	I	65	Module XAUI Input Lane 3–
TX LANE 3+		I	64	Module XAUI Input Lane 3+
TX LANE 2–		I	62	Module XAUI Input Lane 2–
TX LANE 2+		I	61	Module XAUI Input Lane 2+
TX LANE 1–		I	59	Module XAUI Input Lane 1–
TX LANE 1+		I	58	Module XAUI Input Lane 1+
TX LANE 0–		I	56	Module XAUI Input Lane 0–
TX LANE 0+		I	55	Module XAUI Input Lane 0+
Receive Functions				
Reserved		O	38	Reserved For Future Use
Reserved		O	39	Reserved For Future Use
RX LANE 0+	AC-coupled, Internally biased differential XAUI	O	41	Module XAUI Output Lane 0+
RX LANE 0–		O	42	Module XAUI Output Lane 0–
RX LANE 1+		O	44	Module XAUI Output Lane 1+
RX LANE 1–		O	45	Module XAUI Output Lane 1–
RX LANE 2+		O	47	Module XAUI Output Lane 2+
RX LANE 2–		O	48	Module XAUI Output Lane 2–
RX LANE 3+		O	50	Module XAUI Output Lane 3+
RX LANE 3–		O	51	Module XAUI Output Lane 3–

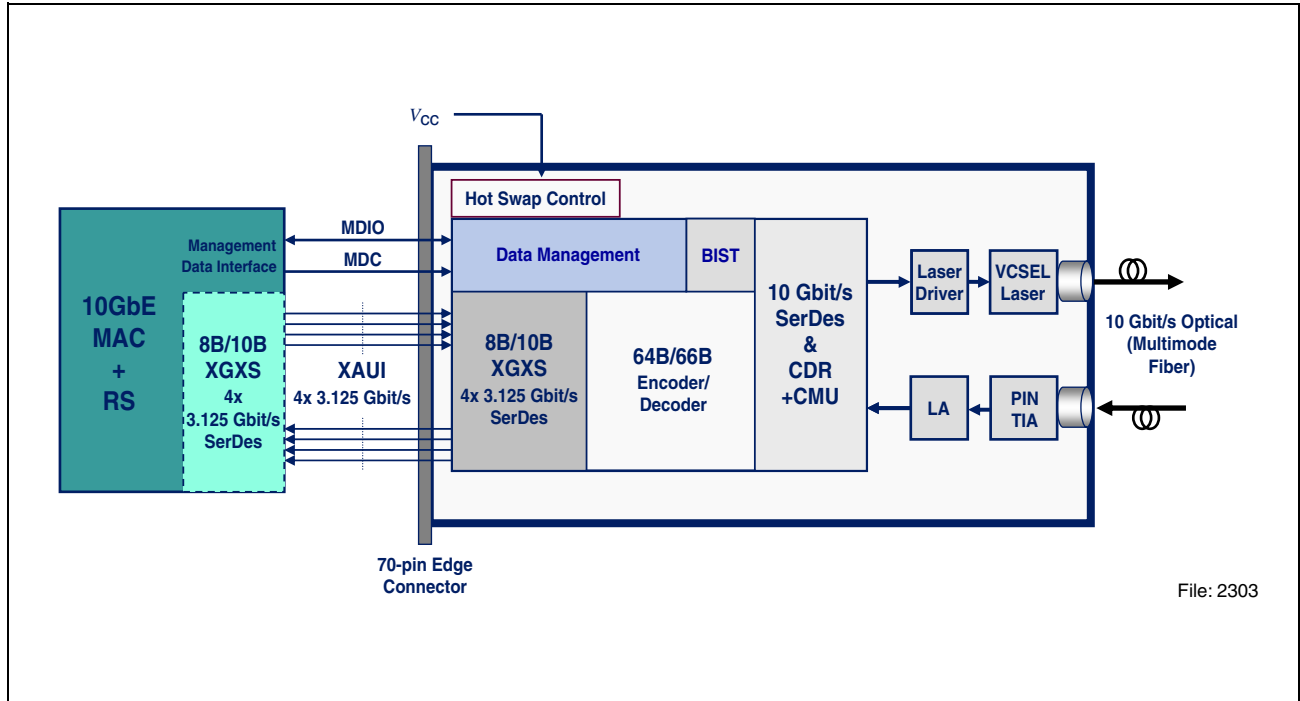
Pin Configuration

Pin Description (cont'd)

Signal Name	Level	I/O	Pin No.	Description
DC Power				
GND	0 V DC	I	1,2,3,33,34, 35,36,37,40, 43,46,49,52, 53,54,57,60, 63,66,69,70	Ground connection for signal ground on the module
APS	+1.8 V	I	7,8,28,29	Input from Adaptive Power Supply
APS SENSE	+1.8 V	O	27	APS Sense Output. Connected to the APS input inside transceiver.
APS SET	GND	I	25	Feedback input from APS. Connected to GND through a zero Ω resistor inside the transceiver.
3.3 V	+3.3 V DC	I	5,6,30,31	DC Power Input, +3.3 V DC, Nominal
5.0 V	+5.0 V DC	I	4,32	DC Power Input, +5.0 V DC, Nominal
Reserved			26	Reserved for APD. Do not connect.
Reserved			13	Reserved. Do not connect.

Description

System Block Diagram (10 Gbit/s Ethernet)



File: 2303

Figure 2

Optical Interface Standard Specifications

- IEEE 802.3ae™-2002 clause 52, 10GBASE-SR
- Fibre Channel 10GFC Draft 3.5, 1200-M5-SN-I
- Fibre Channel 10GFC Draft 3.5, 1200-M5E-SN-I
- Fibre Channel 10GFC Draft 3.5, 1200-M6-SN-I
- XPAK MSA 2.3

Standard	Fiber Type	Minimum Modal Bandwidth at 850 nm (MHz*km)	Operating Range ¹⁾ (meters)
IEEE	62.5 µm MMF	160	2 to 26
	50 µm MMF	400	2 to 66
Fibre Channel	62.5 µm MMF	200	0.5 to 33
	50 µm MMF	500	0.5 to 82
	50 µm MMF	2000	0.5 to 300

¹⁾ Longer reaches possible depending upon link implementation.

Electrical Interface Standard Specifications

- IEEE 802.3ae™-2002 clause 45 & 47
- XPAK MSA 2.3

Environment: Thermal Management Recommendations

Operating air inlet temperature:	0°C - 50°C
Operating Airflow:	3 m/s maximum defined per XPAK MSA
Operating Humidity:	0% - 95% RH non-condensing

Module can withstand and operate with case temperature of 75°C for up to 96 hrs/yr. Transceiver requires airflow across cooling fins. Maximum airflow required per XPAK MSA is 3 m/s. Actual airflow required to provide adequate cooling for Infineon transceiver TBD.

Fibers and Connectors

The transceiver has LC or SC receptacles for both Tx and Rx distinguished by part number. The transceiver is designed for multimode LC or SC cables, 0° polished endface (PC).

70-pin Connector

The module interface connector is a 70-pin, printed circuit board edge connection with a 0.5 mm pitch. The appropriate mating connector for the customer PCB is a 70-pin SMT, dual row, right angled, edge connector, 0.5 mm pitch (TycoAmp part number 1367337-1, Molex part number 74441-0003 or equivalent).

Cage Requirement

The cage assembly required to mount the XPAK module is defined by the MSA. There are two cage designs for the module, tall and mezzanine profile. For correct operation and EMI design the correct cage size must be selected for the appropriate module. Alternatively a flangeless cage design is specified where there is limited size.

Description

DOM Parameters

Parameter	Values			Unit
	min.	typ.	max.	
Transceiver Temperature Monitor Accuracy ¹⁾			±5	°C
Transmit Bias Current Monitor Accuracy ²⁾			±10	%
Transmit Power Monitor Accuracy ³⁾			±3	dB
Receive Power Monitor Accuracy ³⁾			±3	dB

¹⁾ 0 to 70°C case temperature.

²⁾ 0 to 12.5 mA.

³⁾ 0 to 6.5 mW.

Regulatory Compliance

Feature	Standard	Comments
ESD: Electrostatic Discharge to the Electrical Pins (HBM)	EIA/JESD22-A114-B (MIL-STD 883D Method 3015.7)	Class 1a (> 500 V)
Immunity: Against Electrostatic Discharge (ESD) to the Module Receptacle	EN 61000-4-2 IEC 61000-4-2	Discharges ranging from ±2 kV to ±15 kV to the front end / faceplate / receptacle cause no damage to module (under recommended conditions).
Immunity: Against Radio Frequency Electromagnetic Field	EN 61000-4-3 IEC 61000-4-3	With a field strength of 3 V/m, noise frequency ranges from 10 MHz to 2 GHz. No effect on module performance between the specification limits.
Emission: Electromagnetic Interference (EMI)	FCC 47 CFR Part 15, Class B EN 55022 Class B CISPR 22	Noise frequency range: 30 MHz to 40 GHz Radiated emission does not exceed specified limits when measured inside a shielding enclosure with MSA conform cutout.

Technical Data
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Storage Ambient Temperature ¹⁾	T_{As}	-20	85	°C
Operating Ambient Temperature ¹⁾	T_{Ao}	0	65	°C
Operating Case Temperature ¹⁾	T_{Co}	0	80	°C
Supply Voltage +5.0 V	V_5	0	6	V
Supply Voltage +3.3 V	V_3	0	4	V
Supply Voltage APS	V_{aps}	0	2	V
Static Discharge Voltage, All Pins	ST_d		500	V
Average Receive Optical Power	$Rx_{P_{max}}$		0	dBm

¹⁾ Non condensing.

Exceeding any one of these values may permanently destroy the device.

Recommended Operating Conditions

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Operating Case Temperature ¹⁾	T_C	0		70	°C
Transceiver Total Power Consumption	P		3.3	3.5	W
Supply Voltage +5.0 V	V_{CC5}	4.75	5.0	5.25	V
Supply Current +5.0 V	I_{CC5}		50		mA
Supply Voltage +3.3 V	V_{CC3}	3.14	3.3	3.47	V
Supply Current +3.3 V	I_{CC3}		550		mA
Supply Voltage APS	$V_{CC_{aps}}$	1.746	1.8	1.854	V
Supply Current APS	$I_{CC_{aps}}$		700		mA

¹⁾ Worst case thermal location, see **Figure 9**.

Optical Characteristics
 $(V_{CC5} = 4.75 \text{ V to } 5.25 \text{ V}, V_{CC3} = 3.14 \text{ V to } 3.47 \text{ V}, V_{CC\text{aps}} = 1.746 \text{ V to } 1.854 \text{ V}, T_C = 0^\circ\text{C to } 70^\circ\text{C})$

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Transmitter					
Launch Power in OMA ¹⁾	$P_{O\text{-OMA}}$	-2.8			dBm
Average Launch Power	$P_{O\text{-Avg}}$	-3	-2	-1	dBm
Center Wavelength Range ¹⁾	$\lambda_{C\text{-Tx}}$	840	850	860	nm
RMS Spectral Width ¹⁾	σ_I		0.4	0.45	nm
Extinction Ratio	ER	3	5.5	6.5	dB
Relative Intensity Noise ₁₂ OMA	RIN			-128	dB/Hz
Eye Mask Definition	According to IEEE and Fibre Channel				
Transmitter and Dispersion Penalty	TDP			3.9	dB
Encircled Flux	EF	at 19 $\mu\text{m} \geq 86\%$, at 4.5 $\mu\text{m} \leq 30\%$			
Optical Return Loss Tolerance	ORL _T			12	dB
Average Launch Power of OFF Transmitter	$P_{O\text{-OFF}}$			-30	dBm
Receiver					
Stressed Receiver Sensitivity in OMA	$P_{IN\text{-S}}$			-7.5	dBm
Sensitivity in OMA ²⁾	P_{IN}			-11.1	dBm
Average Receive Power	$P_{IN\text{-max}}$			-1	dBm
Signal Detect Deassert Level	P_{SDL}	-30			dBm
Signal Detect Assert Level	P_{SD}		-20	-13	dBm
Signal Detect Hysteresis	P_{SD}	1	2	4	dB
Receiver Reflectance	REF _{Rx}			-12	dB
Center Wavelength Range	$\lambda_{C\text{-Rx}}$	840		860	nm
Electrical 3 dB Upper Cut-off Frequency	3dB _{CO}			12.3	GHz

¹⁾ Conforms to IEEE triple trade off between center wavelength, RMS spectral width and minimum OMA.

²⁾ Receiver sensitivity is informative only. Measured with an ideal transmitter.

Electrical DC Characteristics

($V_{CC5} = 4.75\text{ V to }5.25\text{ V}$, $V_{CC3} = 3.14\text{ V to }3.47\text{ V}$, $V_{CCaps} = 1.746\text{ V to }1.854\text{ V}$, $T_C = 0^\circ\text{C to }70^\circ\text{C}$)

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

1.2 V CMOS (1.8 V CMOS Compatible¹⁾) I/O DC Characteristics (PRTAD; LASI; RESET; TX_ONOFF)

External Pull-up Resistor for Open Drain	R_{pullup}	10		22	k Ω
Output High Voltage ²⁾	V_{oh}	1			V
Output Low Voltage ²⁾	V_{ol}			0.15	V
Input High Voltage	V_{ih}	0.84		1.854	V
Input Low Voltage	V_{il}			0.36	V
Input Pull-down Current ³⁾	I_{pd}	20		120	μA

XAUI I/O DC Characteristics (TXLANE[0..3]; RXLANE[0..3])

Differential Input Amplitude (pk-pk) ⁴⁾	V_{in_xau}	200		2500	mV
Differential Output Amplitude (pk-pk) ⁴⁾	V_{out_xau}	800		1600	mV

MDIO I/O DC Characteristics (MDIO; MDC)

Output Low Voltage ⁵⁾	V_{OL}	-0.3		0.2	V
Output Low Current	I_{OL}			4	mA
Input High Voltage	V_{IH}	0.84		1.854	V
Input Low Voltage	V_{IL}	-0.3		0.36	V
Pull-up Supply Voltage	V_{PU}	1.746	1.8	1.854	V
Input Capacitance	C_{IN}			10	pF
Load Capacitance	C_{LOAD}			470	pF
External Pull-up Resistance	R_{LOAD}	200			Ω

¹⁾ For 1.8 V CMOS $V_{oh} = 1.65\text{ V min.}$, $V_{ol} = 0.15\text{ V max.}$, $V_{ih} = 1.17\text{ V min.}$, $V_{il} = 0.63\text{ V max.}$

²⁾ $R_{pull-up} = 10\text{ k}\Omega\text{ to }1.8\text{ V}$.

³⁾ $V_{in} = 1.8\text{ V}$.

⁴⁾ AC coupled.

⁵⁾ $I_{OL} = 100\ \mu\text{A}$.

Electrical AC Characteristics
 $(V_{CC5} = 4.75 \text{ V to } 5.25 \text{ V}, V_{CC3} = 3.14 \text{ V to } 3.47 \text{ V}, V_{CC\text{aps}} = 1.746 \text{ V to } 1.854 \text{ V}, T_C = 0^\circ\text{C to } 70^\circ\text{C})$

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

**XAUI Input AC Characteristics
(TXLANE[0..3])**

Baud Rate	R_{XAUIIN}		3.125		Gbit/s
Baud Rate Tolerance	$R_{TOLXAUI}$	-100		100	ppm
Differential Input Impedance	Z_{INXAUI}	80	100	120	Ω
Differential Return Loss ¹⁾	$ S_{11} $	10			dB
Input Differential Skew ²⁾	t_{SKEWIN}			75	ps
Jitter Amplitude Tolerance ³⁾	$J_{XAUITOL}$				

**XAUI Output AC Characteristics
(RXLANE[0..3])**

Baud Rate	R_{XAUIIN}		3.125		Gbit/s
Baud Rate Variation	$R_{XAUIVAR}$	-100		100	ppm
Rise and Fall Times 20% - 80%	t_r, t_f	40		100	ps
Output Differential Skew	$t_{SKEWOUT}$			15	ps
Output Differential Impedance	$Z_{OUTXAUI}$	80	100	120	Ω
Differential Output Return Loss ¹⁾	$ S_{22} $	10			dB
Total Jitter ⁴⁾	TJ_{XAUI}			0.35	UI
Deterministic Jitter ⁴⁾	DJ_{XAUI}			0.17	UI

Power-On Reset AC Characteristics

Power-On Reset and TX_ONOFF Characteristics	According to XENPAK MSA Issue 3.0 Draft 4.0, 2002-9-9				
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**MDIO I/O AC Characteristics
(MDIO; MDC)**

MDIO Data Hold Time	t_{HOLD}	10			ns
MDIO Data Setup Time	t_{SU}	10			ns
Delay from MDC Rising Edge to MDIO Data Change	t_{DELAY}			300	ns
MDC Clock Rate	f_{MAX}			2.5	MHz

¹⁾ 100 MHz to 2.5 GHz.

²⁾ At crossing point.

³⁾ Per IEEE 802.3ea.

⁴⁾ At near-end. No pre-equalization. 1 UI = 320 ps.

Eye Safety

This laser based multimode transceiver is a Class 1 or Class 1M product distinguished by part number (see **Ordering Information**). It complies with IEC 60825-1 and FDA 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice 50, dated July 26, 2001.

To meet laser safety requirements the transceiver shall be operated within the Absolute Maximum Ratings.

Attention: All adjustments have been made at the factory prior to shipment of the devices. No maintenance or alteration to the device is required. Tampering with or modifying the performance of the device will result in voided product warranty.

Note: Failure to adhere to the above restrictions could result in a modification that is considered an act of “manufacturing”, and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (ref. 21 CFR 1040.10 (i)).

Application Notes

PCB Cage Footprints

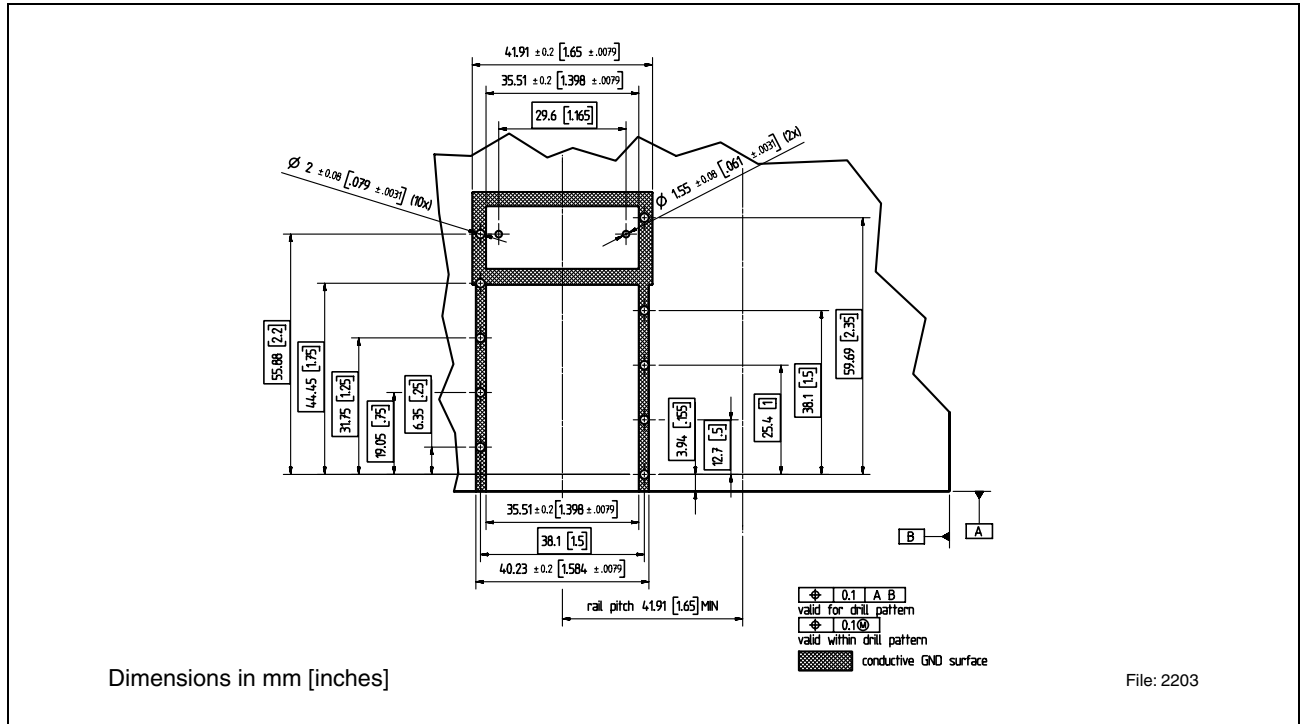


Figure 3 Standard Mounting

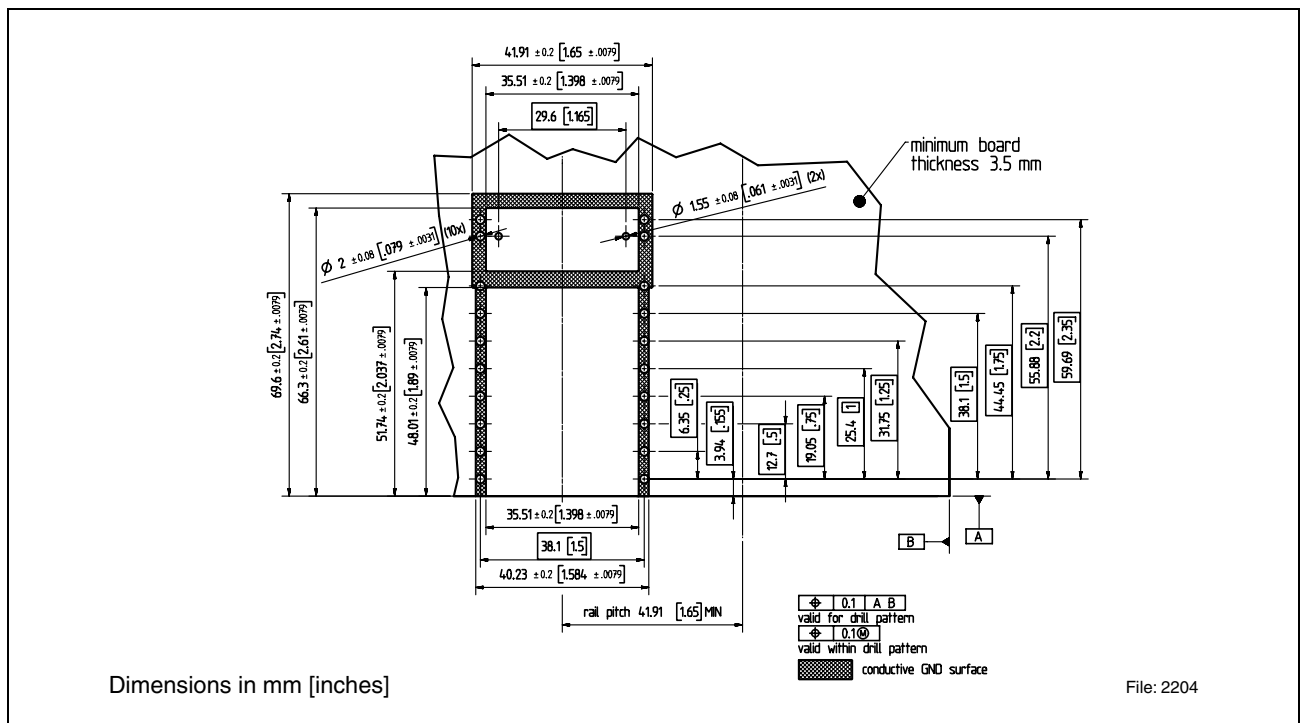


Figure 4 Belly-to-Belly Mounting

Host Board Layouts

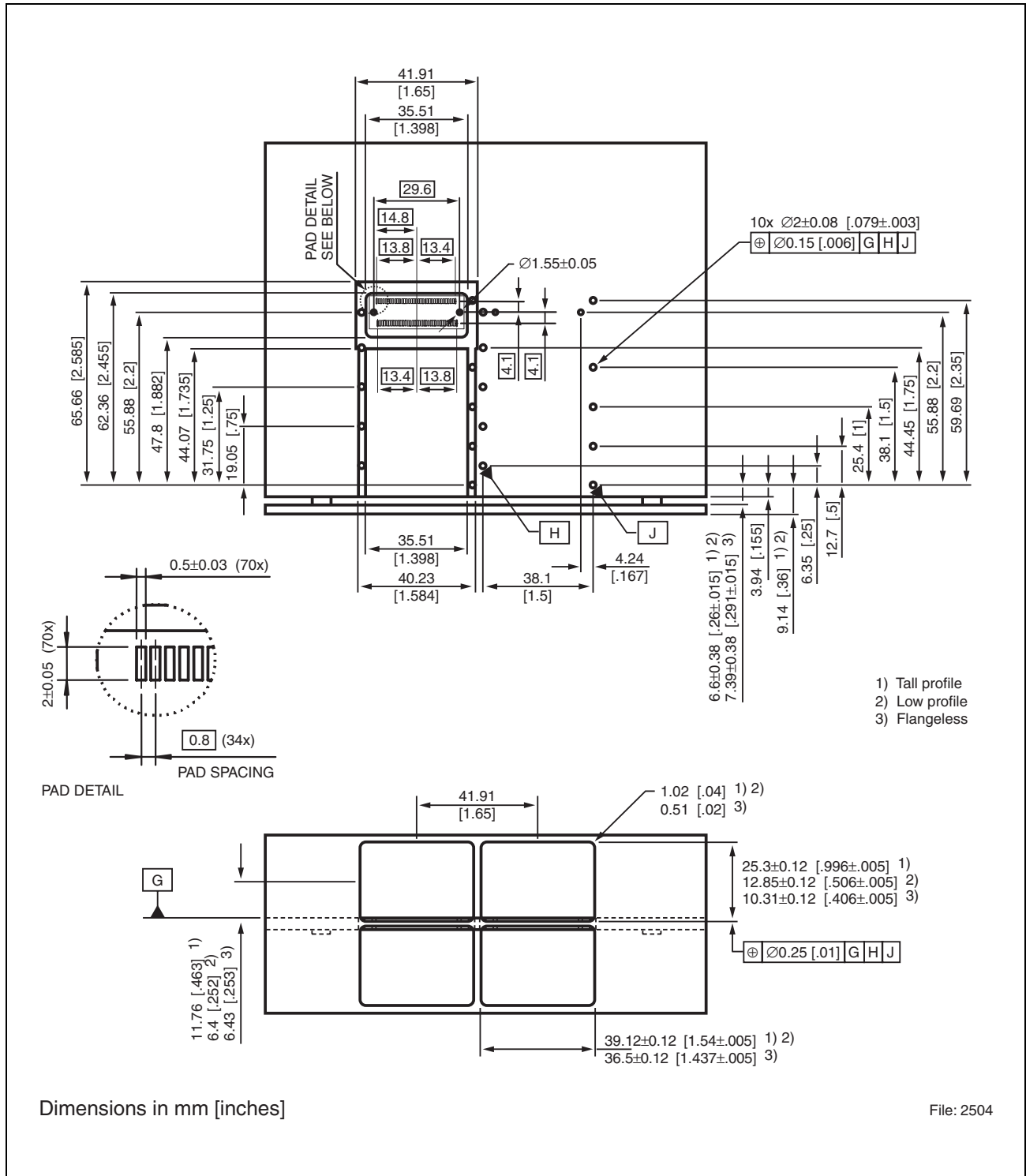


Figure 5 Host PCB, Board Connector Layout and Bezel Opening

Package Outlines

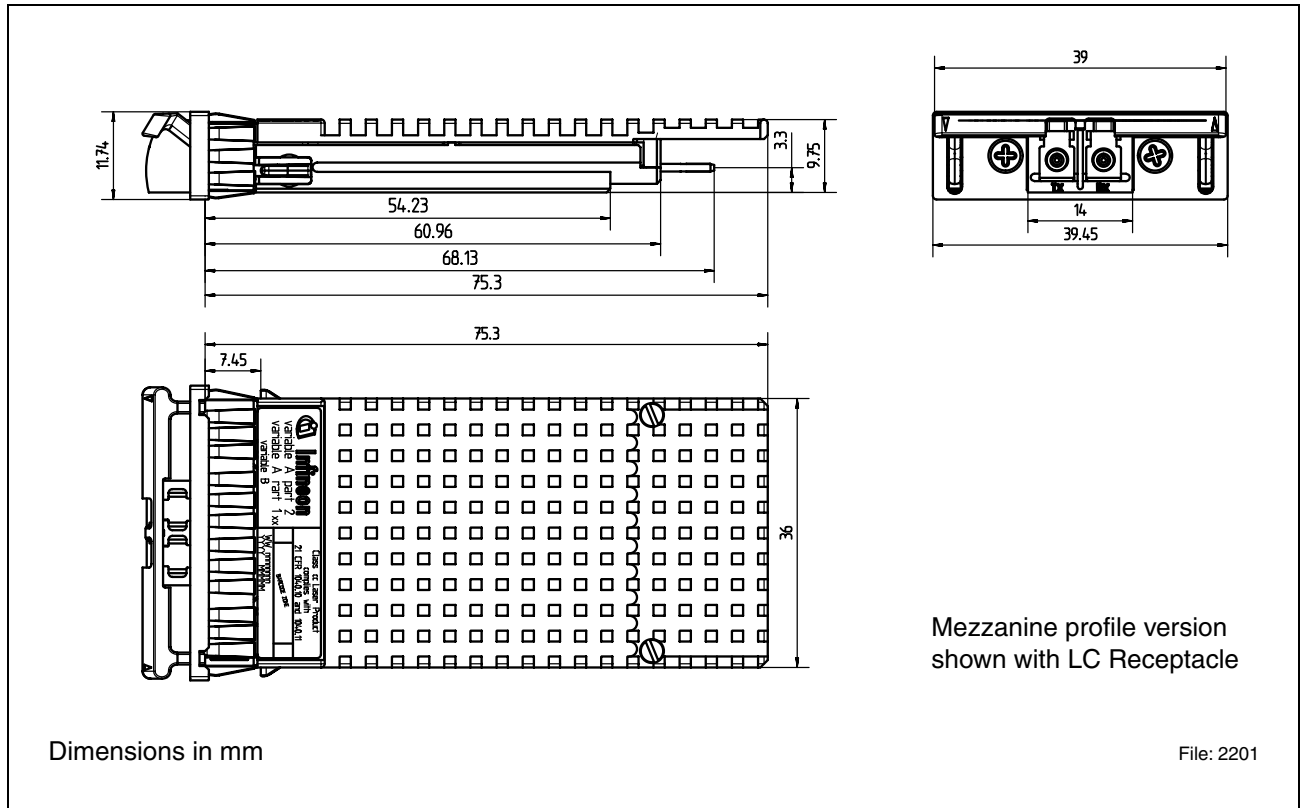


Figure 7 Mechanical Dimensions

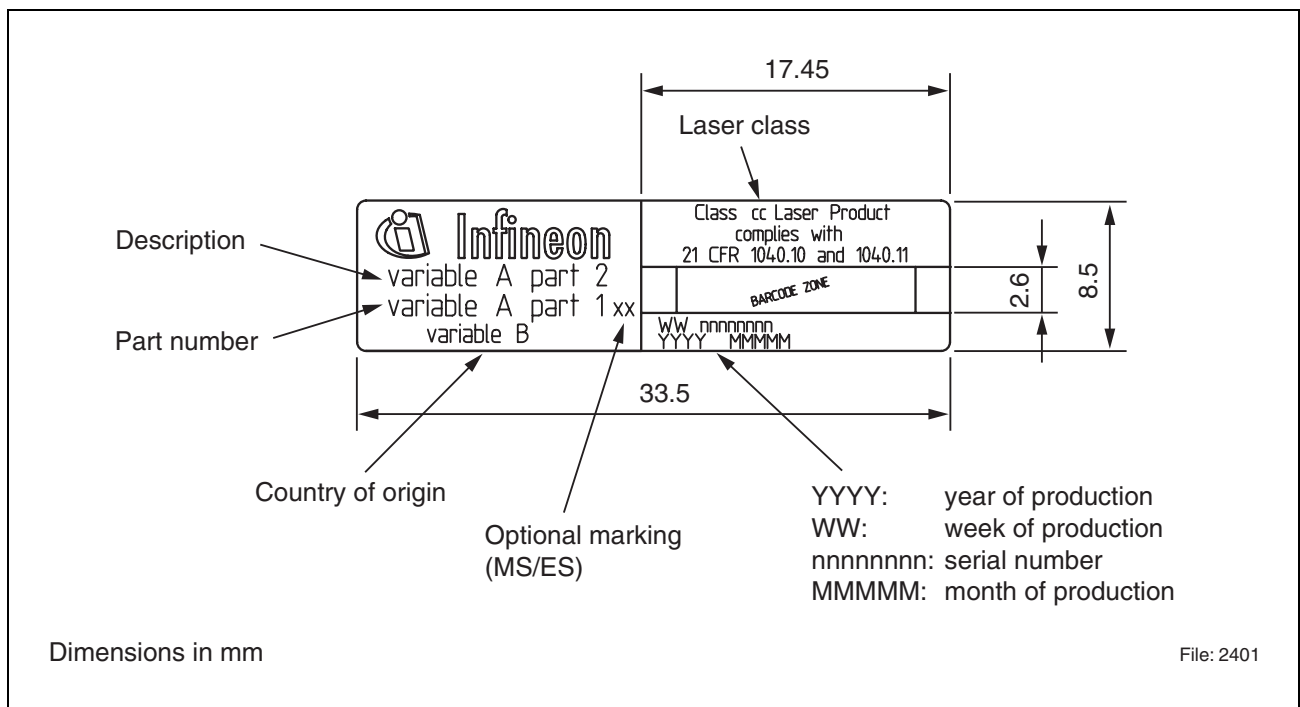


Figure 8 Label Description

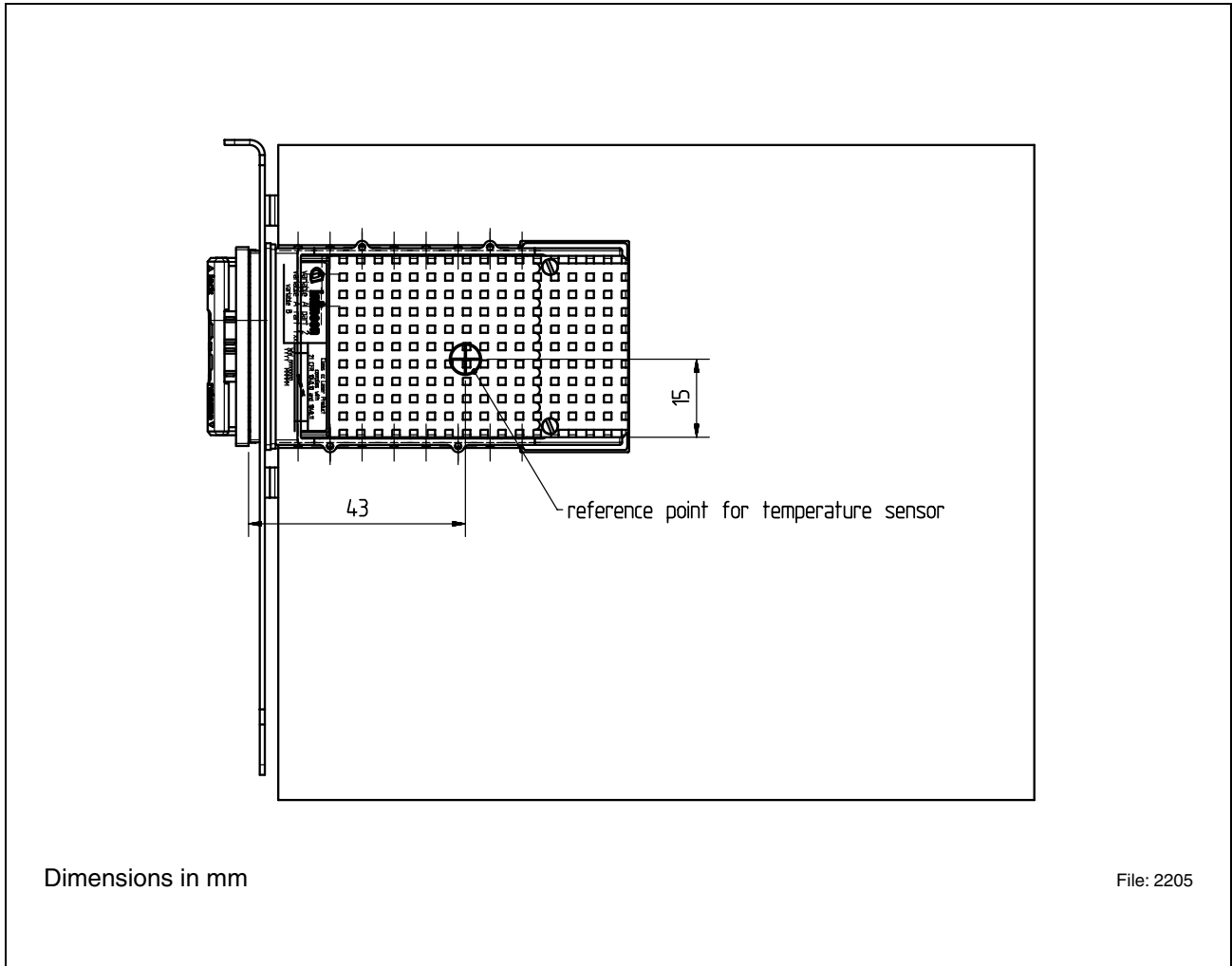


Figure 9 XPAK Temperature Reference Point

V23833-G2005-A101

V23833-G6005-A101

Revision History: 2004-02-23

DS2

Previous Version: 2003-08-25

Page	Subjects (major changes since last revision)
1	Features Optical changed
2	Features Mechanical changed
5, 8, 12, 13, 14	Tables changed
10	Table " Regulatory Compliance " changed
11	Table " Absolute Maximum Ratings " changed

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