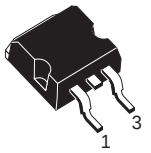
STB60NE03L-12

N-CHANNEL 30V - 0.009 Ω - 60A D^2PAK
STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB60NE03L-12	30 V	<0.012 Ω	60 A

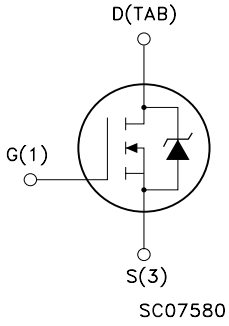
- TYPICAL $R_{DS}(on)$ = 0.009 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETETIVE AVALANCHE DATA AT 100 ^{0}C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175 ^{0}C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL



D^2PAK
TO-263
(suffix"T4")

DESCRIPTION
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS
- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE ENVIRONMENT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	±20	V
I_D	Drain Current (continuos) at T_C = 25°C	60	A
I_D	Drain Current (continuos) at T_C = 100°C	42	A
I_{DM}(•)	Drain Current (pulsed)	240	A
P_{tot}	Total Dissipation at T_C = 25°C	100	W
	Derating Factor	0.67	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(•)Pulse width limited by safe operating area

(1)$I_{SD} \leq$ 60 A, di/dt ≥ 300A/ms, $V_{DD} \leq V_{(BR)DSS}$, Tj ≤ T_{JMA}

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case Max	Max	1.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient Max	Max	62.5	°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink Typ	Max	0.5	°C/W
T_j	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	60	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 15 V)	150	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 30 A V_{GS} = 5 V I_D = 30 A		0.009	0.012 0.018	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	60			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D=30 A	20	30		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitances	V_{DS} = 25V f = 1 MHz V_{GS} = 0		2200 570 200	2800 750 250	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15 V I_D = 30 A R_G = 4.7 Ω V_{GS} = 5 V (see test circuit, Figure 3)		40 260	50 320	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 24 V I_D= 60 A V_{GS}=5 V		35 18 13	45	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{clamp} = 24 V I_D = 60 A R_G = 4.7 Ω V_{GS} = 5 V (Inductive Load, see fig.5)		35 120 175	50 160 230	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				60 240	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 60 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} =60 A di/dt = 100 A/µs V_{DD} = 24 V T_j = 150 °C (see test circuit, Figure 5)		55 0.1 3.5		ns µC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

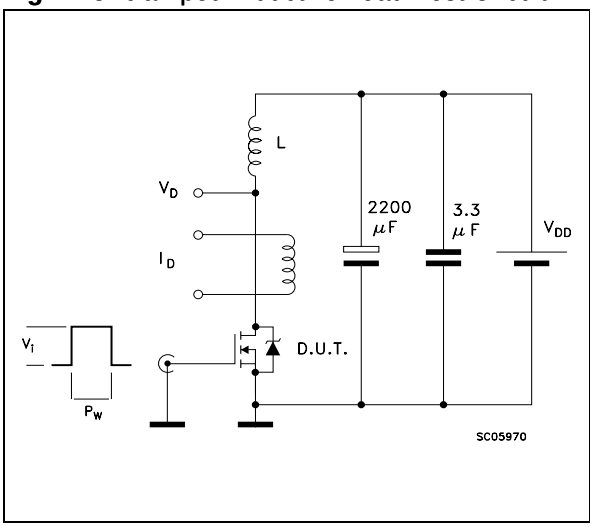


Fig. 2: Unclamped Inductive Waveform

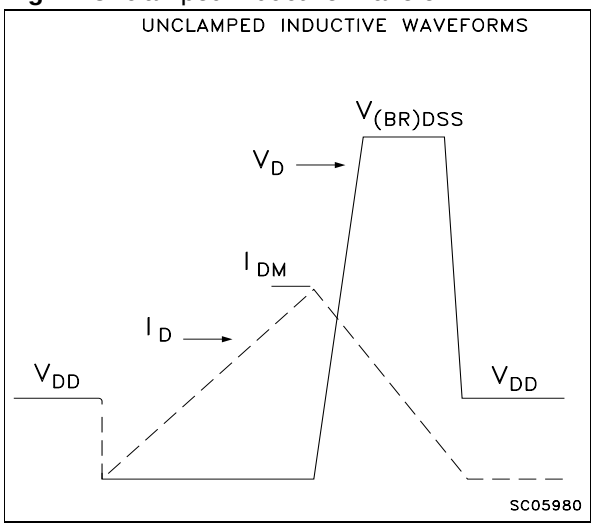


Fig. 3: Switching Times Test Circuits For Resistive Load

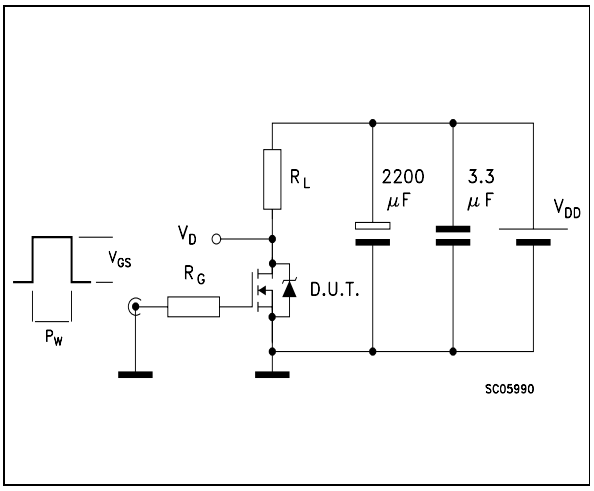


Fig. 4: Gate Charge test Circuit

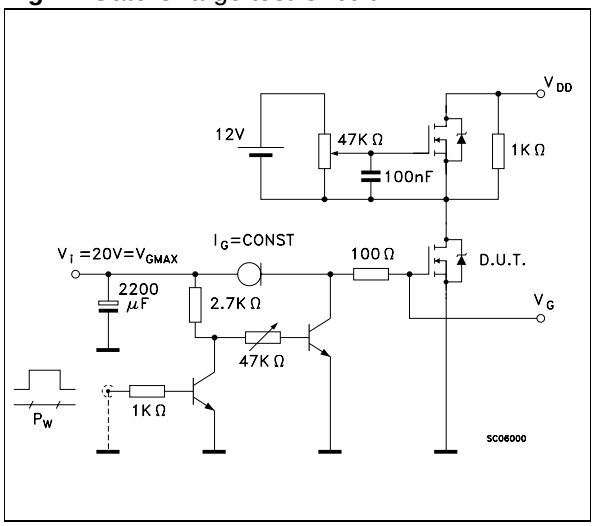
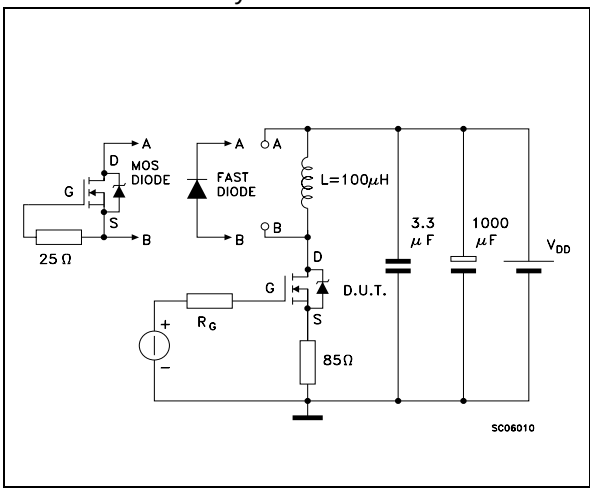


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		8º