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# ICS8737I-11
## LOW SKEW ÷1/÷2
### DIFFERENTIAL-TO- 3.3V LVPECL CLOCK GENERATOR

## GENERAL DESCRIPTION

HiPerClockS™

The ICS8737I-11 is a low skew, high perfor-mance Differential-to-3.3V LVPECL Clock Generator/Divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8737I-11 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8737I-11 ideal for clock distribution applications demanding well defined performance and repeatability.

## FEATURES

- 2 divide by 1 differential 3.3V LVPECL outputs; 2 divide by 2 differential 3.3V LVPECL outputs

- Selectable differential CLK, nCLK or LVPECL clock inputs

- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL

- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL

- Maximum output frequency: 650MHz

- Translates any single ended input signal (LVCMOS, LVTTL, GTL) to LVPECL levels with resistor bias on nCLK input

- Output skew: 75ps (maximum)

- Part-to-part skew: 300ps (maximum)

- Bank skew: Bank A - 30ps (maximum)
  Bank B - 45ps (maximum)

- 3.3V operating supply

- -40°C to 85°C ambient operating temperature

## BLOCK DIAGRAM
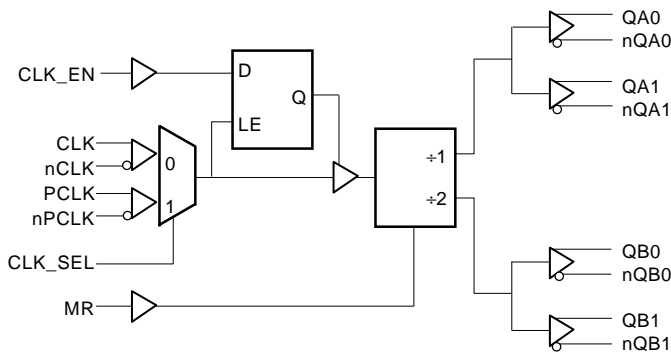


## PIN ASSIGNMENT
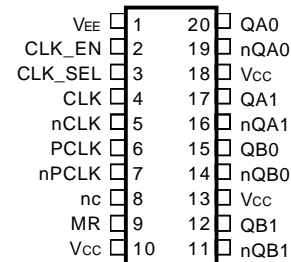


**ICS8737I-11**
**20-Lead TSSOP**
6.50mm x 4.40mm x 0.92 package body
**G Package**
Top View

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### TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{EE}$ | Power | | Negative supply pin. |
| 2 | CLK_EN | Power | Pullup | Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVTTL / LVCMOS interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock Select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVTTL / LVCMOS interface levels. |
| 4 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 5 | nCLK | Input | Pullup | Inverting differential clock input. |
| 6 | PCLK | Input | Pulldown | Non-inverting differential LVPECL clock input. |
| 7 | nPCLK | Input | Pullup | Inverting differential LVPECL clock input. |
| 8 | nc | Unused | | No connect. |
| 9 | MR | Input | Pulldown | Master reset. Resets the output divider. LVCMOS / LVTTL interface levels. |
| 10, 13, 18 | $V_{CC}$ | Power | | Positive supply pins. |
| 11, 12 | nQB1, QB1 | Output | | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQB0, QB0 | Output | | Differential output pair. LVPECL interface levels. |
| 16, 17 | nQA1, QA1 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQA0, QA0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

### TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 4 | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | KΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | KΩ |

# ICS8737I-11

LOW SKEW ÷1/÷2
DIFFERENTIAL-TO- 3.3V LVPECL CLOCK GENERATOR

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**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| MR | CLK_EN | CLK_SEL | Selected Source | QA0, QA1 | nQA0, nQA1 | QB0, QB1 | nQB0, nQB1 |
| 1 | X | X | X | LOW | HIGH | LOW | HIGH |
| 0 | 0 | 0 | CLK, nCLK | Disabled; LOW | Disabled; HIGH | Disabled; LOW | Disabled; HIGH |
| 0 | 0 | 1 | PCLK, nPCLK | Disabled; LOW | Disabled; HIGH | Disabled; LOW | Disabled; HIGH |
| 0 | 1 | 0 | CLK, nCLK | Enabled | Enabled | Enabled | Enabled |
| 0 | 1 | 1 | PCLK, nPCLK | Enabled | Enabled | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.
In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.
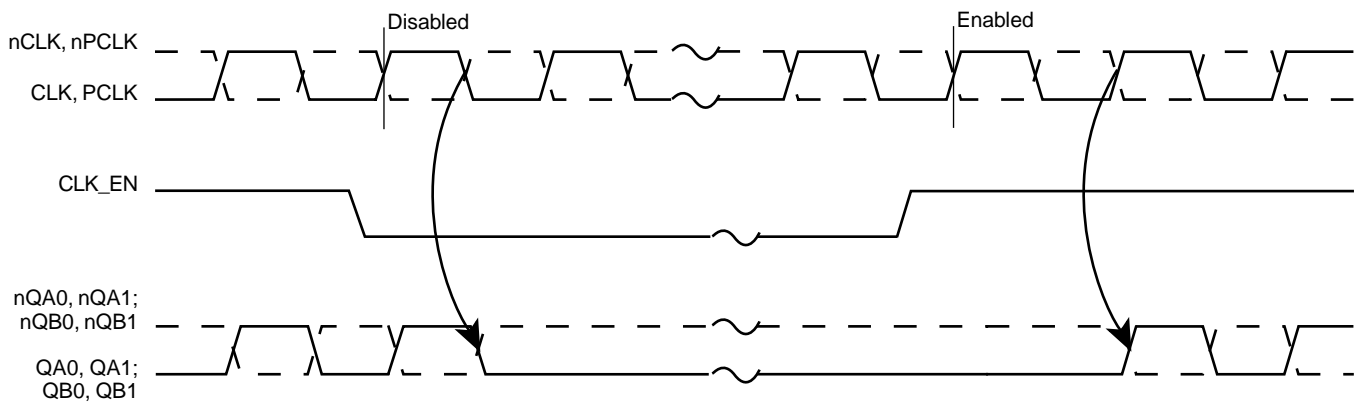


**FIGURE 1 - CLK_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

| Inputs | | Outputs | | | | Input to Output Mode | Polarity |
|---|---|---|---|---|---|---|---|
| CLK or PCLK | nCLK or nPCLK | QAx | nQAx | QBx | nQBx | | |
| 0 | 0 | LOW | HIGH | LOW | HIGH | Differential to Differential | Non Inverting |
| 1 | 1 | HIGH | LOW | HIGH | LOW | Differential to Differential | Non Inverting |
| 0 | Biased; NOTE 1 | LOW | HIGH | LOW | HIGH | Single Ended to Differential | Non Inverting |
| 1 | Biased; NOTE 1 | HIGH | LOW | HIGH | LOW | Single Ended to Differential | Non Inverting |
| Biased; NOTE 1 | 0 | HIGH | LOW | HIGH | LOW | Single Ended to Differential | Inverting |
| Biased; NOTE 1 | 1 | LOW | HIGH | LOW | HIGH | Single Ended to Differential | Inverting |

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{CC}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 55 | mA |

### TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | CLK_EN, CLK_SEL, MR | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | CLK_EN, CLK_SEL, MR | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK_EN | $V_{IN} = V_{CC}$ = 3.465V | | | 5 | μA |
| | | CLK_SEL, MR | $V_{IN} = V_{CC}$ = 3.465V | | | 150 | μA |
| $I_{IL}$ | Input Low Current | CLK_EN | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -150 | | | μA |
| | | CLK_SEL,MR | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -5 | | | μA |

### TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | nCLK | $V_{IN} = V_{CC}$ = 3.465V | | | 5 | μA |
| | | CLK | $V_{IN} = V_{CC}$ = 3.465V | | | 150 | μA |
| $I_{IL}$ | Input Low Current | nCLK | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -150 | | | μA |
| | | CLK | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -5 | | | μA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 0.5 | | $V_{CC}$ - 0.85 | V |

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{CC}$ + 0.3V.
NOTE 2: Common mode voltage is defined as $V_{IH}$.

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**TABLE 4D. LVPECL DC CHARACTERISTICS,** $V_{CC}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | $V_{IN} = V_{CC}$ = 3.465V | | | 150 | µA |
| | | $V_{IN} = V_{CC}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -5 | | | µA |
| | | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | 0.3 | | 1 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE}$ + 1.5 | | $V_{CC}$ | V |
| $V_{OH}$ | Output High Voltage; NOTE 3 | | $V_{CC}$ - 1.4 | | $V_{CC}$ - 1.0 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 3 | | $V_{CC}$ - 2.0 | | $V_{CC}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 0.9 | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is $V_{CC}$ + 0.3V.
NOTE 3: Outputs terminated with 50Ω to $V_{CC}$ - 2V.

**TABLE 5. AC CHARACTERISTICS,** $V_{CC}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | | 650 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | CLK, nCLK | $f ≤$ 650MHz | 1.2 | | 1.8 | ns |
| | | PCLK, nPCLK | $f ≤$ 650MHz | 1.1 | | 1.7 | ns |
| $t$sk(o) | Output Skew; NOTE 2, 4 | | | | | 75 | ps |
| $t$sk(b) | Bank Skew; NOTE 4 | Bank A | | | | 30 | ps |
| | | Bank B | | | | 45 | ps |
| $t$sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | | 300 | ps |
| $t_R$ | Output Rise Time | | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| $t_F$ | Output Fall Time | | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| odc | Output Duty Cycle | | | 47 | 50 | 53 | % |

All parameters measured at 500MHz unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
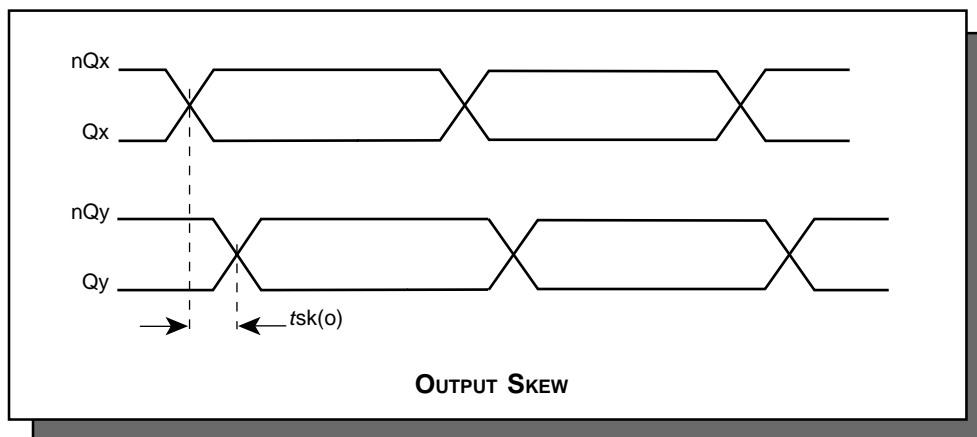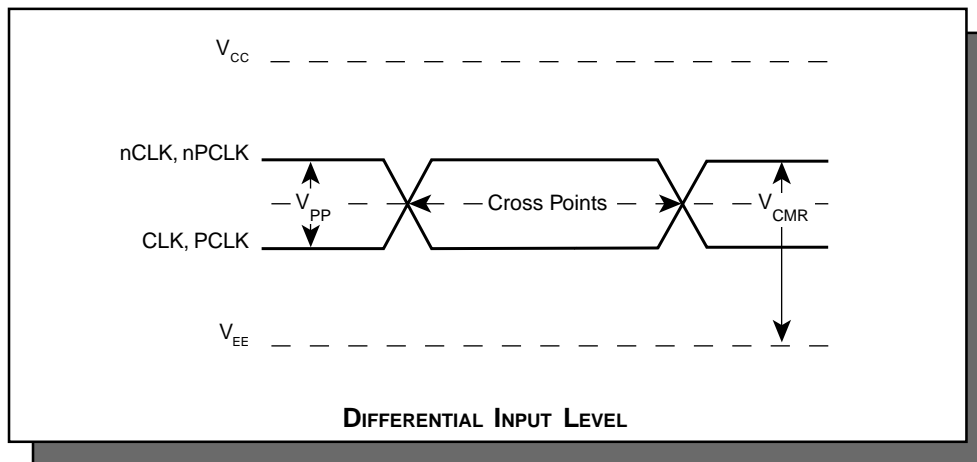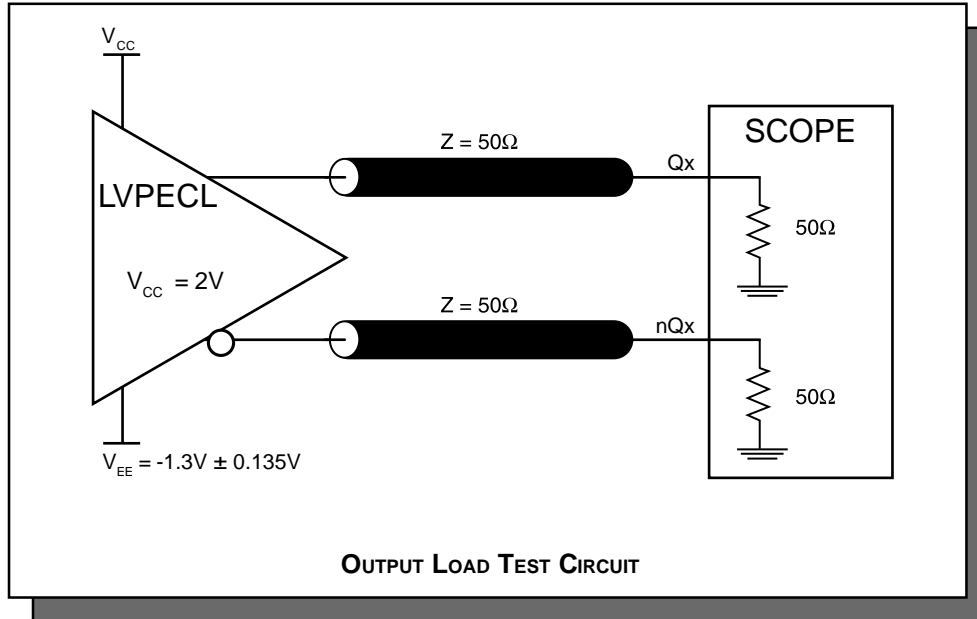NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages
and with equal load conditions. Using the same type of inputs on each device, the outputs are measured
at the differential cross points.
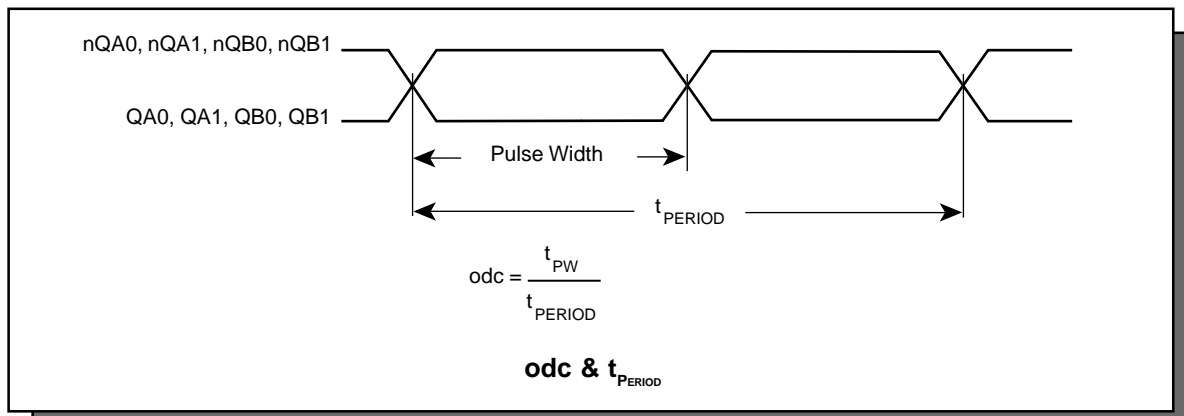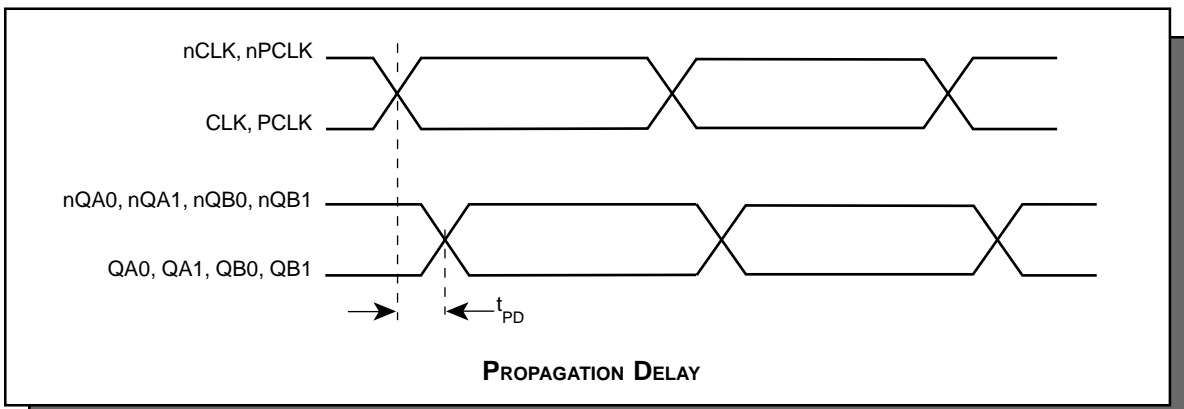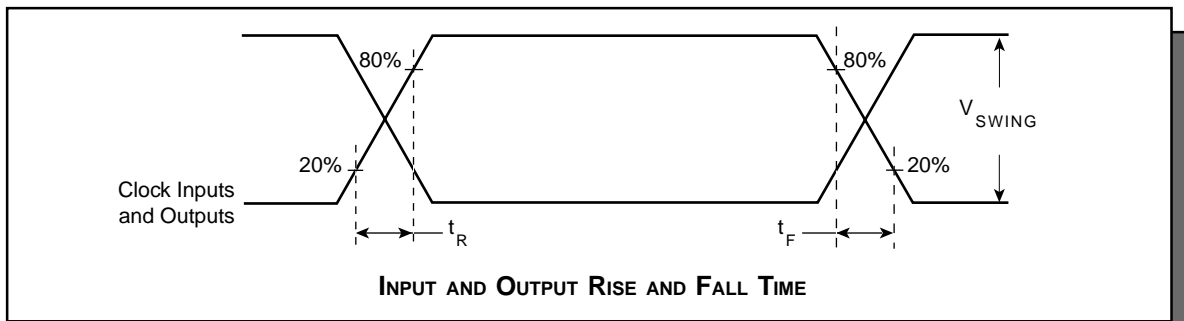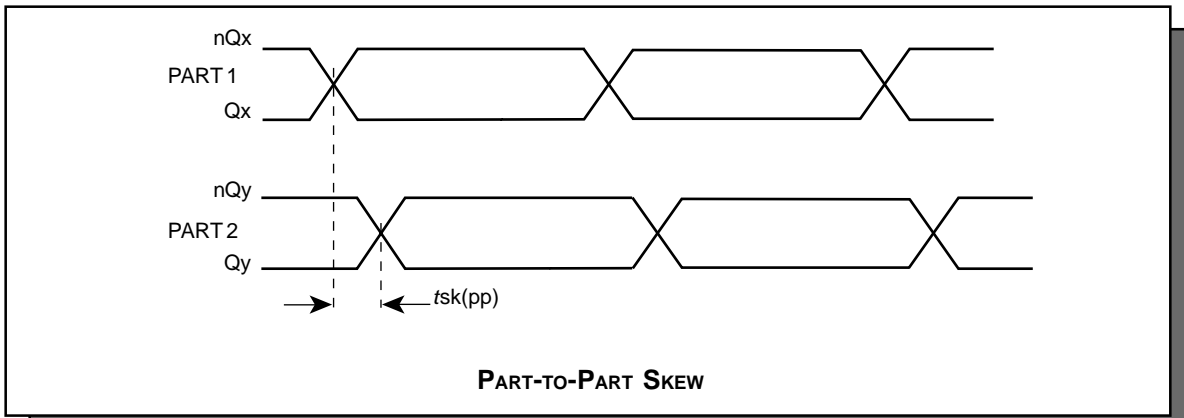NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

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# PARAMETER MEASUREMENT INFORMATION



$V_{CC}$

LVPECL

$V_{CC}$ = 2V

$Z = 50\Omega$

$Z = 50\Omega$

Qx

nQx

SCOPE

$50\Omega$

$50\Omega$

$V_{EE}$ = -1.3V ± 0.135V

**OUTPUT LOAD TEST CIRCUIT**



$V_{CC}$

nCLK, nPCLK

CLK, PCLK

$V_{PP}$

Cross Points

$V_{CMR}$

$V_{EE}$

**DIFFERENTIAL INPUT LEVEL**



nQx

Qx

nQy

Qy

$t$sk(o)

**OUTPUT SKEW**

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nQx
PART 1
Qx

nQy
PART 2
Qy

$t$sk(pp)

**PART-TO-PART SKEW**

80%          80%

$V_{SWING}$

20%          20%

Clock Inputs
and Outputs

$t_R$          $t_F$

**INPUT AND OUTPUT RISE AND FALL TIME**

nCLK, nPCLK

CLK, PCLK

nQA0, nQA1, nQB0, nQB1

QA0, QA1, QB0, QB1

$t_{PD}$

**PROPAGATION DELAY**

nQA0, nQA1, nQB0, nQB1

QA0, QA1, QB0, QB1

Pulse Width

$t_{PERIOD}$

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**odc & $t_{PERIOD}$**

# ICS8737I-11
## Low Skew ÷1/÷2
### Differential-to- 3.3V LVPECL Clock Generator

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## APPLICATION INFORMATION
### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF $\sim V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC}$ = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.



**FIGURE 2 - SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT**
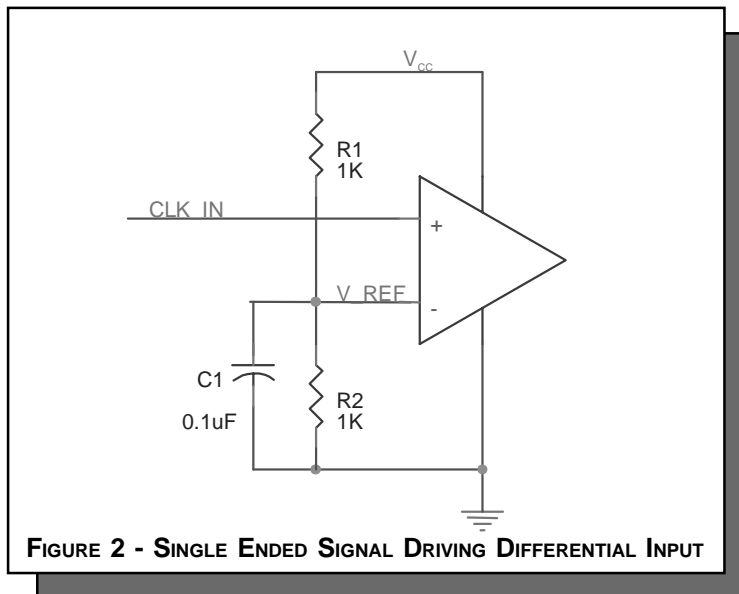
### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
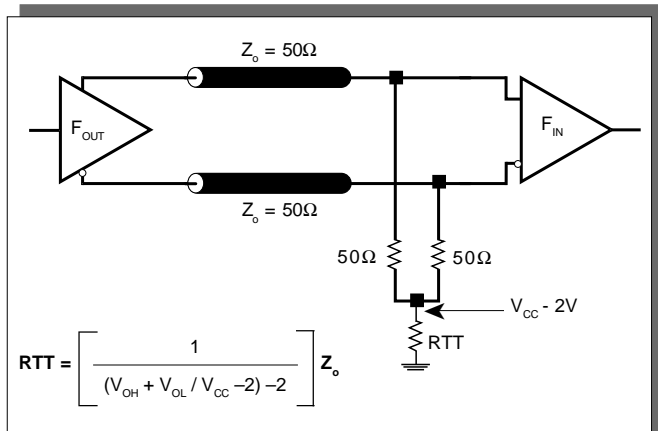


$$RTT = \left[ \frac{1}{(V_{OH} + V_{OL} / V_{CC} - 2) - 2} \right] Z_o$$

**FIGURE 3A - LVPECL OUTPUT TERMINATION**



**FIGURE 3B - LVPECL OUTPUT TERMINATION**

Integrated
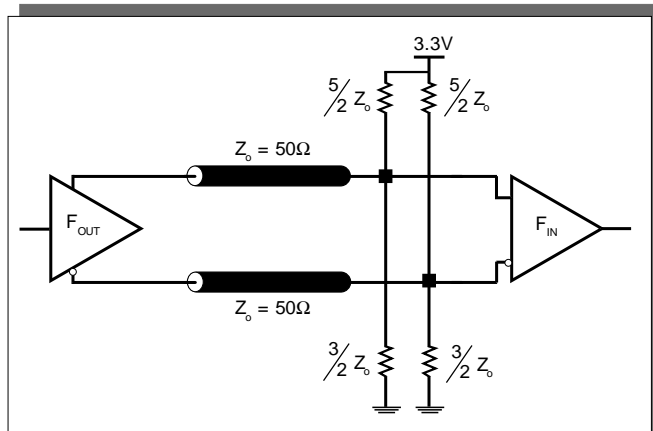Circuit
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# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8737I-11.
Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS8737I-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{CC\_MAX}$ = 3.465V * 55mA = **190.6mW**

- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.2mW = **120.8mW**

  **Total Power$_{\_MAX}$** (3.465V, with all outputs switching) = 190.6mW + 120.8mW = **311.4mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.311W * 66.6°C/W = 105.7°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE $\theta_{JA}$ FOR 20-PIN TSSOP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |
| **NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. | | | |

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### DIFFERENTIAL-TO- 3.3V LVPECL CLOCK GENERATOR

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*3. Calculations and Equations.*

LVPECL output driver circuit and termination are shown in *Figure 4.*



**FIGURE 4 - LVPECL DRIVER CIRCUIT AND TERMINATION**
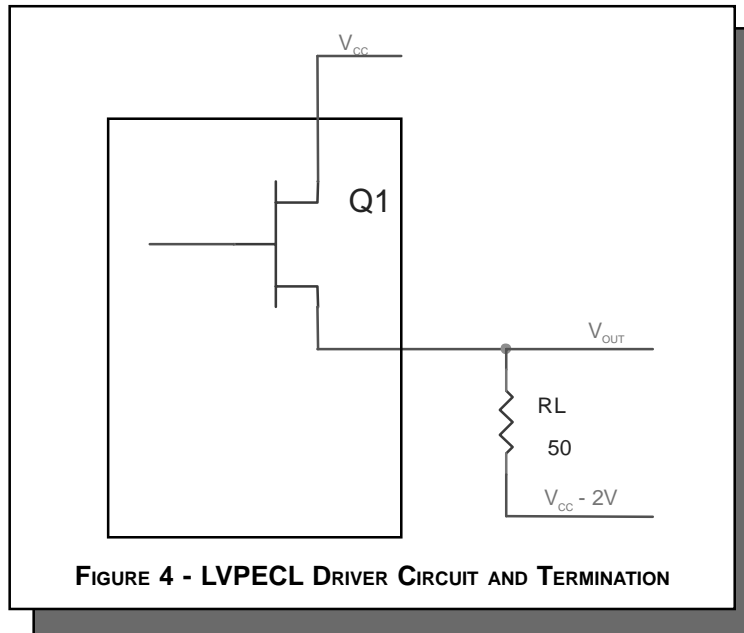
To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 1.0V}$

    $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

    $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50Ω] * 1V = \mathbf{20.0mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

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# RELIABILITY INFORMATION

**TABLE 7.** $\theta_{JA}$ **VS. AIR FLOW TABLE**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **200** | **500** |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TRANSISTOR COUNT**

The transistor count for ICS8737I-11 is: 510

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**PACKAGE OUTLINE - G SUFFIX**
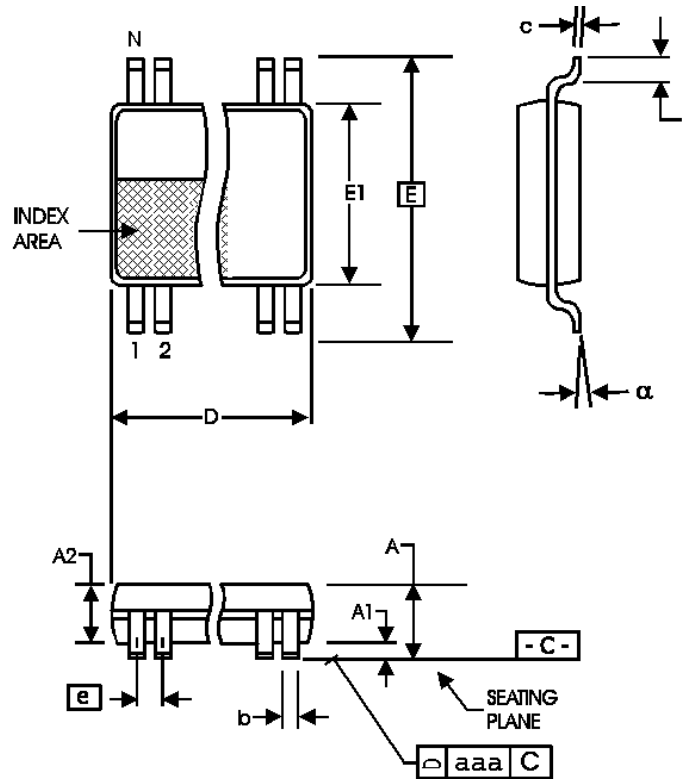


**TABLE 8. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
| --- | --- | --- |
| | Minimum | Maximum |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

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### TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS8737AGI-11 | ICS8737AI-11 | 20 lead TSSOP | 72 | -40°C to 85°C |
| ICS8737AGI-11T | ICS8737AI-11 | 20 lead TSSOP on Tape and Reel | 2500 | -40°C to 85°C |

**ICS8737I-11**

LOW SKEW ÷1/÷2

DIFFERENTIAL-TO- 3.3V LVPECL CLOCK GENERATOR

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| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| A | | 8 | Added Termination for LVPECL Outputs section. | 6/3/02 |
| | | | | |
| | | | | |