SONY

CXD1271Q/R

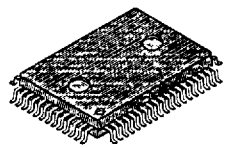
Cellular Telephone Filter LSI

Description

The CXD1271Q/R is a filter LSI chip designed for the cellular telephone. A successor to the already marketed CXD1237Q/R, this LSI chip conforms to the N-TACS standards and is easy to adjust as it allows serial data based gain control.

Also, a modem is formed by combining the CXD1271Q/R to the CXD1270Q/R control signal processing LSI.

CXD1271Q
64 pin QFP (Plastic)



CXD1271R
64 pin VQFP (Plastic)

Structure

Silicon gate CMOS IC

Features

- Ultra-low current consumption
  2.1mA during operation; 0.6mA during PS (5V Typ.)
- Increased power savings
- 4-bit control attenuator for ease of gain adjustment
- Conforms to the AMPS, DOC, TACS, and N-TACS standards
- Stable characteristics due to the use of SCF technology
- Built-in electronic volume control varies the level over eight 3dB steps

Functions

- Received DATA filtering
- Received SAT PLL lock detection
- Transmitted DATA filtering and summing
- Received voice filtering
- Transmitted voice filtering
- Serial data based gain control
- Volume control (2 systems)

Absolute Maximum Ratings

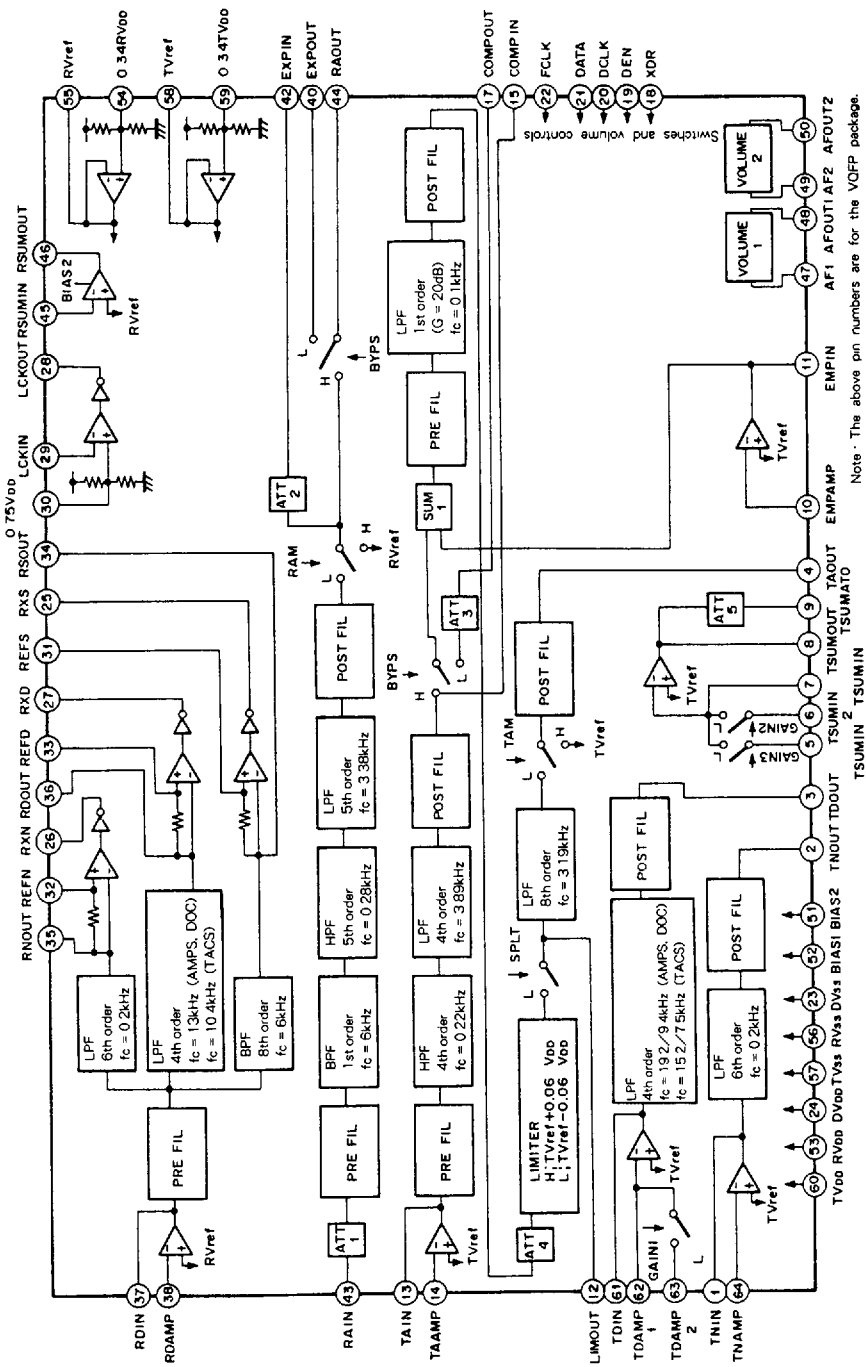
• Supply voltage	V_{DD}	–0.3 to 7.0	V
• Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	–34 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	–34 to +85	°C

E91650 – ST

Block Diagram



Pin Description

Pin No.		Symbol	I/O	Description
VQFP	QFP			
1	3	TNIN	O	Output for the transmitted data (N-TACS standard) input gain control amplifier.
2	4	TNOUT	O	Filter output for transmitted data (N-TACS standard).
3	5	TDOUT	O	Filter output for the transmitted WIDE BAND DATA, ST, and SAT.
4	6	TAOUT	O	Filter output for transmitted voice.
5	7	TSUMIN3	I	Input for the transmitter system summing amplifier. Gain control through the GAIN3 control data.
6	8	TSUMIN2	I	Input for the transmitter system summing amplifier. Gain control through the GAIN2 control data.
7	9	TSUMIN1	I	Input for the transmitter system summing amplifier. Used in conjunction with the TSUMIN2 and TSUMIN3 pins for data (TDOUT and TNOUT outputs) and voice (TAOUT) summing and other operations.
8	10	TSUMOUT	O	Output for the transmitter system summing amplifier.
9	11	TSUMATO	O	Output for the transmitter system summing amplifier after attenuation. Controlled by the control data, A5C3 to A5C0.
10	12	EMPAMP	I	Input for the emphasis input, gain control amplifier.
11	13	EMPIN	O	Output for the emphasis input, gain control amplifier.
12	14	LIMOUT	I/O	Output for the transmitted voice limiter. Also serves as the input when the latter stage transmitter splatter filter characteristics are tested on an individual basis.
13	15	TAIN	O	Output for the transmitted voice input gain control amplifier.
14	16	TAAMP	I	Input for the transmitted voice input gain control amplifier.
15	17	COMPIN	O	Output for the external compressor input. Compressor bypass control through the BYPS control data.
16	18	—	—	—
17	19	COMPOUT	I	Input for the external compressor output.
18	20	XDR	I	Control data reset pin. Activated at "Low".
19	21	DEN	I	Load signal input pin for loading serial data into data buffer. Activated at "High".
20	22	DCLK	I	Clock signal input for serial data input.
21	23	DATA	I	8-bit serial data input.
22	24	FCLK	I	Filter clock input. Receives a 4.8MHz clock input.
23	25	DVss	—	Digital system GND.
24	26	DV_{DD}	—	Digital system power supply.

Pin No. VQFP	Pin No. QFP	Symbol	I/O	Description
25	27	RXS	O	Output for the received SAT comparator.
26	28	RXN	O	Output for the received data (N-TACS standard) comparator.
27	29	RXD	O	Output for the received WIDE BAND DATA comparator.
28	30	LCKOUT	O	Output for the received SAT PLL lock detection comparator.
29	31	LCKIN	I	Input for the received SAT PLL lock detection comparator.
30	32	0.75VDD	I	Reference voltage input for the received SAT PLL lock detection comparator. Supply voltage is biased by 0.75. External capacitance of 1 µF is normally connected between this pin and the RVss pin.
31	33	REFS	I	Reference voltage input for the received SAT comparator. External capacitance of 0.1 µF is connected between this pin and the RVss pin to eliminate the output offset of the fore stage band-pass filter.
32	34	REFN	I	Reference voltage input for the received data (N-TACS standard) comparator. External capacitance of 1 µF is connected between this pin and the RVss pin to eliminate the output offset of the fore stage low-pass filter.
33	35	REFD	I	Reference voltage input for the received WIDE BAND DATA comparator. External capacitance of 0.1 µF is connected between this pin and the RVss pin to eliminate the output offset of the fore stage low-pass filter.
34	36	RSOUT	O	Filter output for the received SAT.
35	37	RNOUT	O	Filter output for the received data (N-TACS standard).
36	38	RDOUT	O	Filter output for the received WIDE BAND DATA. Also capable of the received voice prefatory-filter function.
37	39	RDIN	O	Output for the received WIDE BAND DATA/SAT input gain control amplifier.
38	40	RDAMP	I	Input for the received WIDE BAND DATA/SAT input gain control amplifier.
39	41	—	—	—
40	42	EXPOUT	I	Input for the external expander output.
41	43	—	—	—
42	44	EXPIN	O	Output for the input to the external expander. As with the transmitter compressor, bypass control is through the BYPS control data.
43	45	RAIN	O	Input for the received voice.
44	46	RAOUT	O	Filter output for the received voice.
45	47	RSUMIN	I	Input for the receiver system summing amplifier. Used mainly for DTMF and voice summing.
46	48	RSUMOUT	O	Output for the receiver system summing amplifier.
47	49	AF1	I	Input for volume control 1.
48	50	AFOUT1	O	Output for volume control 1. Volume control is through the control data, V1C2 to V1C0.

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Pin No.		Symbol	I/O	Description
VQFP	QFP			
49	51	AF2	I	Input for volume control 2.
50	52	AFOUT2	O	Output for volume control 2. Volume control is through the control data, V2C2 to V2C0.
51	53	BIAS2	I	Determines the receiver summing amplifier bias current. A 100kΩ resistor is normally connected between this pin and the RV_{DD} pin.
52	54	BIAS1	I	Determines the internal operational amplifier bias current. A 500kΩ resistor is normally connected between this pin and the RV_{DD} pin.
53	55	RV_{DD}	—	Receiver system power supply.
54	56	$0.34RV_{DD}$	I	Reference voltage input for the receiver processing system operational amplifier. Supply voltage is biased by 0.34. External capacitance of 1 µF is normally connected between this pin and the RVss pin.
55	57	RVref	O	Reference voltage output for the receiver processing system operational amplifier. Supply voltage is biased by 0.34. External capacitance of 1 µF is normally connected between this pin and the RVss pin.
56	58	RVss	—	Receiver system GND.
57	59	TVss	—	Transmitter system GND.
58	60	TVref	O	Reference voltage output for the transmitter processing system operational amplifier. Supply voltage is biased by 0.34. External capacitance of 1 µF is normally connected between this pin and the TVss pin.
59	61	$0.34TV_{DD}$	I	Reference voltage input for the transmitter processing system operational amplifier. Supply voltage is biased by 0.34. External capacitance of 1 µF is normally connected between this pin and the TVss pin.
60	62	TV_{DD}	—	Transmitter power supply.
61	63	TDIN	O	Output for the transmitted WIDE BAND DATA/ST/SAT input summing amplifier.
62	64	TDAMP1	I	Input for the transmitted SAT.
63	1	TDAMP2	I	Input for the transmitted WIDE BAND DATA/ST. Gain control is through the GAIN1 control data.
64	2	TNAMP	I	Input for the transmitted data (N-TACS standard) input gain control amplifier.

Electrical Characteristics

(V_{DD}=5V ± 10%, Ta=–34 to +85°C)

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Supply current 1 (N-TACS specification)	I_{DD1}	RV_{DD} TV_{DD} DV_{DD} Total	STD="L" STN="L" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	2.1	4.0	mA
Supply current 2 (Non-N-TACS specification)	I_{DD2}	RV_{DD} TV_{DD} DV_{DD} Total	STD="L" STN="H" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	1.9	3.6	mA
Supply current 3 (Standby for all excluding volume)	I_{STB1}	RV_{DD} TV_{DD} DV_{DD} Total	STD="H" STN="H" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	0.7	1.2	mA
Supply current 4 (All standby)	I_{STB2}	RV_{DD} TV_{DD} DV_{DD} Total	STD="H" STN="H" V1ST=V2ST="H" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	0.6	1.0	mA
Digital input voltage "Low"	V_{IL}	FCLK, DATA, DCLK, DEN, XDR	—	—	—	0.3V_{DD}	V
Digital input voltage "High"	V_{IH}	FCLK, DATA, DCLK, DEN, XDR	—	0.7V_{DD}	—	—	V
Digital input current "Low"	I_{IL}	FCLK, DATA, DCLK, DEN, XDR	V_{IN}=GND	–10	—	10	µA
Digital input current "High"	I_{IH1}	FCLK, DATA, DCLK, DEN, XDR	V_{IN}=V_{DD}	–10	—	10	µA
Digital output voltage "Low"	V_{OL}	RXD, RXN, RXS, LCKOUT	I_{OL}=0.4mA	—	—	0.8	V
Digital output voltage "High"	V_{OH}	RXD, RXN, RXS, LCKOUT	I_{OH}=–0.4mA	V_{DD}–1	—	—	V
Analog input voltage range	V_{LA}	RDAMP, RAIN, TAAMP, TNAMP TDAMP1, TDAMP2, RSUMIN, TSUMIN1, TSUMIN2, TSUMIN3 AF1, AF2, EMPAMP	BIAS1=500kΩ	—	—	1	Vp-p
Analog input resistance	R_I	AF1, RAIN, AF2, COMPOUT	Input pin –0.34V_{DD}	70	130	190	kΩ
Analog switch "ON" resistance	R_{SW}	TDAMP2, TSUMIN2, TSUMIN3, EXPOUT, RAOUT	Input pin –0.34V_{DD}	—	0.6	1.5	kΩ

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Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Analog output load resistance 1	R_{L1}	RSUMOUT	Output pin $-0.34V_{DD}$ BIAS2 resistance=100kΩ	2	—	—	kΩ
Analog output load resistance 2	R_{L2}	EXPIN, RAOUT, COMPIN, TAOUT, TDOUT, AFOUT1, EMPIN, TSUMOUT, TSUMATO, AFOUT2, TNOUT	Output pin $-0.34V_{DD}$ BIAS1 resistance=500kΩ	10	—	—	kΩ
Analog output load resistance 3	R_{L3}	RDIN, TAIN, TDIN, TNIN	Output pin $-0.34V_{DD}$ BIAS1 resistance=500kΩ	100	—	—	kΩ
Analog output voltage range 1	V_{OA1}	RSUMOUT	BIAS2 resistance=100kΩ Load resistance=2kΩ	—	—	0.4	Vp-p
Analog output voltage range 2	V_{OA2}	EXPIN, RAOUT, COMPIN, EMPIN, TSUMATO, TSUMOUT, TAOUT, TDOUT, RDOUT, TNOUT, AFOUT1, AFOUT2	BIAS1 resistance=500kΩ Load resistance=10kΩ	—	—	0.4	Vp-p
Limiter voltage "Low"	V_{LL}	LIMOUT	SPLT="L"	$0.34V_{DD}$ -0.066 V_{DD}	$0.34V_{DD}$ -0.06 V_{DD}	$0.34V_{DD}$ -0.054 V_{DD}	V
Limiter voltage "High"	V_{LH}	LIMOUT	SPLT="L"	$0.34V_{DD}$ $+0.054$ V_{DD}	$0.34V_{DD}$ $+0.06$ V_{DD}	$0.34V_{DD}$ $+0.066$ V_{DD}	V
Electronic volume control step	V_{STEP}	AF1–AFOUT1 AF2–AFOUT2	—	2.5	3	3.5	dB
Attenuation step	A_{STEP}	—	—	0.2	0.4	0.6	dB
Received DATA filter gain 1 (AMPS)	G_{RD1}	RDAMP–RDOUT	Input: −18dBV 13kHz AT="H"	−5	−3	−1	dB
Received DATA filter gain 2 (TACS)	G_{RD2}	RDAMP–RDOUT	Input: −18dBV 10.4kHz AT="L"	−4	−3	−2	dB
Received DATA (N-TACS) filter gain	G_{RN}	RDAMP–RNOUT	Input: −18dBV 0.2kHz	−4	−3	−2	dB
Received SAT filter gain	G_{SAT}	RDAMP–RSOUT	Input: −18dBV 6kHz	−1	0	1	dB
Transmitted DATA filter gain 1 (AMPS)	G_{TD1}	TDAMP1–TDOUT	Input: −18dBV 19.2kHz AT="H", DS="H"	−5	−3	−1	dB
Transmitted DATA filter gain 2 (AMPS)	G_{TD2}	TDAMP1–TDOUT	Input: −18dBV 9.4kHz AT="H", DS="L"	−4	−3	−2	dB

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Transmitted DATA filter gain 3 (TACS)	G_{TD3}	TDAMP1–TDOUT	Input: –18dBV 15.2kHz AT="L", DS="H"	–5	–3	–1	dB
Transmitted DATA filter gain 4 (TACS)	G_{TD4}	TDAMP1–TDOUT	Input: –18dBV 7.5kHz AT="L", DS="L"	–4	–3	–2	dB
Transmitted DATA (N-TACS) filter gain	G_{TN}	TNAMP–TNOUT	Input: –18dBV 0.2kHz	–4	–3	–2	dB
Received voice filter gain	G_{RA}	RAIN–RAOUT	Input: –16dBV 1kHz RAM="L" BYPS="H" ATT1=0dB	–1	–0.3	1	dB
Received voice muting amount	G_{RAM}	RAIN–RAOUT	Input: –16dBV 1kHz RAM="H" BYPS="H" ATT1=0dB	50	—	—	dB
Received voice S/N ratio	SN_R	RAIN–RAOUT	Input: –16dBV 1kHz RAM="L" BYPS="H" ATT1=0dB Band: 50Hz to 30kHz	50	—	—	dB
Received voice distortion factor	THD_R	RAIN–RAOUT	Input: –16dBV 1kHz RAM="L" BYPS="H" ATT1=0dB Band: 50Hz to 30kHz	—	—	–50	dB
Transmitted voice gain	G_{TA}	TAAMP–TAOUT	Input: –16dBV 1kHz TAM="L" BYPS="H" SPLT="L" ATT4=0dB	–1	–0.3	1	dB
Transmitted voice muting amount	G_{TAM}	TAAMP–TAOUT	Input: –16dBV 1kHz TAM="H" BYPS="H" SPLT="L" ATT4=0dB	50	—	—	dB
Transmitted voice S/N ratio	SN_T	TAAMP–TAOUT	Input: –16dBV 1kHz TAM="L" BYPS="H" SPLT="L" ATT4=0dB Band: 50Hz to 30kHz	45	—	—	dB
Transmitted voice distortion factor	THD_T	TAAMP–TAOUT	Input: –16dBV 1kHz TAM="L" BYPS="H" SPLT="L" ATT4=0dB Band: 50Hz to 30kHz	—	—	–45	dB

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Description of Operation

This IC is a filter IC which is designed for use in cellular car telephones. It conforms to the AMPS (North America), TACS (United Kingdom), DOC (Canada), and N-TACS standards. When this filter IC is combined with the CXD1270Q/R control signal processing LSI chip, a modem is constituted with the following functions:

(1) Received WIDE BAND DATA filtering
(2) Received SAT filtering
(3) Received SAT PLL lock detection
(4) Received N-TACS data filtering
(5) Transmitted WIDE BAND DATA, ST, and SAT summing
(6) Transmitted WIDE BAND DATA, ST, and SAT filtering
(7) Transmitted N-TACS data filtering
(8) Received voice filtering
(9) Transmitted voice filtering
(10) Attenuator and volume control
(11) Serial data input

These functions are detailed below:

1. Received WIDE BAND DATA filtering

In a cellular car telephone system, data is exchanged in the line connection and hand-off processes between land stations (base stations) and mobile stations (mobile switching offices) for channel setup and other purposes. The data consists of Manchester code which is called WIDE BAND DATA. The specified data transmission rate for the AMPS/DOC standard is 20kbaud, and the TACS standard is 16kbaud. The received WIDE BAND DATA is passed through the gain control amplifier and prefilter and fed to the fourth-order Butterworth low-pass filter which functions as a DATA demodulation rolloff filter. The low-pass filter cutoff frequency varies with the cellular system standard and is controlled according to serial data. In the AMPS or DOC cellular system, a low-pass filter cutoff frequency of 13kHz (typical value) is obtained when AT="High". In the TACS or N-TACS system, a low-pass filter cutoff frequency of 10.4kHz (typical value) is obtained when AT="Low".Bandwidth limiting is provided in this manner so as to minimize the error rate.

After the filter output is wave-shaped to CMOS logic levels by a comparator, it is transmitted to the CXD1270Q/R.

2. Received SAT filtering

While the cellular car telephone line is connected (during mobile telephone conversation), the land and mobile stations exchange a sine wave signal called SAT (supervisory audio tone) to acknowledge one another. Each cellular system standard provides three different SAT frequencies: 5.97kHz, 6.00kHz, and 6.03kHz. In the line connection and hand-off processes, one of these three frequencies is chosen. The land station sends 2-bit data called SCC (SAT color code) to the mobile station to notify which frequency is used. While the line is connected, the mobile and land stations receive the SAT from one another to recognize each other.

As is the case with the WIDE BAND DATA, the SAT transmitted from the land station passes through the gain control amplifier and prefilter and then goes through the 6kHz eighth-order Butterworth bandpass filter which is provided to protect the SAT from the voice components (300Hz to 3kHz) and reduce weak electric field high-frequency noise (6kHz to 13kHz). As a bandpass filter having a center frequency of 6kHz is formed, SAT detection is accomplished with high-efficiency. The 6kHz bandpass filter output is wave-shaped to CMOS logic levels by a comparator and then transmitted to the CXD1270Q/R.

3. Received SAT PLL lock detection

When the SAT having a frequency designated by the SCC is received by the CXD1270Q/R, the DPLL is locked. The CXD1271Q/R incorporates a lock /unlock judgment comparator. The output of this comparator switches from the "Low" to the "High" level when the CXD1270Q/R SAT lock detection output (SDET) exceeds the reference voltage (0.75V_{DD}).

4. Received N-TACS data filtering

To obtain 100Hz data to be used in an N-TACS system, the received N-TACS data is passed through the sixth-order Butterworth low-pass filter having a cutoff frequency of 200Hz. The filter output is wave-shaped to CMOS logic levels by a comparator and then transmitted.

5. Transmitted WIDE BAND DATA, ST, and SAT summing

In a cellular car telephone system, the mobile station sends the WIDE BAND DATA or ST and SAT to the land station.

The ST is a signal transmitted for telephone conversation termination or bell ringing purposes. Its frequency is 10kHz (AMPS/DOC standard) or 8kHz (TACS/N-TACS standard). WIDE BAND DATA, ST, and SAT input from the CXD1270Q/R to the CXD1271Q/R is accomplished via an attenuation pad.

The CXD1271Q/R incorporates an inverting summing amplifier which is used to sum up the WIDE BAND DATA, ST, and SAT signals before transmission. As the transmission filer subsequent to the summing amplifier, the fourth-order Butterworth low-pass filter having a cutoff frequency of 19.2kHz (AMPS/DOC standard) or 15.2kHz (TACS/N-TACS standard) is selected at the time of WIDE BAND DATA transmission, or the fourth-order Butterworth low-pass filter having a cutoff frequency of 9.4kHz (AMPS/DOC standard) or 7.5kHz (TACS/N-TACS standard) is chosen at the time of ST transmission.

To compensate for the amplitude characteristics difference between the 19.2kHz (15.2kHz) and 9.4kHz (7.5kHz) low-pass filters at a ST frequency of 10kHz, two different summing amplifiers gains can be selected. For ST transmission, the gain control data (GAIN1) is set to "Low" to obtain a gain of + (plus) several dB or set to "High" to obtain a gain of – (minus) several dB. An external resistor is to be adjusted to obtain the optimum gain.

6. Transmitted WIDE BAND DATA, ST, and SAT filtering

A low-pass filter is provided subsequently to the summing amplifier to eliminate the high-order harmonic content of the summing amplifier output. The AMPS/DOC prescribes that a 20kHz±10% fourth-order Butterworth low-pass filter be used as the transmitted WIDE BAND DATA rolloff filter. Therefore, the CXD1271Q/R employs a 19.2kHz fourth-order Butterworth low-pass filter to meet the AMPS 60kHz attenuation requirement (38dB min.). Further, the cutoff frequency of this transmission filter needs to be lower than 19.2kHz because the ST and SAT transmission frequencies are 10kHz and 6kHz, respectively. The CXD1271Q/R provides control according to serial data. When AT="High" and DS="High", a cutoff frequency of 19.2kHz (typical value) is obtained. When AT="High" and DS="Low", the obtained cutoff frequency is 9.4kHz (typical value).

As for the TACS/N-TACS system, the transmission speed difference is compensated for by obtaining a cutoff frequency of 15.2kHz (typical value) when AT="Low" and DS="High", or a cutoff frequency of 7.5kHz (typical value) when AT="Low" and DS="Low".

7. Transmitted N-TACS data filtering

For the N-TACS system, the sixth-order Butterworth low-pass filter having a cutoff frequency of 200Hz is employed as the transmitted data rolloff filter as is the case with the received N-TACS data.

8. Received voice filtering

Three Butterworth filters are employed to meet each cellular standard.

The input stage is equipped with a gain control amplifier and a loopback distortion elimination prefilter. The output stage is provided with a carrier elimination postfilter.

The RDOUT output is fed into the gain control amplifier, passed through the prefilter, deemphasized by the first-order Butterworth low-pass filter, bandlimited by the fifth-order Butterworth high-pass and low-pass filter, and transferred out via the postfilter.

RAM provides muting control. Expander bypass control is exercised according to the BYPS control data.

9. Transmitted voice filtering

In the transmitter system, the voice is passed through the gain control amplifier and prefilter, bandlimited by the fourth-order Butterworth high-pass filter and low-pass filter, passed through the postfilter prefilter, emphasized by the first-order Butterworth high-pass filter, and transferred out via the postfilter.

Further, the output is entered into the limiter via the gain control amplifier, clipped at 1.7±0.3V (V_{DD}=5V typ.), passed through the eighth-order Butterworth low-pass filter which serves as an abrupt splatter filter, and transferred out via the postfilter.

TAM exercises muting control, and the BYPS control data provides bypass control of compressor.

SPLT is normally at "Low". However, when it is placed at "High", the splatter filter characteristics can be observed without being affected by the limiter.

10. Attenuator and volume control

4-bit control attenuators (ATT1 to ATT5) are provided at places where the voice signal level needs to be fine tuned. Therefore, final level adjustments can be made according to serial data.

Further, two 3-bit control electrical volume controls are incorporated to adjust the loudness of the speaker and exercise linking and other volume control.

* ATT1 to 5

C3	C2	C1	C0	GAIN
1	1	1	1	–2.8
1	1	1	0	–2.4
1	1	0	1	–2.0
1	1	0	0	–1.6
1	0	1	1	–1.2
1	0	1	0	–0.8
1	0	0	1	–0.4
1	0	0	0	0
0	1	1	1	0.4
0	1	1	0	0.8
0	1	0	1	1.2
0	1	0	0	1.6
0	0	1	1	2.0
0	0	1	0	2.4
0	0	0	1	2.8
0	0	0	0	3.2

dB

* VOLUME1, 2

C2	C1	C0	GAIN
1	1	1	–21
1	1	0	–18
1	0	1	–15
1	0	0	–12
0	1	1	–9
0	1	0	–6
0	0	1	–3
0	0	0	0

dB

11. Serial data input

The CXD1271Q/R IC receives internal control data input in the form of 8-bit serial data. The four high-order bits are used for address indication, whereas the remaining four low-order bits are handled as data.

In the input process, 8-bit serial data is entered into the internal shift register when the DCLK clock pulse rises, and put into the internal buffer designated by the address upon receipt of the DEN load signal.

When the XDR reset signal is received, the internal buffer is initialized.

Serial data structure descriptions, timing chart, and switching characteristics descriptions are presented below.

Serial Data Format (8-bit Serial)

t →

7	6	5	4	3	2	1	0

7	6	5	4	3	2	1	0	
0	0	0	0	AT $_0$	SPLT $_0$	BYPS $_0$		
0	0	0	1	RAM $_1$	TAM $_1$	DS $_1$		
0	0	1	0	GAIN1 $_0$	GAIN2 $_0$	GAIN3 $_0$		
0	0	1	1	STD $_1$	STN $_1$	V1ST $_1$	V2ST $_1$	
0	1	0	0					
0	1	0	1					
0	1	1	0	V1C2 $_1$	V1C1 $_1$	V1C0 $_1$		VOLUME1
0	1	1	1	V2C2 $_1$	V2C1 $_1$	V2C0 $_1$		VOLUME2
1	0	0	0	A1C3 $_1$	A1C2 $_0$	A1C1 $_0$	A1C0 $_0$	ATT1
1	0	0	1	A2C3 $_1$	A2C2 $_0$	A2C1 $_0$	A2C0 $_0$	ATT2
1	0	1	0	A3C3 $_1$	A3C2 $_0$	A3C1 $_0$	A3C0 $_0$	ATT3
1	0	1	1	A4C3 $_1$	A4C2 $_0$	A4C1 $_0$	A4C0 $_0$	ATT4
1	1	0	0	A5C3 $_1$	A5C2 $_0$	A5C1 $_0$	A5C0 $_0$	ATT5
1	1	0	1					
1	1	1	0					
1	1	1	1					

Address Data

Note) The state ("0" or "1") prevailing upon data reset (XDR="Low") is indicated at the lower right-hand corner of above table columns.

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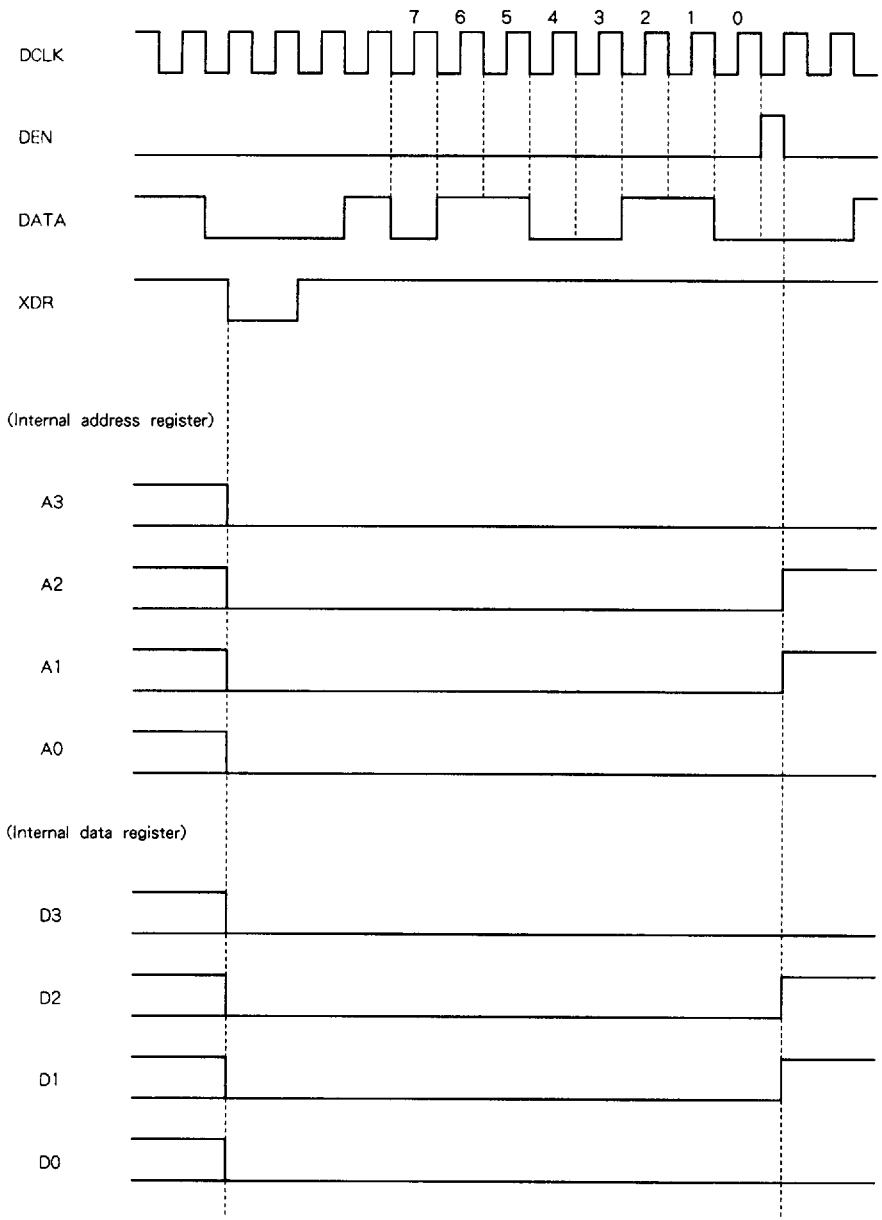
Control Data Description

Data name	Description
AT	AMPS/DOC system is used at "High"; TACS/N-TACS system is used at "Low"
SPLT	Input through LIMOUT at "High" to evaluate the splatter filter characteristics
BYPS	Compander is bypassed at "High"
RAM	Received voice is muted at "High"
TAM	Transmitted voice is muted at "High"
DS	WBD transmitted at "High"; ST/STA transmitted at "Low"
GAIN1	Gain control of transmitted data summing input. TDAMP2 input switch opens at "High".
GAIN2	Gain control of transmitted data summing amplifier. TSUMIN2 input switch opens at "High".
GAIN3	Gain control of transmitted data summing amplifier. TSUMIN3 input switch opens at "High".
STD	Power save mode at "High". (However, the data reception block operates at all times.)
STN	N-TACS data processing block in standby mode at "High"
V1ST	VOLUME1 in standby mode at "High"
V2ST	VOLUME2 in standby mode at "High"
V1C2 to V1C0	VOLUME1 gain control (3-bit control; MSB: V1C2)
V2C2 to V2C0	VOLUME2 gain control (3-bit control; MSB: V2C2)
A1C3 to A1C0	ATT1 gain control (4-bit control; MSB: A1C3)
A2C3 to A2C0	ATT2 gain control (4-bit control; MSB: A2C3)
A3C3 to A3C0	ATT3 gain control (4-bit control; MSB: A3C3)
A4C3 to A4C0	ATT4 gain control (4-bit control; MSB: A4C3)
A5C3 to A5C0	ATT5 gain control (4-bit control; MSB: A5C3)

Serial Data Timing Chart



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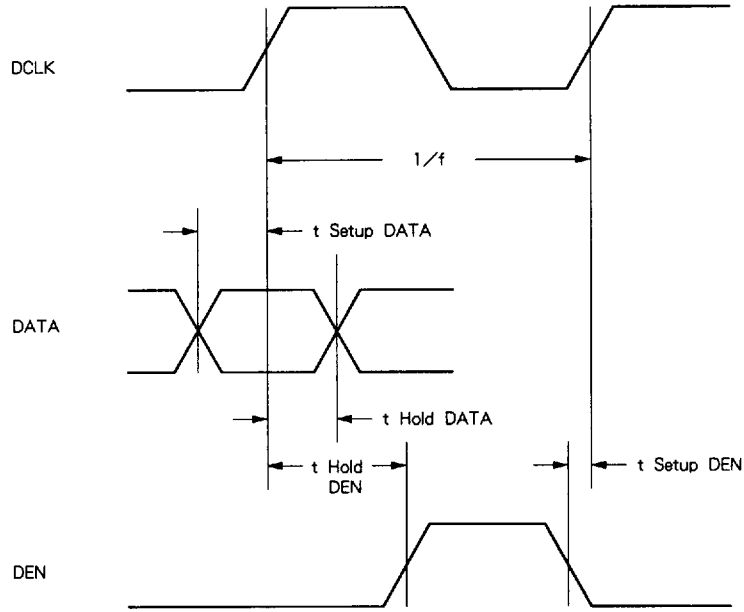
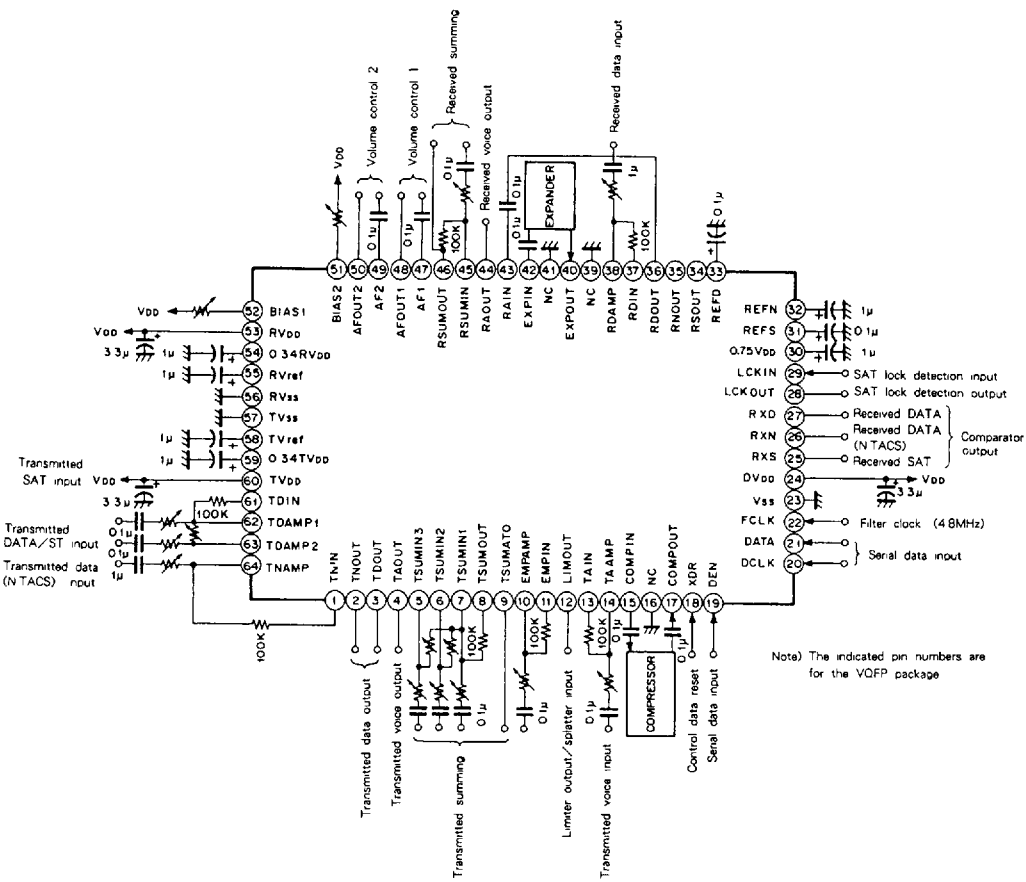
Serial Data Switching Characteristics



Item	Symbol	Min.	Typ.	Max.	Unit
DATA setup time	t Setup DATA	500	—	—	ns
DATA hold time	t Hold DATA	500	—	—	ns
DEN setup time	t Setup DEN	100	—	—	ns
DEN hold time	t Hold DEN	500	—	—	ns
DCLK frequency	f	—	—	1.2	MHz

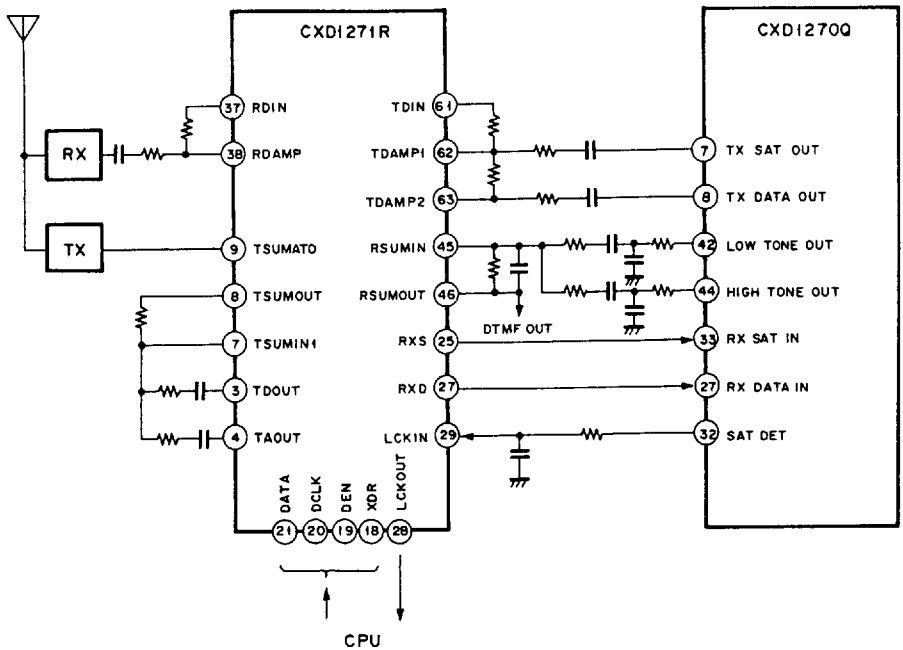
Application Circuit



Note) The indicated pin numbers are for the VQFP package

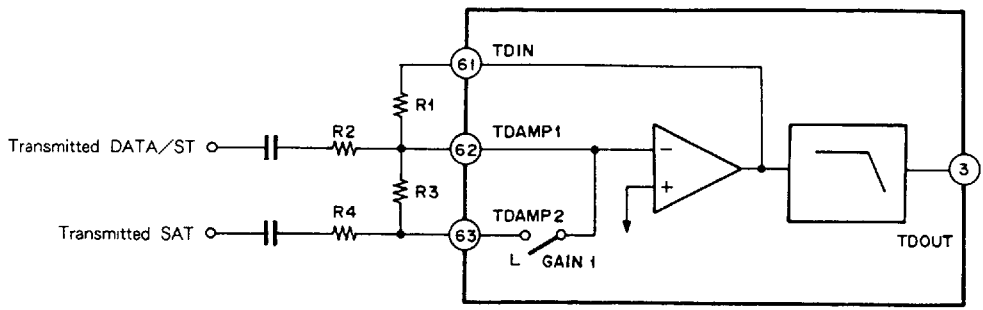
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

CXD1271R – CXD1270Q Connection Example



Notes on Operation

1. Transmitted Data Summing Amplifier Gain Adjustment



Note) The indicated pin numbers are for the VQFP package

Resistors R2 and R1 in the above circuit adjust the transmitted SAT attenuation, whereas resistors R4, R3, and R1 adjust the transmitted DATA/ST attenuation. The recommended amount of attenuation is –20dB. Further, the transmitted output level difference between the DATA and ST is compensated for by the Resistor R3.

For ST transmission, the GAIN1 data is set to "Low" to raise the gain. For DATA transmission, the GAIN1 data is set to "High" to lower the gain.

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2. Cellular System Setup and Transmitted Data Changeover

The data filter cutoff frequency is controlled to match the employed cellular system and transmitted data. For this control, the AT and DS control data are used.

Transmitted data / Cellular system	WBD	ST, SAT
AMPS, DOC	AT=H DS=H	AT=H DS=L
TACS, N-TACS	AT=L DS=H	AT=L DS=L

3. Standby Control

Standby control is exercised independently by the "STD", "STN", "V1ST", "V2ST" control data.

Control data	Control block	"H"	"L"
STD	Blocks other than VOLUME1, VOLUME2, and N-TACS data processing blocks	Only blocks up to RDAMP-RXD, and the RVref generator circuit are active	Active
STN	N-TACS data processing block (fc=0.2kHz, sixth-order LPF)	Standby	Active
V1ST	VOLUME1	Standby	Active
V2ST	VOLUME2	Standby	Active

Note) The condition in which STD="High" and STN="Low" is strictly prohibited.

4. Output Voltage Range and Supply Current Adjustment

The CXD1271Q/R varies its output level range and supply current depending on the BIAS resistor (resistor connected between the BIAS1 and RV_{DD} pins).

The data presented under Electrical Characteristics are obtained at a BIAS resistance of 500kΩ with 10kΩ output load.

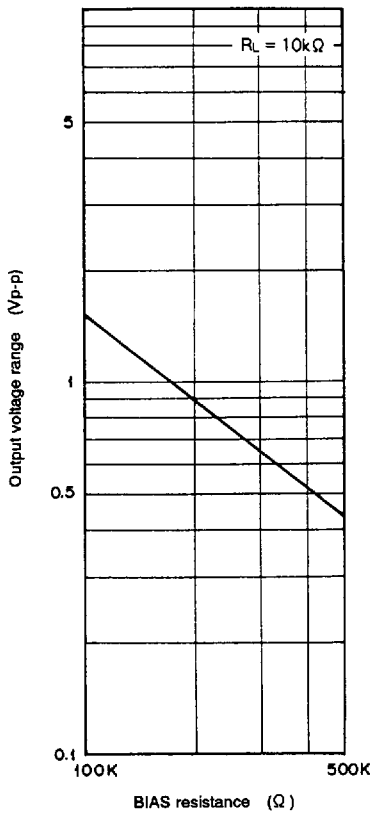
As the BIAS resistance determines the internal operational amplifier bias current, decreasing the BIAS resistance enlarges the output level range and supply current, and increasing the BIAS resistance reduces the output level range and supply current.

Therefore, the output voltage range and supply current can be adjusted as desired by varying the BIAS resistance.

For reference, the relation between the BIAS resistance and output level range/supply current is indicated below (V_{DD}=5V, load resistance=10kΩ).

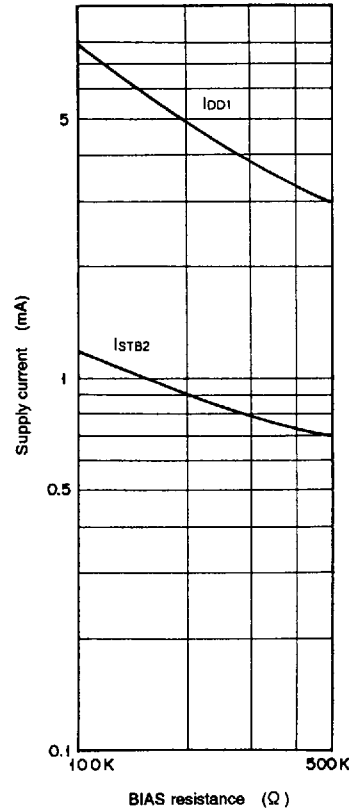
(BIAS1)

BIAS resistance vs. Output voltage range



(BIAS1)

BIAS resistance vs. Supply current



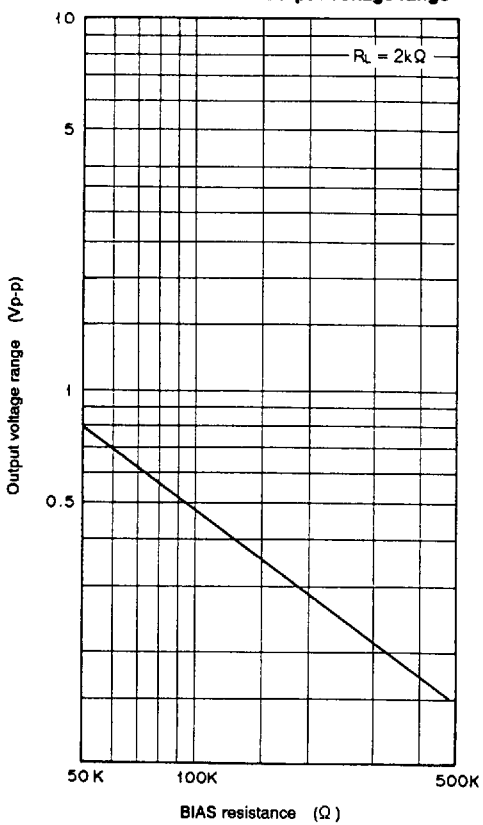
5. High-load Operational Amplifier Output Voltage Range Adjustment

As stated in the preceding section, the output voltage range can be adjusted by varying the BIAS resistance. However, the output voltage range of the receiver system summing amplifier (RSUMIN-RSUMOUT) can be independently varied by adjusting the other BIAS resistance (connected between the BIAS2 and RV_{DD} pins). This feature is convenient in driving a heavy load without significantly affecting the supply current.

For reference, the relationship between the BIAS resistance and output voltage range is indicated below (V_{DD}=5V, load resistance=2kΩ).

(BIAS2)

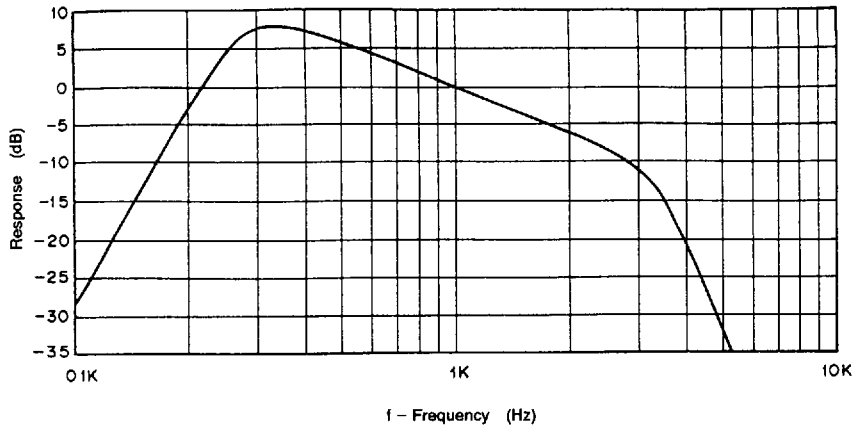
BIAS resistance vs. Output voltage range



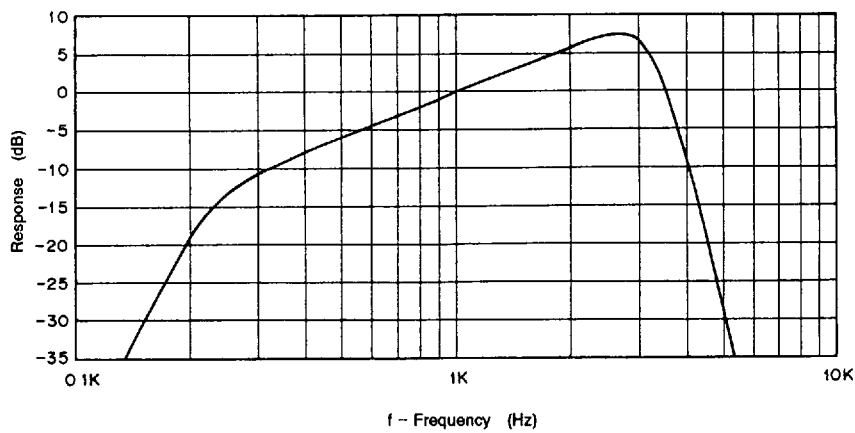
4

Filter Characteristics

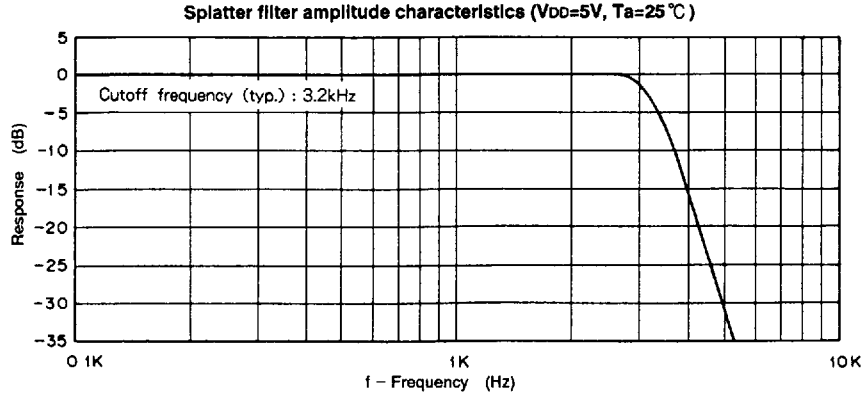
Received voice filter amplitude characteristic (V_{DD}=5V, Ta=25℃)



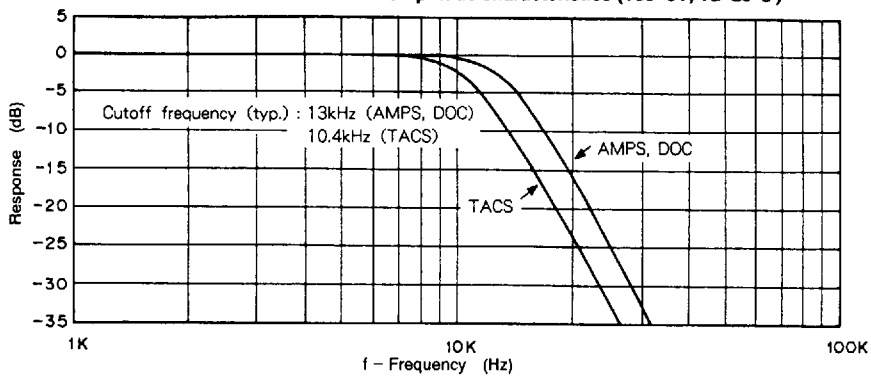
Transmitted voice filter (splatter filter included) amplitude characteristics (V_{DD}=5V, Ta=25℃)



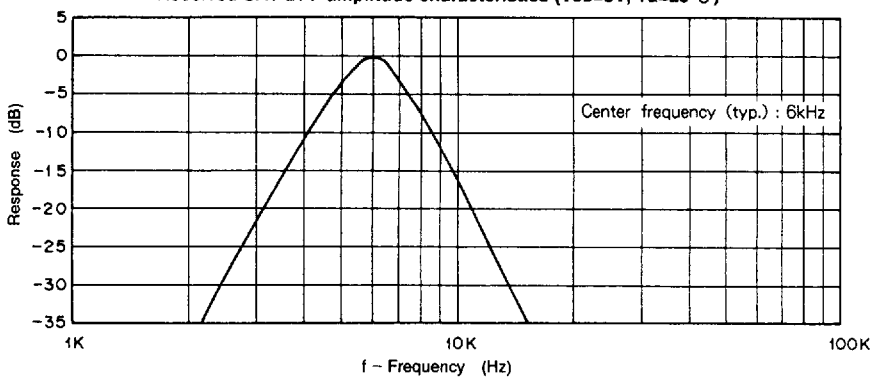
Splatter filter amplitude characteristics (V_{DD}=5V, Ta=25℃)



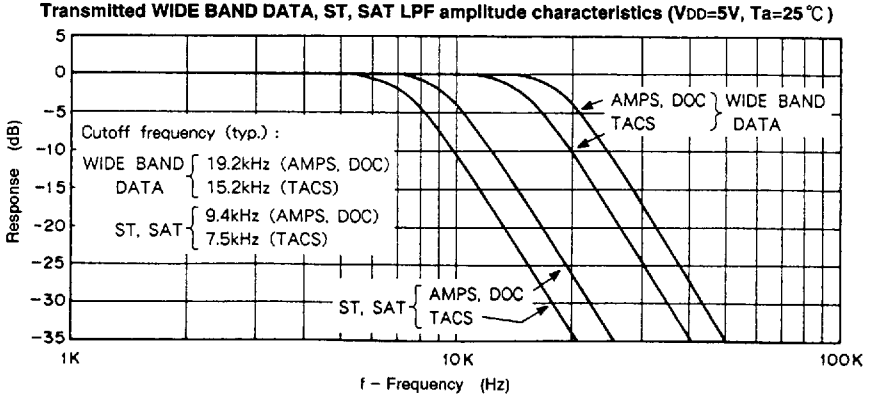
Received WIDE BAND DATA LPF amplitude characteristics (V_{DD}=5V, Ta=25℃)



Received SAT BPF amplitude characteristics (V_{DD}=5V, Ta=25℃)



Transmitted WIDE BAND DATA, ST, SAT LPF amplitude characteristics (V_{DD}=5V, Ta=25℃)



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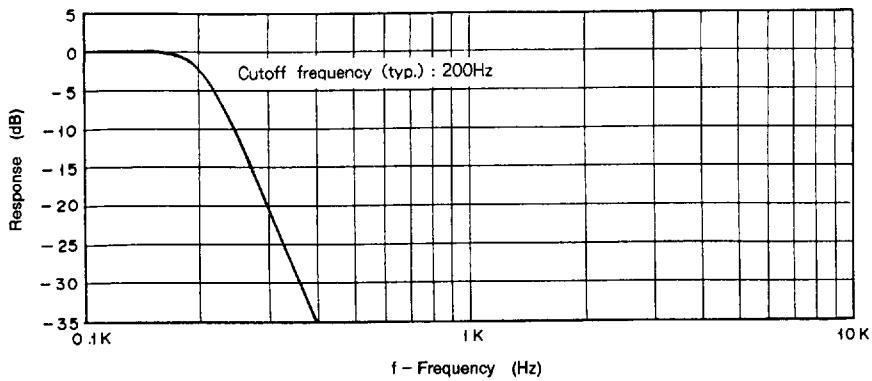
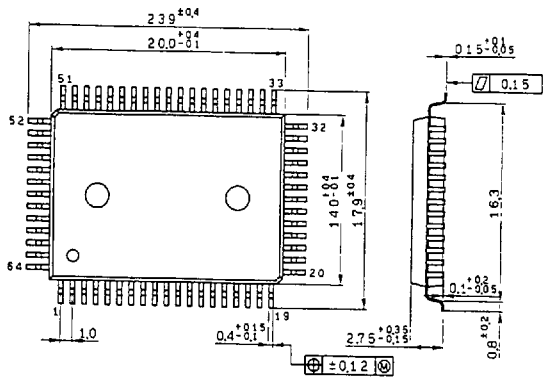
Received/Transmitted N-TACS data LPF amplitude characteristics (V_{DD}=5V, Ta=25°C)



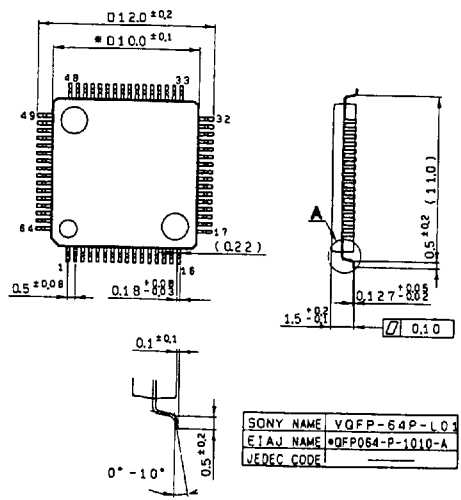
Package Outline Unit : mm

CXD1271Q 64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	———

CXD1271R 64pin VQFP (Plastic) 0.3g



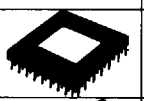
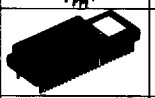
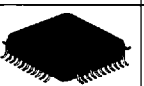
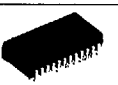
SONY NAME	VQFP-64P-L01
EIAJ NAME	*QFP064-P-1010-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue

4

Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C···Ceramic

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