

CAT27256 OTP

32,768 x 8-BIT ONE-TIME PROGRAMMABLE ROM

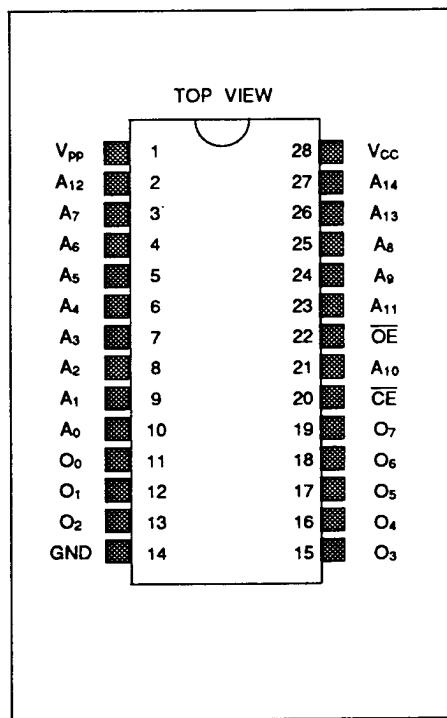
DESCRIPTION

The CAT27256 is a 32,768x8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27256 allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT27256 is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC-approved package.

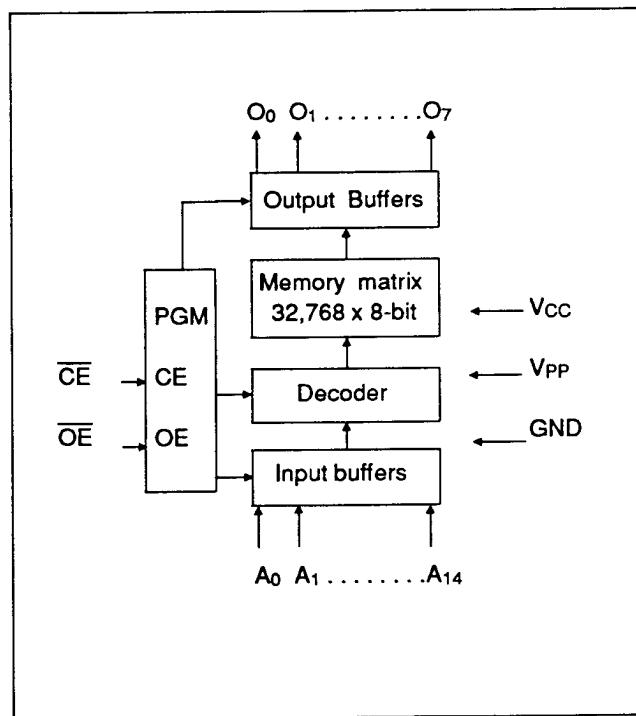
FEATURES

- 5V single power supply
- 32,768 words x 8-bit configuration
- Access time:
 - 170ns max (CAT27256-17)
 - 200ns max (CAT27256-20)
 - 250ns max (CAT27256-25)
- Power consumption:
 - Active: 100mA max
 - Standby: 35mA max
- Fully static operation
- TTL compatible Input/Output (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

Mode	Pins	\overline{CE} (20)	\overline{OE} (22)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V _{IL}	V _{IL}		+5V	+5V	D _{OUT}
Output disable	V _{IL}	V _{IH}		+5V	+5V	High impedance
Standby	V _{IH}	-		+5V	+5V	High impedance
Program	V _{IL}	V _{IH}		+12.5V	+6V	D _{IN}
Program verify	V _{IH}	V _{IL}		+12.5V	+6V	D _{OUT}
Program inhibit	V _{IH}	V _{IH}		+12.5V	+6V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	0°C ~ 70 °C
Storage temperature	- 55°C ~ 125 °C
All input/output voltages	- 0.6 ~ 13.5V
V _{CC} supply voltage	- 0.6V ~ 7V
Program Voltage	- 0.6 ~ 14V
Power assembly voltage	1.5W

(Voltages with respect to ground)

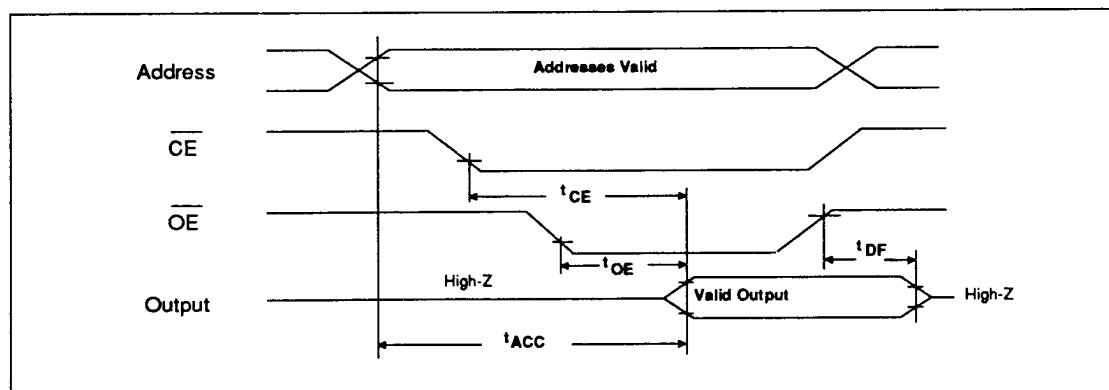
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>(V_{CC} = 5V ± 5%, V_{PP} = V_{CC} voltages with respect to ground, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I _{LI}	Input leakage current	V _{IN} = 5.25V	-	-	10	µA
I _{LO}	Output leakage current	V _{OUT} = 5.25V	-	-	10	µA
I _{CC1}	V _{CC} power current (standby)	CE = V _{IH}	-	-	35	mA
I _{CC2}	V _{CC} power current (operation)	CE = V _{IL}	-	-	100	mA
I _{PP1}	Program power current	V _{PP} = V _{CC}	-	-	5	mA
V _{IH}	Input voltage "H" level	-	2.0	-	V _{CC} +1	V
V _{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V _{OH}	Output voltage "H" level	I _{OH} = -400µA	2.4	-	-	V
V _{OL}	Output voltage "L" level	I _{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, PGM = V_{IH}, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	27256-17		27256-20		27256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{ACC}	Address access time	CE = OE = V _{IL}	-	170	-	200	-	250	ns
t _{CE}	CE access time	OE = V _{IL}	-	170	-	200	-	250	ns
t _{OE}	OE access time	CE = V _{IL}	-	60	-	75	-	100	ns
t _{DF}	Output disable time	CE = V _{IL}	0	50	0	55	0	60	ns

TIMING <Read Operation>

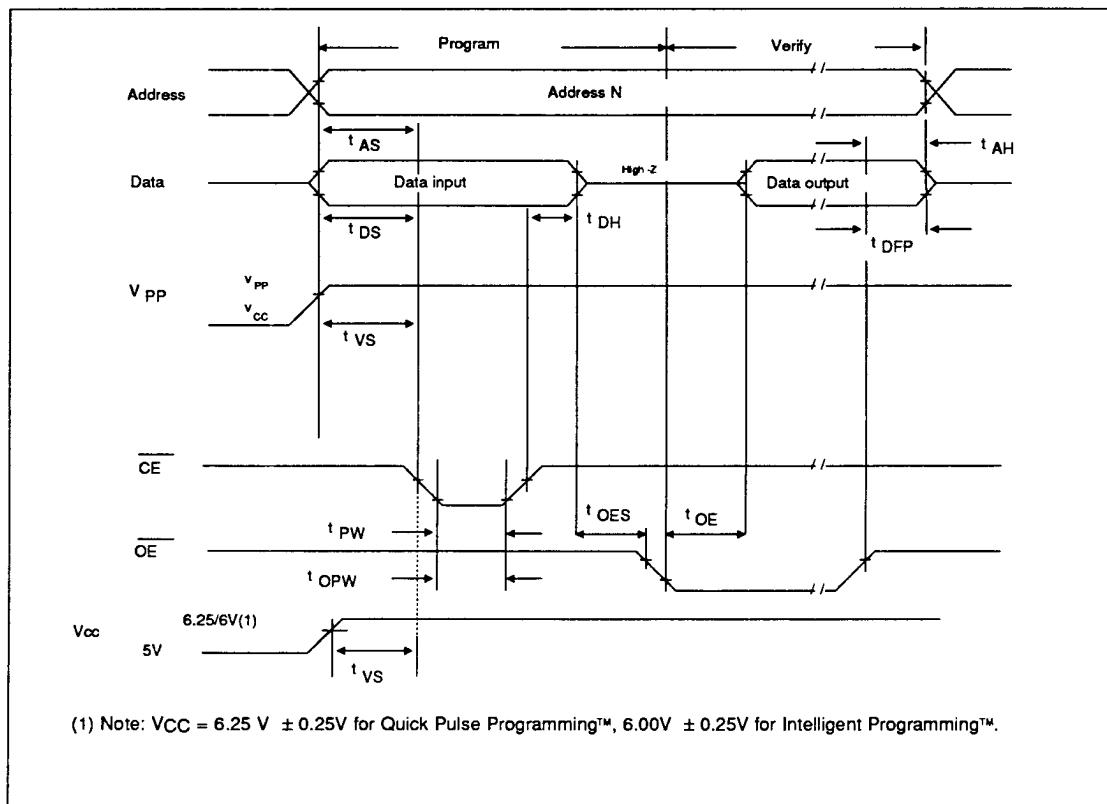
DC CHARACTERISTICS <Programming Operation>(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{LI}	Input leakage current	V _{IN} = 5.25V	-	-	10	µA
I _{PP}	V _{PP} power current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	-	50	mA
I _{CC}	V _{CC} power current	-	-	-	100	mA
V _{IH}	Input voltage "H" level	-	2.0	-	V _{CC} +1	V
V _{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V _{OH}	Output voltage "H" level	I _{OH} = -400µA	2.4	-	-	V
V _{OL}	Output voltage "L" level	I _{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{AS}	Address set-up time	-	2	-	-	µs
t _{OE}	\overline{OE} set-up time	-	2	-	-	µs
t _{DS}	Data set-up time	-	2	-	-	µs
t _{AH}	Address hold time	-	0	-	-	µs
t _{DH}	Data hold time	-	2	-	-	µs
t _{DPF}	Output enable to output float delay	-	0	-	130	ns
t _{VS}	V _{PP} power set-up times	-	2	-	-	µs
t _{PW}	\overline{CE} initial program pulse width	V _{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
t _{PW}	\overline{CE} program pulse width	V _{CC} = 6.25V ± 0.25V	95	100	105	µs
t _{OPW}	\overline{CE} overprogram pulse width	V _{CC} = 6V ± 0.25V	2.85	-	78.75	ms
t _{OE}	Data valid from \overline{OE}	-	-	-	150	ns
t _{OE}	Data valid from \overline{OE}	-	-	-	150	ns

TIMING <Programming Operation>



Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, outputs are disabled ($\overline{OE} = V_{IL}$), and a program write pulse must be applied to the CE pin. After the program write pulse the programmed data may be

verified by enabling the outputs ($\overline{OE} = V_{IL}$) and comparing the written data to the read data. This device is compatible with the Intelligent Programming™ algorithm, and the Quick Pulse Programming™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.