BLF6G10L-260PRN; BLF6G10LS-260PRN

Power LDMOS transistor

Rev. 1 — 12 August 2010 Product data sheet

1. Product profile

1.1 General description

260 W LDMOS power transistor for base station applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	920 to 960	28	40	22.0	26.5	−39[1]

[1] Test signal: 3GPP test model 1; 1 to 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

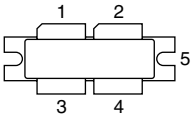
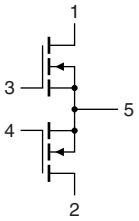
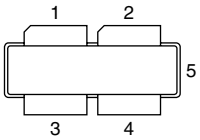
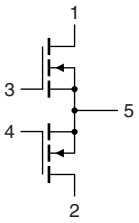
- Typical 2-carrier W-CDMA performance at frequencies of 920 MHz and 960 MHz, a supply voltage of 28 V and an I_{Dq} of 1800 mA:
  - Average output power = 40 W
  - Power gain = 22.0 dB
  - Efficiency = 26.5 %
  - ACPR = −39 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE, W-CDMA and CDMA base stations and multi carrier applications in the 700 MHz to 1000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF6G10L-260PRN (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF6G10LS-260PRN (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G10L-260PRN	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF6G10LS-260PRN	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	64	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 40 W	0.28	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C; values per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1000 mA	1.45	2.1	2.55	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	24.1	30	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	7.02	12	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	0.053	0.1	0.165	Ω

7. Application information

Table 7. 2-carrier W-CDMA Application information

Class-AB production test circuit; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 917.5 MHz; f_2 = 922.5 MHz; f_3 = 957.5 MHz; f_4 = 962.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1800 mA; T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	40	-	W
G_p	power gain	$P_{L(AV)}$ = 40 W	19.8	22.0	-	dB

Table 7. 2-carrier W-CDMA Application information *...continued*

Class-AB production test circuit; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 917.5 MHz; f_2 = 922.5 MHz; f_3 = 957.5 MHz; f_4 = 962.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1800 mA; T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL_{in}	input return loss	$P_{L(AV)}$ = 40 W	-	–10.0	–6.0	dB
η_D	drain efficiency	$P_{L(AV)}$ = 40 W	25.0	26.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 40 W	-	–39	–35	dBc

Table 8. 1 carrier W-CDMA Application information

Class-AB production test circuit; PAR 7.5 dB at 0.01 % probability on CCDF; 3 GPP test model 1; 1 to 64 DPCH; f_1 = 960 MHz; RF performance at VDS = 28 V; I_{dq} 1800 mA; T_{case} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_0	output peak-to-average ratio	PL(AV) = 125 W at 0.01 % probability on CCDF	3.8	4.3	-	dB

7.1 Ruggedness in class-AB operation

The BLF6G10L-260PRN and BLF6G10L-260PRN are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1800 mA; P_L = 260 W (CW); f = 920 MHz to 960 MHz.

7.2 Impedance information

Table 9. Typical impedance per section

I_{Dq} = 950 mA; main transistor V_{DS} = 28 V

f MHz	Z_S[1] Ω	Z_L[1] Ω
920	0.7 – j1.0	1.4 + j0.6
940	1.1 – j1.3	1.2 + j0.5
960	1.0 – j1.6	1.2 + j0.3

[1] Z_S and Z_L defined in Figure 1.

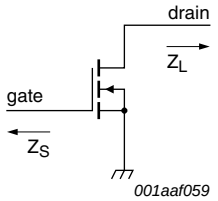
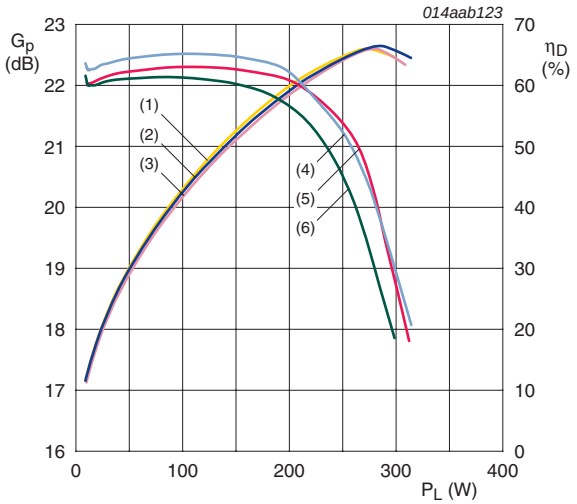


Fig 1. Definition of transistor impedance

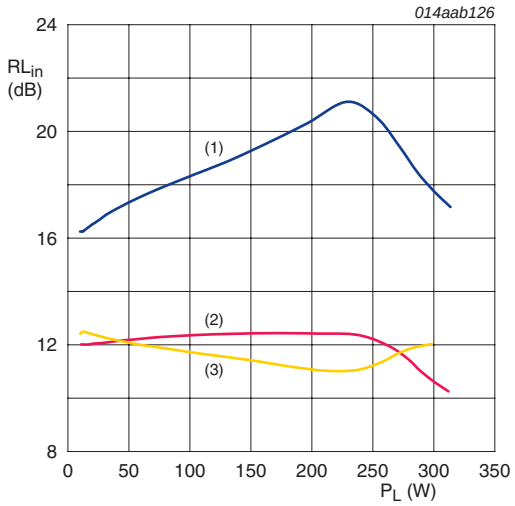
7.3 Typical powersweep

7.3.1 CW



(1) % efficiency at 960 MHz
(2) % efficiency at 940 MHz
(3) % efficiency at 920 MHz
(4) dB gain at 940 MHz
(5) dB gain at 920 MHz
(6) dB gain at 960 MHz

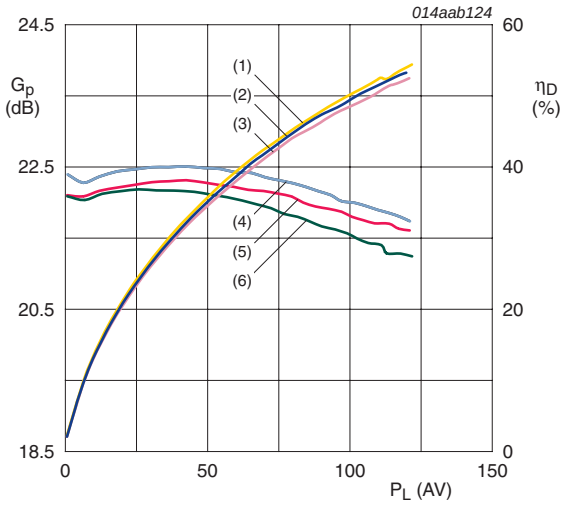
Fig 2. Typical continuous wave 1 (gain; efficiency versus P_O)



(1) dB return loss at 940 MHz
(2) dB return loss at 920 MHz
(3) dB return loss at 960 MHz

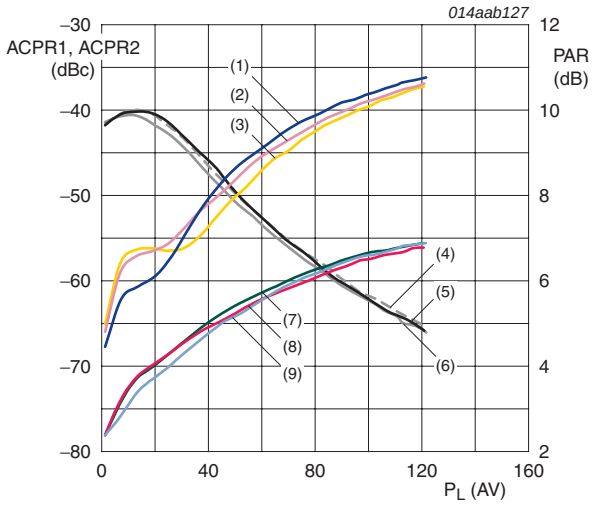
Fig 3. Typical continuous wave 2 (return loss versus P_O)

7.3.2 IS95



(1) % efficiency at 960 MHz
(2) % efficiency at 940 MHz
(3) % efficiency at 920 MHz
(4) dB gain at 940 MHz
(5) dB gain at 920 MHz
(6) dB gain at 960 MHz

a. Gain and efficiency versus P_O



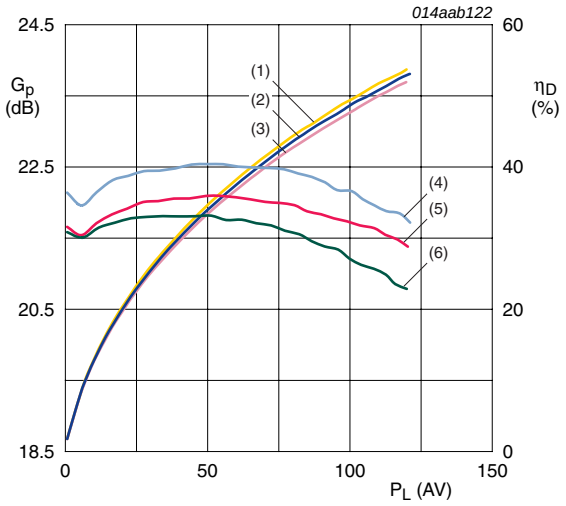
(1) 885 kHz ACPR1, dBc at 960 MHz
(2) 885 kHz ACPR1, dBc at 940 MHz
(3) 885 kHz ACPR1, dBc at 920 MHz
(4) PAR, dB at 940 MHz
(5) PAR, dB at 920 MHz
(6) PAR, dB at 960 MHz
(7) 1980 kHz ACPR2, dBc at 940 MHz
(8) 1980 kHz ACPR2, dBc 920 MHz
(9) 1980 kHz ACPR2, dBc at 960 MHz

b. ACPR1, ACPR2 and PAR versus P_O

IS95, PAR = 9.8 dB at 0.01% probability of the CCDF.

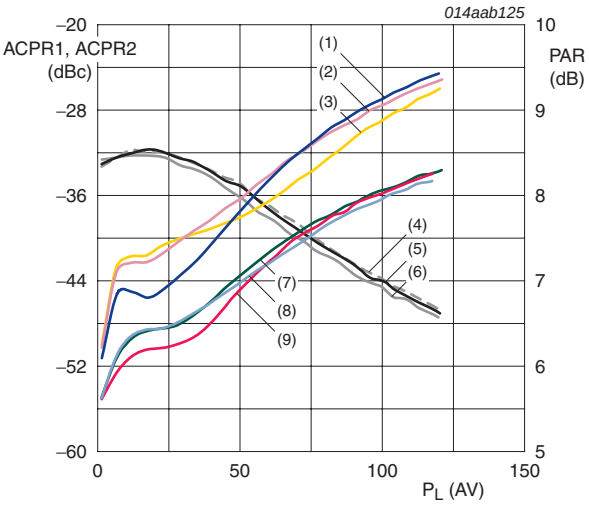
Fig 4. Typical IS95 (gain; efficiency; ACPR1, ACPR2 and PAR versus P_O)

7.3.3 2C-WCDMA (5 MHz spacing)



(1) % efficiency at 960 MHz
(2) % efficiency at 940 MHz
(3) % efficiency at 920 MHz
(4) dB gain at 940 MHz
(5) dB gain at 920 MHz
(6) dB gain at 960 MHz

a. Gain and efficiency versus P_O



(1) 5 MHz ACPR1, dBc at 960 MHz
(2) 5 MHz ACPR1, dBc at 940 MHz
(3) 5 MHz ACPR1, dBc at 920 MHz
(4) PAR, dB at 920 MHz
(5) PAR, dB at 940 MHz
(6) PAR, dB at 960 MHz
(7) 10 MHz ACPR2, dBc at 940 MHz
(8) 10 MHz ACPR2, dBc 920 MHz
(9) 10 MHz ACPR2, dBc at 960 MHz

b. ACPR1, ACPR2 and PAR versus P_O

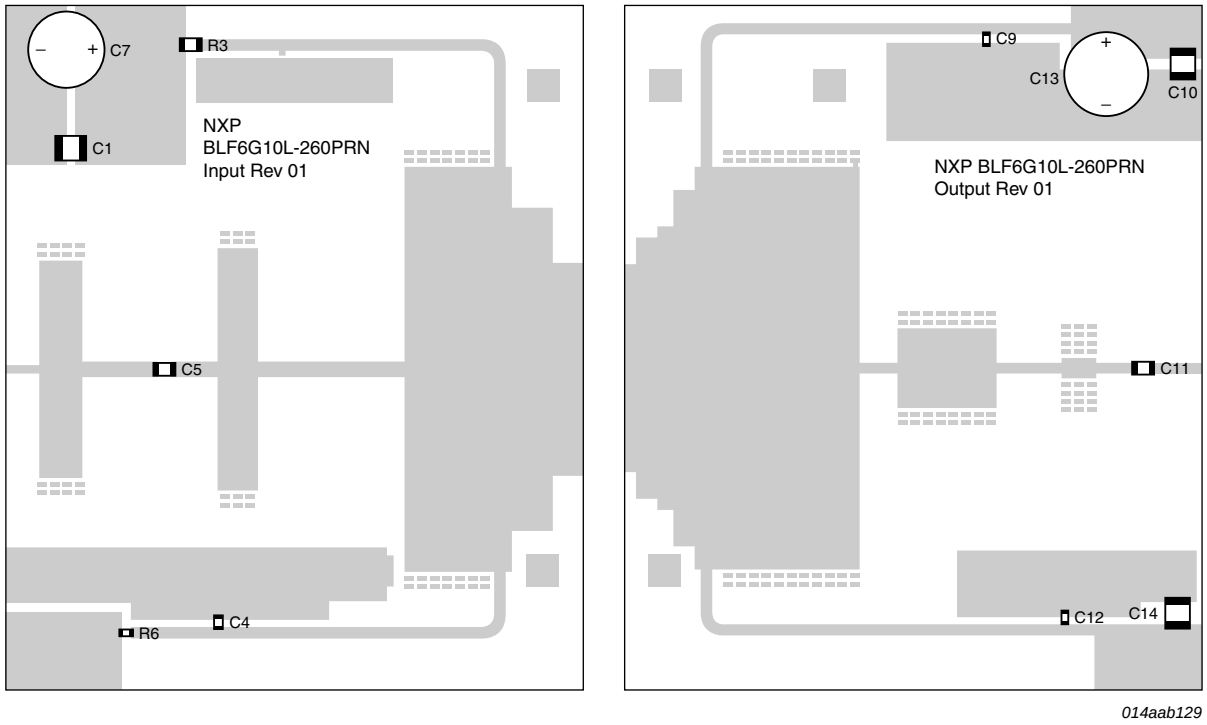
3GPP, Test Model 1, 64 DPCH, PAR=7.5 dB at 0.01% probability per carrier. 5 MHz carrier spacing.

Fig 5. Typical 2C-WCDMA (gain; efficiency; ACPR1, ACPR2 and PAR versus P_O)

8. Test information

8.1 Test circuit

Figure 6 shows the PCB test circuit layout



The above layout shows the test circuit used to measure the devices in production. The RF Power and Base-Stations group can provide a more appropriate application demonstration for specific customer needs.

Fig 6. Input and output test circuit PCBs'

8.2 Bill of materials (B.O.M.)

The following Bill of materials (Table 10) shows a list of all the components needed to build the RF test circuit.

Table 10. Bill of materials

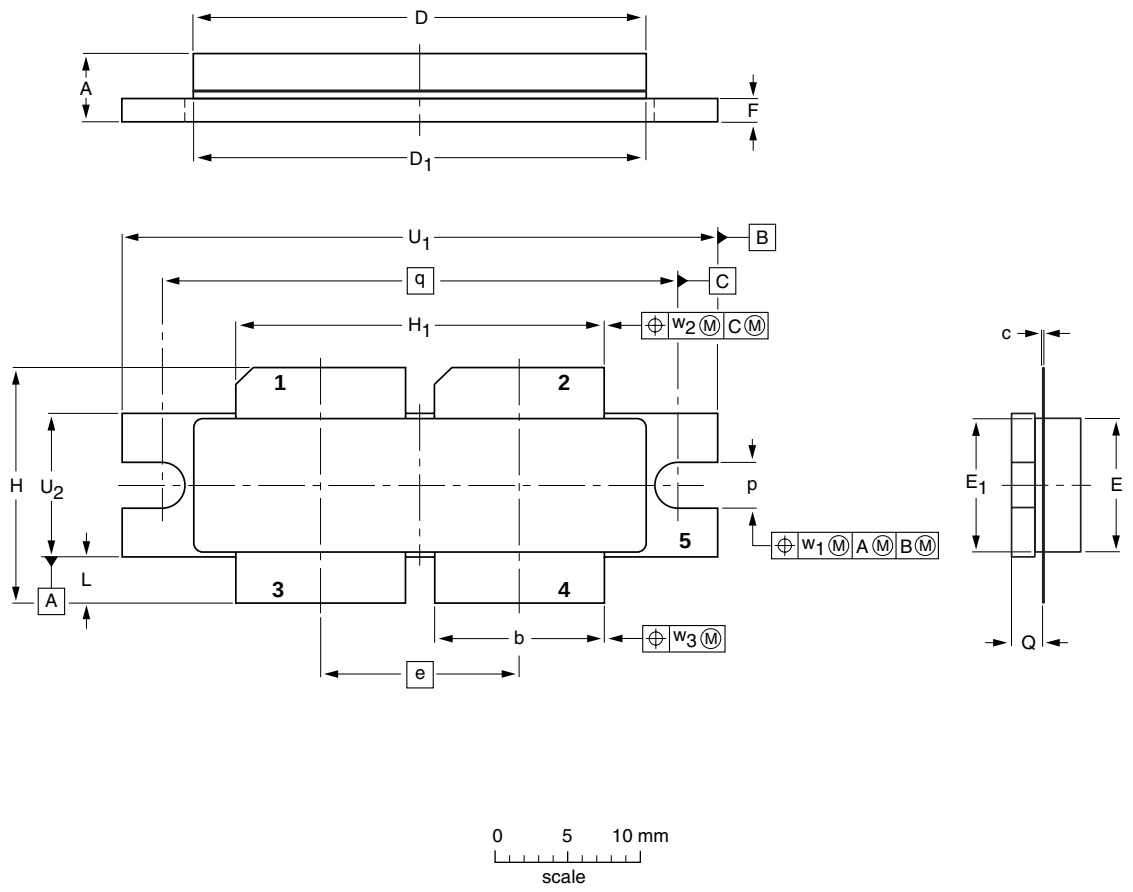
Component	Description	Type	Value	Code number	Remarks
	base plate				see mechanical drawing.
	input PCB				see PCB info.
	output PCB				see PCB info.
	15 × bolt M2				brass (nickel plated)
	15 × washer M2				brass (nickel plated)
	4 × contact block		12 × 4 mm		brass (milled)
	rubber O-ring	Viton	17 × 1 mm		
	conductive elastomer ("silver" rubber)	Chomerics	35 × 1 mm (2x)	CHO-SEAL 1273	

Table 10. Bill of materials *...continued*

Component	Description	Type	Value	Code number	Remarks
C4, C5, C9, C11, C12	multilayer ceramic chip capacitor	ATC 800B	100 pF		
	multilayer ceramic chip capacitor				
C1, C10, C14	multilayer ceramic chip capacitor	TDK	10 μF		
C7, C13	electrolytic capacitor		470 μF		
R3, R6	chip resistor	Philips 0603	10 Ω		
	copper foil strip				needed for tuning
	standard components:				
	N-connector male	13N-50-057/1			Suhner
	N-connector female	23N-50-057/1			Suhner
	4 × bolt M3		12 mm		chromium nickle steel
	4 × spring washer M3				chromium nickle steel
	DC-connector 8 pin male	8140-115			Souriau (Farnell)
	2 × DC-connector 2 pin male	8140-12			Souriau (Farnell)
	2 × bolt M3		30 mm		chromium nickle steel
	2 × washer M3				chromium nickle steel
	solid copper wire (diam. 1 mm)		30 mm		
	flexible copper wire	SIMX-F	0.75 mm^2		silicon isolated
	4 × cable isolator (diam. 3 mm)	P/H30X15WE		1922.000.10134	
	4 × cable isolator (diam. 2 mm)	P/H20X10WE		1922.000.10033	

9. Package outline

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

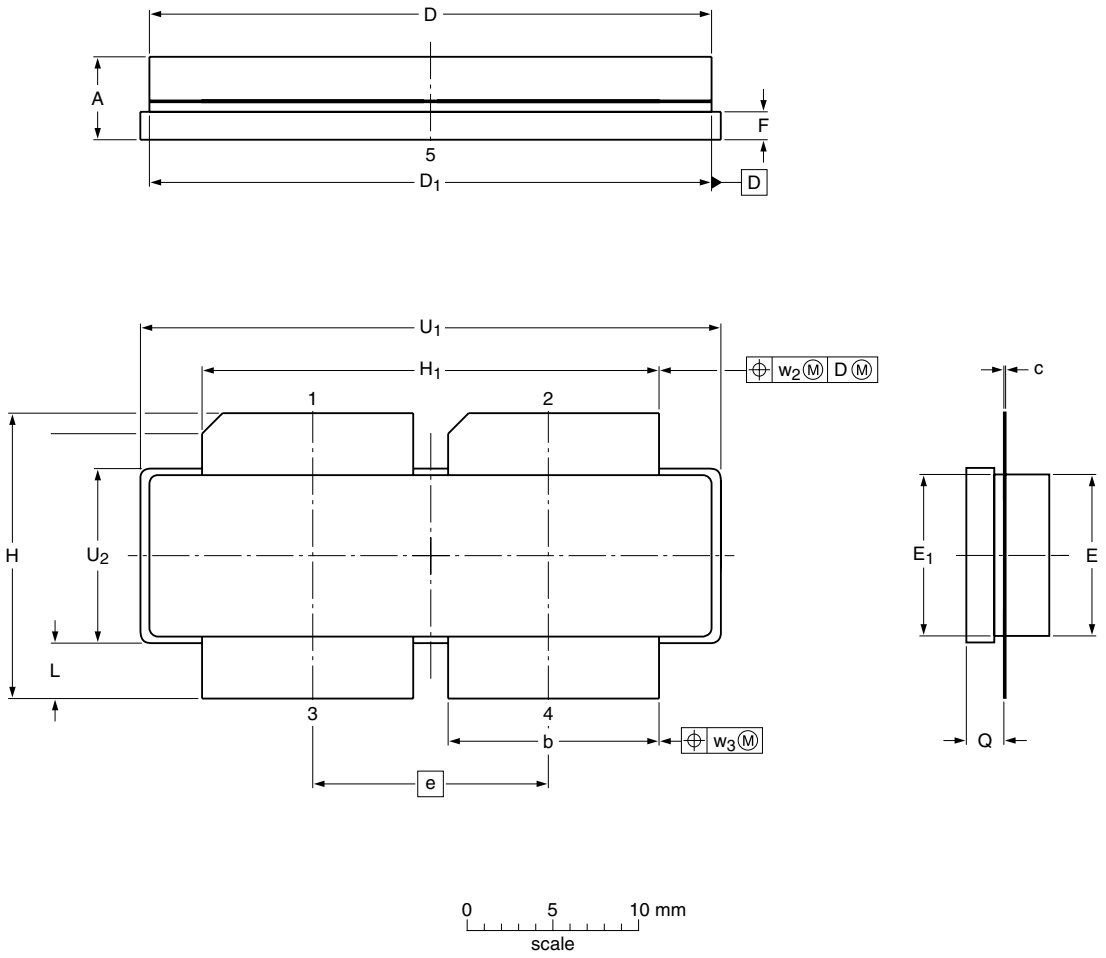
Note

1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~00-03-03~~ 10-02-02

Fig 7. Package outline SOT539A

Earless flanged balanced LDMOST ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.77	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
mm	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~09-10-16~~ 10-02-02

Fig 8. Package outline SOT539B

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G10L-260PRN_LS-260PRN v.1	20100812	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contact information

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