MSC8126 Design Checklist

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This application note provides a set of recommendations to assist you in a first-time design with the MSC8126 device. This document can also be useful as a general guideline for designing new systems because it highlights the aspects of a design that merit special attention during initial system start-up.

CONTENTS

1 Getting Started

During the first phase of designing a system with the MSC8126 device, your main tasks are to make the pin assignments and configure the reset parameters. Before you get started, you should be familiar with the available documentation, silicon revisions, software, models, and tools. Refer to **Section 9**, *Related Reading*, on page 18.

1.1 Pin Assignments

Some MSC8126 pins are multiplexed, depending on the device programming. Take care in programming MSC8126 registers to configure these multiplexed pins as needed for your system design. A signal function should be routed to a single pin, so any other pins providing that signal functionality should have it turned off. Pin multiplexing is configured in the following registers:

- Hard Reset Configuration Word (HRCW)
- SIU module configuration register (SIUMCR)
- Memory controller registers ORx and BRx
- GPIO port registers.

Some signals have one function during reset but switch to another multiplexed function during regular operation. These signals include SWTE, DSISYNC, DSI64, MODCK[1–2], and CNFGS. These signals switch to DSI functionality after the system exits the reset state.

Table 1 shows an overview of the multiplex options for the TDM interface, DSI bus, system bus, and Ethernet controller. The pins are chosen based on the settings of the DSI reset configuration pin, the ETHSEL bit in the Hard Reset Configuration Word, and the EN and IFMODE bits in the Ethernet MIIGSK configuration registers. There are two options for the location of the Ethernet pins: exposed on the low part of the DSI/system bus or exposed on the GPIO pins. Even though the pins are repeated in each option, the options cannot be mixed. All Ethernet pins must be from the DSI/system bus or from the GPIO pins. You cannot choose some of the Ethernet pins from the DSI/system bus and the others from the GPIO pins. The SMII mode of the Ethernet controller is available only on the GPIO pins. **Table 1** also indicates which TDMs are available on the GPIO pins when the different Ethernet options are chosen.

Table 1. Multiplexing Overview

Configuration				Pins				
DSI64 (Reset Pin)	ETHSEL (HRCW)	EN (MIIGSK_ENR)	IFMODE (MIIGSK_CFGR)	TDMs Available	DSI Bus Width	System Bus Width	Ethernet on DSI/System Bus	Ethernet on GPIO Pins
0	0	0	xx	0,1,2,3	32 bit	64 bit	—	—
0	0	1	00	0,1	32 bit	64 bit	—	MII
0	0	1	10	0,1,3	32 bit	64 bit	—	RMII
0	0	1	01	0,1,3	32 bit	64 bit	—	SMII
0	1	0	xx	0,1,2,3	32 bit	32 bit	—	—
0	1	1	00	0,1,2,3	32 bit	32 bit	MII	—
0	1	1	10	0,1,2,3	32 bit	32 bit	RMII	—
0	1	1	01	0,1,2,3	32 bit	32 bit	—	—
1	0	0	xx	0,1,2,3	64 bit	32 bit	—	—
1	0	1	00	0,1	64 bit	32 bit	—	MII
1	0	1	10	0,1,3	64 bit	32 bit	—	RMII
1	0	1	01	0,1,3	64 bit	32 bit	—	SMII
1	1	x	xx	0,1,2,3	64 bit	32 bit	—	—

1.2 Configuring Reset Parameters

Review the HRCW to determine initial power-on-reset parameters, such as single MSC8126 bus mode versus 60x–compatible bus mode, boot port size, and on, and then set the bits for your application (see **Table 2**).

Table 2. Hard Reset Configuration Word (HRCW)

Name	Reset	Description	Settings
EARB 0	0	**External Arbitration** Defines the initial value for ACR[EARB].	0 Internal arbitration is performed. 1 External arbitration is assumed.
EXMC 1	0	**External MEMC** Defines the initial value of BR0[EMEMC].	0 No external memory controller is assumed. 1 External memory controller is assumed.
INTOUT 2	0	**INT_OUT or $\overline{\text{IRQ7}}$ Selection** Defines the initial value of SIUMCR[INTOUT].	0 $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ is $\overline{\text{IRQ7}}$. 1 $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ is $\overline{\text{INT\_OUT}}$.
EBM 3	0	**External 60x-compatible Bus Mode** Defines the initial value of BCR[EBM].	0 Single MSC8126 bus mode. 1 60x-compatible bus mode.
BPS 4–5	00	**Boot Port Size** Defines the initial value of BR0[PS], the port size for memory controller bank 0.	00 64-bit port size. 01 8-bit port size. 10 16-bit port size. 11 32-bit port size.
SCDIS 6	0	**SC140 Cores Disabled** Enables/disables the SC140 cores.	0 SC140 cores enabled. 1 SC140 cores disabled.
ISPS 7	0	**Internal Space Port Size** Defines the initial value of BCR[ISPS]. Setting ISPS enables a 32-bit master to access the MSC8126 internal space.	0 MSC8126 acts as a 64-bit slave to external masters access to its internal space. 1 MSC8126 acts as a 32-bit slave to external masters access to its internal space.
IRPC 8	0	**Interrupt Pin Configuration** Defines the initial value of SIUMCR[IRPC].	0 $\overline{\text{IRQ2}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ5}}$ active. 1 BADDR29, BADDR30, BADDR31 active.
— 9	0	Reserved. Cleared to zero for future compatibility.	
DPPC 10–11	00	**Data Parity Pin Configuration** Defines the initial value of SIUMCR[DPPC].	00 $\overline{\text{IRQ[1–7]}}$ active. 01 DP[0–7] active. 10 DREQ[1–4], $\overline{\text{DACK[1–4]}}$ active. 11 $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, and $\overline{\text{IRQ[6–7]}}$ active.
NMI OUT 12	0	**NMI OUT** Defines whether the host or one of the SC140 cores handles a non-maskable interrupt (NMI) event.	0 $\overline{\text{NMI}}$ is serviced by SC140 cores. 1 $\overline{\text{NMI}}$ is routed to $\overline{\text{NMI\_OUT}}$ and serviced by the external host.
ISBSEL 13–15	000	**Initial Internal Space Base Select** Defines the initial value of IMMR[ISB], which determines the base address of the internal memory space. The SC140 internal address space spans from 0x00000000–0x00FFFFFF (16 MB). Therefore it is not advisable to map the IMMR in this space, since the SC140s cannot access the SIU registers.	000 0xF0000000. 001 0xF0F00000. 010 0xFF000000. 011 0xFFF00000. 100 Reserved. This option should not be used. 101 Reserved. This option should not be used. 110 0x0F000000. 111 0x0FF00000.

Table 2. Hard Reset Configuration Word (HRCW) (Continued)

Name	Reset	Description	Settings
BBD 17	0	**Bus Busy Disable** Defines the initial value of SIUMCR[BBD].	0 $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ active. 1 $\overline{\text{IRQ}}$[4–5] active.
MMR 18	0	**Mask Masters Requests** Defines the initial value of SIUMCR[MMR].	0 No masking on bus request lines. 1 All external bus requests masked (boot master is the one of the internal cores).
ETHSEL 19	0	**Ethernet Select** Defines whether the Ethernet is exposed on the low part of the DSI/60x data bus lines (when ETHSEL is set and the DSI64 line is sampled low at reset) or the GPIO lines (when ETHSEL is clear).	
TTPC 20	0	**Transfer Type Pin Configuration** Defines the initial value of SIUMCR[TTPC].	0 TT[0, 2–4] active. 1 $\overline{\text{CS}}$[5–7] active.
CS5PC 21	0	**Chip Select 5 Pin Configuration** Defines the initial value of SIUMCR[CS5PC].	0 $\overline{\text{CS5}}$ active. 1 $\overline{\text{BCTL1}}$ active.
TCPC 22–23	0	**Transfer Code Pin Configuration** Defines the initial value of SIUMCR[TCPC].	00 TC[0–2] active. 10 BNKSEL[0–2] active.
LTLEND 24	0	**Little Endian** Defines the host Endian mode of operation.	0 Big-Endian. 1 Little-Endian.
PPCLE 25	0	**Munged Little Endian** When the LTLEND bit is set, PPCLE specifies whether the host is a Little-Endian host or a host that works in Munged Little-Endian mode.	0 True Little-Endian host. 1 Munged Little-Endian host.
— 26	0	Reserved. Cleared to zero for future compatibility.	
— 27	1	Reserved. Must be set to 1.	
MODCK[3–5] 28–30	0	**MODCK High Order Bits** High-order bits of the MODCK bus, which determine the clock reset configuration. Refer to the chapter on clocks in the *MSC8126 Reference Manual*.	
— 31	0	Reserved. Cleared to zero for future compatibility.	

2 Power

This section outlines the MSC8126 power supply and power consumption considerations. For information on AC/DC electrical specifications, thermal characteristics, start-up, and power sequencing, refer to the data sheet.

- *Power supply*. The MSC8126 has a core voltage, V_{DD}, that operates at a lower voltage than the I/O voltage V_{DDH}. You should supply the MSC8126 core voltage V_{DD} via a variable power supply (switching supply or regulator) to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied across V_{DD} and V_{SS} (GND). The core supply voltage must be between 1.14 V and 1.26 V for 400 MHz devices. The core supply voltage must be between 1.16 V and 1.24 V for 500 MHz devices.

The I/O section of the MSC8126 is supplied with 3.3 V (± 5%) across V_{DDH} and V_{SS} (GND). Typically, this voltage is supplied by a simple linear regulator, which increases system complexity because multiple power supplies are required for the design. External signals on the MSC8126 are not 5 V tolerant. All input signals must meet the V_{IN} DC spec (–0.2 V to V_{DDH} + 0.2). After the power-up sequence, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

For details on supply design considerations, consult the *MSC8126 Technical Data* sheet and the application note entitled *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937).

- *Power consumption.* The *MSC8126 Technical Data* sheet provides preliminary power dissipation estimates for various configurations. You can take the following steps to reduce power consumption in your design:
  - *Stop mode for SC140 cores*. Any SC140 core can be placed into Stop mode when it is not in use. However, the core can be taken out of Stop mode only through a device reset such as $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, or $\overline{\text{SRESET}}$.
  - *Wait mode for SC140 cores*. Any SC140 core can be placed into Wait mode when it is not in use. The SC140 core exits Wait mode when there is an interrupt request as well as a reset or debug request.
  - *CLKOUT disable*. If the system bus clock output is not needed in a system design, it can be masked by setting the SIUMCR[CLKOD] bit. Masking the clock output not only reduces power consumption but also noise in the design.
  - *Disable unused IP peripherals*. All IP bus peripherals have a control bit to mask their clock. Any unused peripherals should be programmed to Stop mode. For details, see the IPBus chapter of the *MSC8126 Reference Manual*.

3 Clocks

All inputs and outputs except those associated with a serial clock are referenced to REFCLK. There are two modes for clock distribution, Back-Compatibility (with the MSC8102 device) and PLL Skew Elimination mode. PLL Skew Elimination is the recommended mode. In this mode, the REFCLK is CLKIN, which is clocked by an on-board oscillator. The clock mode is determined by the clock mode settings, as follows:

- *MODCK[1–2]*. The MODCK[1–2] pins are sampled at the rising edge of $\overline{\text{PORESET}}$ while $\overline{\text{HRESET}}$ is still asserted. Their value can be set using pull-ups/pull-downs. Therefore, open collector drivers are not needed.
- *MODCK[3–5]*. MODCK[3–5] can be set in the HRCW, or you can take the default value. Collectively, the MODCK[3–5] and MODCK[1–2] fields define the multiplication of the input clock (CLKIN) to derive the SC140 core and system bus clock ratios. Note that the SPLL multiplication value is set only during an initial $\overline{\text{HRESET}}$ caused by a $\overline{\text{PORESET}}$, so the SPLL does not change during subsequent assertions of $\overline{\text{HRESET}}$.

Refer to the *MSC8126 Reference Manual* for the most up-to-date clock configuration mode tables.

4 Reset

This section describes the reset recommendations for configuring the MSC8126 device at reset.

4.1 Power-On-Reset Circuit

There is no power-up detector on the MSC8126 device. Optionally, a power-on-reset chip to monitor the power plane and drive $\overline{\text{PORESET}}$ can be used. $\overline{\text{PORESET}}$ must be asserted externally for at least 16 CLKIN cycles after external power to the MSC8126 reaches nominal value.

HRESET is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as HRESET, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC8126 output current, the pull-up value should not be too small (a 1 KΩ pull-up is used in the MSC8126ADS reference design).

SRESET is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. The MSC8126 device drives SRESET if the PORESET line or the HRESET line is asserted. A software watchdog time-out, bus monitor time-out, JTAG reset, or external soft reset can also drive SRESET.

4.2 Reset Configuration Pins

The default HRCW (0x00000000) can be taken by connecting CNFGS to 0 and RSTCONF to a logic 1 on the rising edge of PORESET. In this case, no accesses are made to the PROM connected to CS0. The default case for the device is single MSC8126 mode. If the configuration word is not written via the 60x system bus during 1024 CLKIN cycles, the MSC8126 gets the default configuration word value.

Initial values other than the default can be obtained by selecting a different combination for the CNFGS and RSTCONF pins. BCTL0 is active (functioning as W/R) during the HRCW write. Take care to avoid bus contention during this time if buffers on the board are under BCTL0 control. BCTL1 should not be used during the reset configuration procedure. **Table 3** shows the reset configuration mode options. For details, refer to the Reset chapter of the *MSC8126 Reference Manual*.

Table 3. Reset Configuration Modes

CNFGS, RSTCONF	Reset Configuration Word Source
00	Reset configuration via system bus. MSC8126 is the configuration master.
01	Reset configuration via system bus. MSC8126 is the configuration slave.
10	Reset configuration via write through DSI.
11	Reserved.

If both CNFGS and RSTCONF are pulled to logic 0 on the rising edge of PORESET, the MSC8126 device is a configuration master. The HRCW is read from the PROM connected to CS0 at addresses 0x00, 0x08, 0x10, and 0x18. These four bytes are written to the fields of the HRCW. The MSC8126 device can act as a configuration master to configure up to seven MSC810x configuration slaves by individually connecting the RSTCONF lines of up to seven slaves to the most significant seven address bits of the configuration master address bus. The master continues to read bytes starting at 0x20, configures the next slave while driving the RSTCONF line of the slave, and writes a 32-bit configuration word to that slave while the master drives the HRESET asserted to the slave. This process is repeated from addresses 0x40, 0x60, 0x80, 0xA0, 0xC0, and 0xE0 for the remaining six slaves. The configuration master drives the full 32-bit configuration word on the 60x data bus after each 4-byte read from the PROM. Avoid any contention on the bus that would affect the configuration word. No pull-ups are required on the address bus because it is actively driven during this operation.

If CNFGS is logic 1 and RSTCONF is pulled to logic 0 on the rising edge of PORESET, the MSC8126 slave can be configured to receive the HRCW via the DSI. The host drives the HCID[0–3] signals to indicate which MSC8126 slave it is configuring. These signals can be driven by the host address lines. Alternatively, the host can write the HRCW to all MSC8126 slaves at once using the host broadcast chip select (HBCS). The MSC8126 slave remains in reset state until it receives its HRCW.

4.3 Boot

The MSC8126 boots from memory on the system bus, a host on the system bus, a host via the direct slave interface (DSI), or via the time-division multiplexing module (TDM), universal asynchronous receiver/transmitter (UART), or I^2C ports. The boot source is determined by the state of the BM[0–2] signals sampled at the rising edge of $\overline{\text{PORESET}}$ (see **Table 4**).

Table 4. Boot Mode Settings

BM[0]	BM[1]	BM[2]	Boot Sequence
0	0	0	External Memory on the system bus
0	0	1	External host via DSI or system bus
0	1	0	TDM
0	1	1	UART
1	0	0	I^2C
1	0	1	Reserved
1	1	x	Reserved

The MSC8126 device boots from memory that is 8-, 16-, 32-, or 64-bits wide. When an internal memory controller is used, the memory should be attached to $\overline{\text{CS0}}$, which functions as the global boot select, and be of a type that the GPCM machine controls (EPROM or Flash memory). The HRCW[BPS] bit sets the width of the $\overline{\text{CS0}}$ space. After configuration, SC140 core 0 fetches the address of the boot routine from location 0xFE000110.

If the MSC8126 device boots from a host via the DSI or 60x system bus interface, the host polls the BR10[V] bit to determine when the boot program is finished. The host then begins its initialization procedure by loading code and data to the MSC8126 device. Then it notifies the MSC8126 by sending VIRQ1 to SC140 core 0.

If the MSC8126 device boots via the TDM, the TDM boot master writes blocks of code and data into MSC8126 internal memory. The transaction requires the TDM physical layer to be set up and the TDM logical layer handshake to be implemented. The boot master transmits messages to a single MSC8126 or multiple MSC8126 devices on TDM channel 0. The MSC8126 slave devices transmit back to the host on the TDM channel associated with their CHIP_ID. When the TDM session is complete, the valid bit of Bank 10 (BR10) is set to 1.

If the MSC8126 device boots from a UART device, a UART boot master writes blocks of code and data into MSC8126 internal memory. Like the TDM boot option, the transaction requires set up of the physical layer and a UART logical layer handshake. When the UART session is complete, the valid bit of Bank 10 (BR10) is set to 1.

If the MSC8126 device boots from an I^2C slave memory device, it retrieves blocks of code from an external I^2C device such as a serial EPROM. At the end of the I^2C process, all SC140 cores jump to address 0x0 of their M1 memory.

For the boot via TDM, UART, and I^2C options, the boot code configures the GPIO pin multiplexing as required for external communication to boot in these modes. As a result, these GPIO configurations become the default pin multiplexing option for the affected signals. For details, see the “Boot Program” chapter of the *MSC8126 Reference Manual*.

5 Bit and Byte Lane Ordering

This section describes the system bus bit and byte lane ordering:

- *Address/data nomenclature*. It is recommended that schematics use documented terminology for the system bus as defined the chapter on "External Signals," in the *MSC8126 Technical Data* sheet.
- *System bus*. The highest-order address bit is A0. The lowest-order address bit is A[31]. All 32 address pins are valid in a byte access. In a 64-bit access, only the upper 29 A[0–28] address pins are valid, and A[29–31] are driven low. For the 60x data bus, the highest-order data bit is D0 and the lowest order data bit is D63.
- *Data byte lane ordering*. D[0–7] is the highest-order byte lane on the data bus, and D0 is the highest-order bit of that byte lane. D[0–7] corresponds to write enable 0 ($\overline{\text{PWE0}}$) and byte lane select 0 ($\overline{\text{PSDDQM0}}$). **Table 5** provides the data byte lane ordering for both the system bus and local bus.

Table 5. 60x Bus Data Byte Lane Ordering

Data Bus Signals	Byte Lane	External Pins (Byte Lane Select)
D[0–7]	0	$\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$
D[8–15]	1	$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$
D[16–23]	2	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$
D[24–31]	3	$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$
D[32–39]	4	$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
D[40–47]	5	$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$
D[48–55]	6	$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
D[56–63]	7	$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$

- *Memory controller byte lanes*. The memory controllers can access memories that are 8-, 16-, 32-, and 64-bits wide without creating any "holes" in the memory space on the system bus. All memories should be placed into the most significant byte lanes as shown in **Table 6**.

Table 6. Byte Lanes for Memory Widths

Memory Width	Byte Lanes
Byte (8-bits)	0
2 Bytes (16-bits)	0, 1
4 Bytes (32-bits)	0, 1, 2, 3
8 Bytes (64-bits)	0, 1, 2, 3, 4, 5, 6, 7

- *Flash Memory Devices*. The data lines of most Flash memory devices connect to the MSC8126 with byte lanes bit-reversed for programming algorithm purposes. A 32-bit example is shown in **Figure 1**. The figure is correct for a Flash SIMM composed of 8-bit Flash devices. Adjust the byte lanes as necessary for the memory in your design. The Flash memory interface requires a reset input that should connect to the MSC8126 $\overline{\text{PORESET}}$.

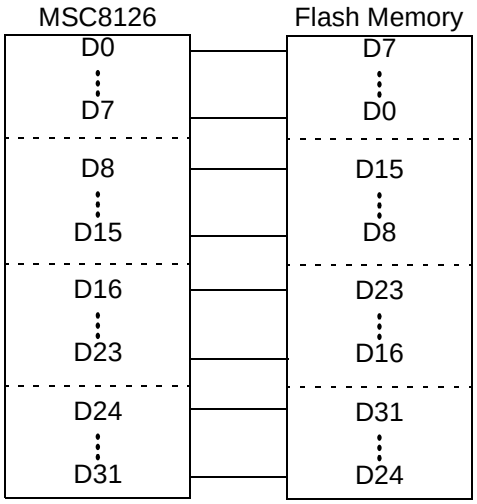

Figure 1. MSC8126 to Flash Memory Byte Lane Reversal

Bringing up a board with blank Flash memory and no host processor requires a switch or other method to force RSTCONF to a logic 1 and CNFGS to 0 to bring up the MSC8126 in the default state. Otherwise, invalid PLL values can be loaded. When the device comes out of reset in the default state, the Flash memory can be programmed. For subsequent resets, the RSTCONF and CNFGS signals can be set appropriately for resetting from Flash memory.

6 Memory

This section provides design considerations for the MSC8126 associated memories.

6.1 60x Bus Signals and Memory Transactions

The MSC8126 is not 5 V tolerant. All input signals must meet V_{IN} DC Spec (–0.2 V to V_{DDH} + 0.2).

- *Partial Data Valid*. The memory controller drives PSDVAL for an access to an MSC8126-controlled resource (internal space or chip-selects). PSDVAL is used only by external devices that implement the MSC8126 memory bank-based bus sizing protocol (for example, an external MSC8126). Devices that do not implement this memory bank-based bus sizing do not use PSDVAL.
- *Non-MSC8126 masters*. MSC8126 designs incorporating devices that do not implement the MSC8126 memory bank-based bus sizing protocol must either use 64-bit accesses on the system bus or ensure that only MSC8126-initiated transactions can access the 8-, 16-, or 32-bit memory mapped slaves on the system bus.
- *Write enable*. PWE[0–7] should be used to control the R/W lines of memories, due to timing flexibility. For buffer direction control, the BCTL[0–1] signals should be used.
- *Pipelining*. The bus can be pipelined up to two address cycles deep. For example, it can have a TS, an AACK, and another TS before the first TA. Because the address is valid only during the address phase ending with AACK, external latches and multiplexes are necessary for SDRAM, and so on. On accesses to internal slaves, as well as SDRAM page hits, TA can come before AACK. In fact, AACK and TA are not guaranteed to be in order.
- *Single MSC8126 mode*. The bus operation is the same as for 60x bus mode, except that the address that is driven on A[0–31] is latched and possibly multiplexed inside the MSC8126. Therefore, the address is valid throughout the data phase of the cycle beginning with AACK and ending with the data phase of the next access. Single MSC8126 mode does not support mastering of the 60x system bus by any other resource, including an additional MSC8126 device.

- *Local bus*. The local bus does not burst when an external master accesses it through the 60x bus bridge. Accesses to the local bus are not snooped by the SC140 core.
- *Bursts*. Burst accesses by 60x masters to registers or to the local bus are terminated with $\overline{\text{TEA}}$.
- *Address acknowledge*. The MSC8126 asserts $\overline{\text{AACK}}$ for all accesses to external memory that match a BR/OR range in the memory controller and also drives $\overline{\text{TA}}$ unless programmed otherwise.

6.2 BADDRx in 60x Mode

In 60x-bus-compatible mode, the BADDR [27–31] pins must be used—not the standard address A[27–31] pins—to address memories when the GPCM and UPM machines are in use. This is necessary because 60x masters, including the internal SC140 core, do not dynamically adjust the transaction for bus size. The 60x masters drive only the starting address on a burst, and thus the address lines do not increment. The GPCM memory controller accesses the memory as single accesses. Both the GPCM and the UPM increment the BADDRx lines to gather the bytes that the 60x master requests. In single MSC8126 mode, the memory controllers drive the address lines for small port sizes and increments for bursts. Therefore, the BADDRx pins are not needed in this mode.

6.3 Bank Selects Versus Address Lines

In single MSC8126 mode, use the BNKSEL lines to interface to SDRAM to support different SDRAM densities without requiring board wiring changes. Also, use the BNKSEL lines and set the BCR[EAV] bit so that logic analyzers can view the non multiplexed address of the access.

6.4 Bank Versus Page Interleaving

Bank interleaving is the preferred method for connecting to SDRAM. To achieve the highest performance, the MSC8126 SDRAM machine provides an interface to SDRAMS using SDRAM pipelining, bank interleaving, and back-to-back reads or writes in page mode.

7 EOnCE/JTAG Interface

The MSC8126 device includes an Enhanced On-Chip Emulation module (EOnCE), a feature common to all Freescale processors with the SC140 core. EOnCE gives internal access to scan chains for debug purposes and also provides a serial connection to the SC140 core for emulator support. An EOnCE/JTAG connection adds little or no cost to a system but adds significant advantages during early system development. This interface is implemented using a standard 14-pin header as shown in **Figure 2**.

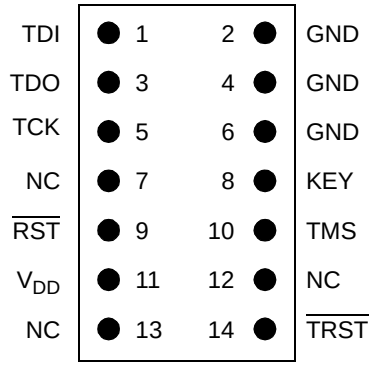

Figure 2. 14-Pin Header for JTAG/EOnCE Interface

The EOnCE interface connects through the JTAG port on the MSC8126 device with some additional status monitoring signals. **Table 7** shows the pin definitions and recommendations.

Table 7. JTAG/EOnCE Interface Pin Definitions

Pins	Connection	Description	Recommendations
1	TDI	Test Data In	If there are multiple devices on the JTAG chain, connect TDI to the TDO signal of the previous device in the chain.
2,4,6	GND	System Ground Plan	Connect to digital ground.
3	TDO	Test Data Out	If there are multiple devices on the JTAG chain, connect TDO to the TDI signal of the next device in the chain.
5	TCK	Test Clock	Add a 10 KΩ pull-down resistor.
7,13,12	NC	No Connect	Leave unconnected.
8	KEY	Mechanical Keying	Pin should be removed.
9	$\overline{\text{RST}}$	Reset	Can be tied to $\overline{\text{HRESET}}$.
10	TMS	Test Mode Select	None.
11	V_{DD}	I/O Power Supply	Connect to MSC8126 I/O Voltage V_{DDH} through a 220 Ω current limiting resistor.
14	$\overline{\text{TRST}}$	Test Reset	$\overline{\text{TRST}}$ has an internal pull-up, so no external pull-up or pull-down is required. However, the recommendation is to add a 1 KΩ pull-down to GND on this signal to keep the JTAG in reset mode while the device is operating normally. Asserting this signal asynchronously initializes the test controller. $\overline{\text{TRST}}$ must be asserted during power up.

Connecting multiple devices via their JTAG port is commonly called *daisy chaining*. Multiple target DSP devices can connect in series so that a single command converter and JTAG connector can control multiple target DSPs. Daisy chaining should be considered for a board with multiple DSPs. In a daisy chain configuration, such as that shown in **Figure 3**, a serial path is formed by the connection of the serial Test Data In (TDI) and Test Data Out (TDO) pins. Essentially, the path formed by TDI and TDO connects the JTAG registers of the devices serially. The input pin to the entire chain is TDI, and the output pin from the entire chain is TDO. The Test Clock (TCK) and Test Mode Select (TMS) pins of all the devices are wired in parallel so that there is a single TCK input and a single TMS input. In this configuration, if a device in the daisy chain is reset, all devices on the chain are reset because the $\overline{\text{RESET}}$ signals are connected.

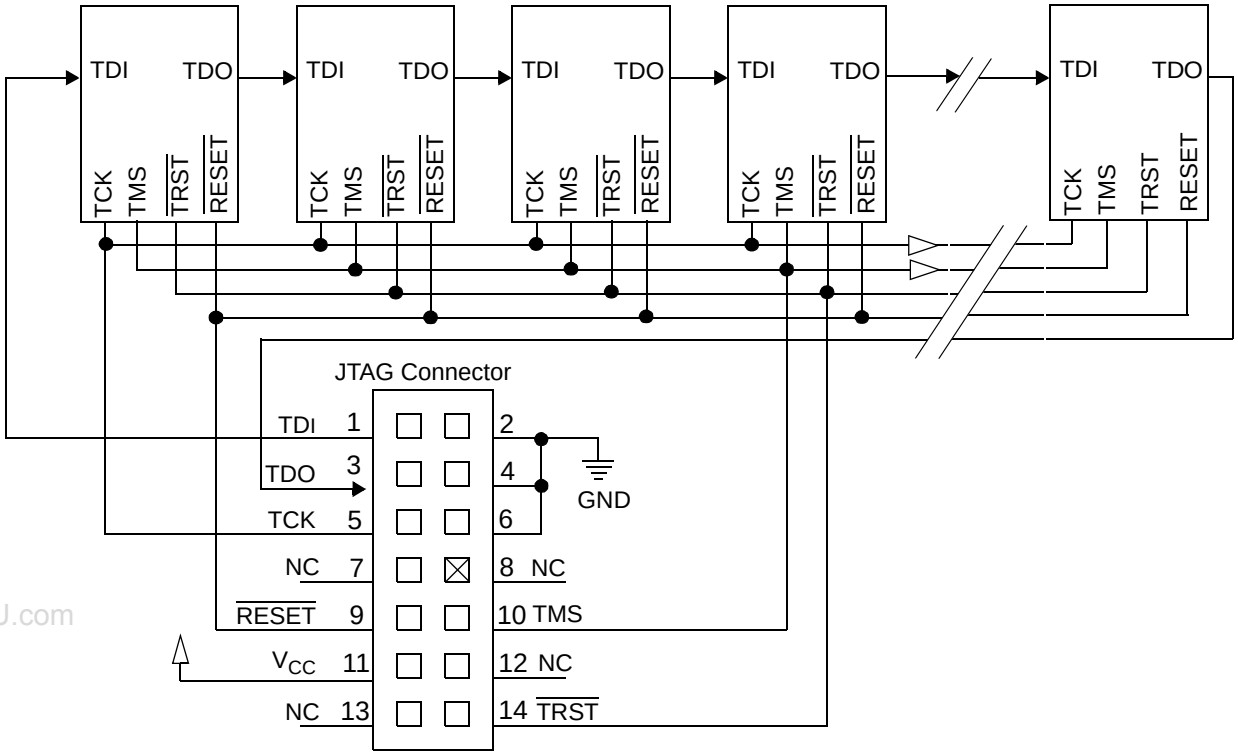

Figure 3. Multiple Target DSP Connection

Since the MSC8126 is a multi-core device, each SC140 core has its own link on the JTAG chain. Therefore, when you are designing a daisy chain, remember that each MSC8126 device provides four indices to the chain. This is also important to remember when you are setting up JTAG chain initialization in software.

Connecting EE0 and EE1 to an additional header is recommended for debug boards. EE0 is used to enter debug mode and EE1 can be used for logic analyzer triggers and other useful debugging activities. Refer to the "Debugging" chapter of the *MSC8126 Reference Manual* for details.

8 Signal Terminations

Table 8 summarizes the signal connections for the MSC8126. Refer to the data sheet for details on the connection guidelines:

- *xx–yy*Ω *VDDH*. A pull-up resistor to the V_{DDH} power supply, with a value between xx and yy Ω. You can select the value on the basis of system requirements, such as noise immunity.
- *xx–yy*Ω *GND*. A pull-down resistor to the ground power connection with a value between xx and yy Ω. Again, you can specify the value.
- O*pen*. The signal should/must be left unconnected. The Note column in **Table 8** specifies whether it is a requirement.
- *As needed*. The connection is determined principally by the system. It connects to the system controller logic, whether from Freescale or one of several third-parties who make such logic. If not designated, a pull-up should be between 1KΩ–10KΩ and connected to V_{DDH} and a pull-down between 100Ω–1KΩ and connected to GND.

Unused inputs should be tied high or low, but not left floating. Unused inputs can be tied directly to GND but a pull-up resistor is recommended if it is tied high. Generally, it is good practice to tie any unused input to GND or V_{DDH} through a resistor for board testability purposes.

The following signals are active during the reset configuration period of $\overline{\text{HRESET}}$: A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, and BADDRx. All signals can be turned off using the HIGHZ JTAG command. Input-only signals such as $\overline{\text{PORESET}}$ or signals configured in an input-only mode, such as $\overline{\text{IRQx}}$ or $\overline{\text{EXT\_BRx}}$, do not require pull-up/pull-down resistors if they are actively driven. However, in the interest of caution, pull-up resistors are recommended in **Table 8**. You should exercise discretion.

The hard reset signal states provided do not include the states during reset configuration. During the assertion of $\overline{\text{PORESET}}$, configurable signals have their default configuration (and are therefore tri-stated or high impedance). During reset configuration, configurable signals still have their default configuration, and certain memory controller signals operate to perform the reset configuration function (A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, BADDRx).

Table 8. Signal States and Recommended Termination

Signal	Function[1]	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTES: 1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{BR}}$	B	Tri-stated, EARB = 0 High, EARB = 1	1–10 KΩ V_{DDH}		
$\overline{\text{BG}}$	B	High, EARB = 0 Tri-stated, EARB = 1	1–10 KΩ V_{DDH}	Open	Pull up if HRCW[EARB] = 1. In Single-Master mode, no pull-up resistor is required.
$\overline{\text{ABB}}$/$\overline{\text{IRQ4}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up.
$\overline{\text{TS}}$	B	Tri-stated	1–10 KΩ V_{DDH}	Open	Pull up. In Single-Master mode, no pull-up resistor is required.
A[0–31]	B	Low	As needed	Open	No requirement
TT0/HA7	B	Tri-stated	1–10 KΩ V_{DDH}	Open	Pull up in Multi-Master mode. In Single-Master mode, no pull-up resistor is required.
TT1	B	Tri-stated	1–10 KΩ V_{DDH}	Open	Pull up in Multi-Master mode. In Single-Master mode, no pull-up resistor is required.
TT[2–4]/$\overline{\text{CS[5–7]}}$	B	Tri-stated	1–10 KΩ V_{DDH}	Open	Pull up TT[2–4] in Multi-Master mode. In Single-Master mode, no pull-up resistor is required.
$\overline{\text{TBST}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
TSZ[0–3]	B	Tri-stated	As needed	Open	The TSZ bus can be pulled up or down. Pull down TSZ0 (100 Ω) for an external master. Otherwise, there is no requirement. In Single-Master mode, these signals can be open.
$\overline{\text{AACK}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up

Table 8. Signal States and Recommended Termination (Continued)

Signal	Function[1]	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTES: 1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{ARTRY}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{DBG}}$	B	High, EARB = 0 Tri-stated, EARB = 1	1–10 KΩ V_{DDH}	Open	Pull up. In Single-Master mode, no pull-up resistor is required.
$\overline{\text{DBB}}$/$\overline{\text{IRQ5}}$	B	Tri-stated	1–10 KΩ VDDH		Pull up
D[0–31]	B	Tri-stated	As needed	Open	No requirement
HD[32–39]/D[32–39]/ HD[44–45]/D[44–45/] HD[50–53]/D[50–53]/ HD[61–63]/D[61–63]	B	Tri-stated	As needed	Open	No requirement
HD[40–43]/D[40–43]/ ETHRX[0–3]	B	Tri-stated	As needed	Open	No requirement
HD[46–49]/D[46–49]/ ETHTX[0–3]	B	Tri-stated	As needed	Open	No requirement
HD54/D54/ETHTX_EN	B	Tri-stated	As needed	Open	No requirement
HD55/D55/ETHTX_ER	B	Tri-stated	As needed	Open	No requirement
HD56/D56/ETHRX_DV/ETHCRS_DV	B	Tri-stated	As needed	Open	No requirement
HD57/D57/ETHRX_ER	B	Tri-stated	As needed	Open	No requirement
HD58/D58/ETHMDC	B	Tri-stated	As needed	Open	No requirement
HD59/D59/ETHMDIO	B	Tri-stated	As needed	Open	No requirement
HD60/D60/ETHCOL	B	Tri-stated	As needed	Open	No requirement
ETHTX_CLK/ ETHREF_CLK	I	Tri-stated	As needed	Pull down	
ETHRX_CLK	I	Tri-stated	As needed	Pull down	
ETHCRS	I	Tri-stated	As needed	Pull down	
DP0/DREQ1/$\overline{\text{EXT\_BR2}}$	B	High, DPPC=11 Tri-stated Otherwise	As needed	Open	Pull up if used as EXT_BR2.
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{DACK1}}$/ $\overline{\text{EXT\_BG2}}$	B	High, DPPC =11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ1}}$ or DACK1. Pull up $\overline{\text{EXT\_BG2}}$ in Multi-Master mode.
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/ $\overline{\text{EXT\_DBG2}}$	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ2}}$ or DACK2. Pull up $\overline{\text{EXT\_DBG2}}$ in Multi-Master mode.

Table 8. Signal States and Recommended Termination (Continued)

Signal	Function[1]	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTES: 1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{IRQ3}}$/DP3/DREQ2/ $\overline{\text{EXT\_BR3}}$	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ3}}$ or EXT_BR3.
$\overline{\text{IRQ4}}$/DP4/DACK3/ $\overline{\text{EXT\_BG3}}$	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ4}}$ or DACK3. Pull up $\overline{\text{EXT\_BG3}}$ in Multi-Master mode.
$\overline{\text{IRQ5}}$/DP5/DACK4/ $\overline{\text{EXT\_DBG3}}$	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ5}}$ or DACK4. Pull up $\overline{\text{EXT\_DBG3}}$ in Multi-Master mode.
$\overline{\text{IRQ6}}$/DP6/DREQ3	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ6}}$.
$\overline{\text{IRQ7}}$/DP7/DREQ4	B	High, DPPC = 11 Tri-stated, Otherwise	As needed	Open	Pull up if used as $\overline{\text{IRQ7}}$.
$\overline{\text{PSDVAL}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{TA}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{TEA}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
$\overline{\text{GBL}}$/$\overline{\text{IRQ1}}$	B	Tri-stated	1–10 KΩ V_{DDH}		Pull up
BADDR29/$\overline{\text{IRQ5}}$	B	Low	As needed	Open	Pull up if used as $\overline{\text{IRQ5}}$.
BADDR30/$\overline{\text{IRQ2}}$	B	Low	As needed	Open	Pull up if used as $\overline{\text{IRQ2}}$.
BADDR31/$\overline{\text{IRQ3}}$	B	Low	As needed	Open	Pull up if used as $\overline{\text{IRQ3}}$.
$\overline{\text{CS[0–4]}}$	O	High	As needed	Open	No requirement
$\overline{\text{BCTL1}}$/$\overline{\text{CS5}}$	O	High	As needed	Open	No requirement
BADDR[27–28]	O	Low	As needed	Open	No requirement
ALE	O	High	As needed	Open	No requirement
$\overline{\text{BCTL0}}$	O	Low	As needed	Open	No requirement
$\overline{\text{PWE[0–3]}}$/ PSDDQM[0–3]/$\overline{\text{PBS[0–3]}}$	O	High	As needed	Open	No requirement
PSDA10/PGPL0	O	High	As needed	Open	No requirement
$\overline{\text{PSDWE}}$/PGPL1	O	High	As needed	Open	No requirement
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	O	High	As needed	Open	No requirement
$\overline{\text{PSDCAS}}$/PGPL3	O	High	As needed	Open	No requirement

Table 8. Signal States and Recommended Termination (Continued)

Signal	Function[1]	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTES: 1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{PGTA}}$/PUPMWAIT/$\overline{\text{PPBS}}$/PGPL4	B	Tri-stated	As needed	Open	Pull up if configured as PUPMWAIT or PGTA (even when using internal TA).
PSDAMUX/PGPL5	O	Low	As needed	Open	No requirement
HD0/SWTE	B	Tri-stated	As needed	—	Pull up or pull down at $\overline{\text{PORESET}}$ to enable/disable software watchdog.
HD1/DSISYNC	B	Tri-stated	As needed	—	Pull up or pull down at $\overline{\text{PORESET}}$ to enable/disable DSI synchronous mode.
HD2/DSI64	B	Tri-stated	As needed	—	Pull up or pull down at $\overline{\text{PORESET}}$ to set the width of the DSI and system buses.
HD3/MODCK1	B	Tri-stated	10 KΩ	—	Pull up or pull down per desired clock configuration at $\overline{\text{PORESET}}$.
HD4/MODCK2	B	Tri-stated	10 KΩ	—	Pull up or pull down per desired clock configuration at $\overline{\text{PORESET}}$.
HD5/CNFGS	B	Tri-stated	As required by reset configuration mode	—	$\overline{\text{RSTCONF}}$ and CNFGS define the MSC8126 reset configuration mode and should be either pulled up or pulled down at $\overline{\text{PORESET}}$ as appropriate for reset mode. For details, see **Section 4**.
HD[6–31]	B	Tri-stated	As needed		
HA[11–29]	I	Tri-stated	As needed	Pull down	
$\overline{\text{HWBS[0–3]}}$/$\overline{\text{HDBS[0–3]}}$/HWBE[0-3]/HDBE[0–3]	I	Tri-stated	As needed	Pull up	Pull up when the DSI is in 32-bit or 64-bit data bus mode.
$\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/PSDDQM[4–7]/$\overline{\text{PBS[4–7]}}$	B	Tri-stated	As needed	Open	Pull up when the DSI is in 64-bit data bus mode.
$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	I	Tri-stated	As needed		Pull up or down if not used.
$\overline{\text{HBCS}}$	I	Tri-stated	As needed	Pull up to V_{DDH}	When used with a pull up, a 2.2 KΩ pull up is recommended.
$\overline{\text{HTA}}$	O	Tri-stated	As needed	Open	Pull up in synchronous mode. In Asynchronous mode, pull up or down, depending on design requirements. When a pull-up resistor is used, the rise time of the HTA signal is determined by the pull-up strength until DCR[HTAAD] is set.

Table 8. Signal States and Recommended Termination (Continued)

Signal	Function[1]	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTES: 1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{HBRST}}$	I	Tri-stated	As needed	Pull up to V_{DDH}	
HCID[0–2]	I	Tri-stated	As needed	Pull down	
HCID[3]/HA8	I	Tri-stated	As needed	Pull down	
HCLKIN	I	Tri-stated	As needed	Pull down	
$\overline{\text{HCS}}$	I	Tri-stated	As needed	Pull up to V_{DDH}	
HDST0/HA9	I	Tri-stated	As needed	Pull down	Can be left disconnected if the DSI is in Big Endian mode.
HDST1/HA10	I	Tri-stated	As needed	Pull down	Can be left disconnected if the DSI is in Big Endian mode.
GPIO0/CHIP_ID0/ $\overline{\text{IRQ4}}$/ETHTXD0	B	Tri-stated	As needed	Pull down	Configure as needed to define the MSC8126 chip ID.
GPIO1/TIMER0/$\overline{\text{IRQ5}}$/ CHIP_ID1/$\overline{\text{ETHTXD0}}$	B	Tri-stated	As needed	Pull down	Configure as needed to define the MSC8126 chip ID.
GPIO2/TIMER1/ CHIP_ID2/ $\overline{\text{IRQ6}}$	B	Tri-stated	As needed	Pull down	Configure as needed to define the MSC8126 chip ID.
GPIO29/CHIP_ID3/ ETHTX_EN	B	Tri-stated	As needed	Pull down	Configure as needed to define the MSC8126 chip ID.
Remaining GPIO signals	B	Tri-stated	As needed	Pull down	Leave any unused GPIO signals as input and tie them to GND.
$\overline{\text{NMI}}$	I	Tri-stated	1–10 KΩ V_{DDH}		Pull up.
$\overline{\text{NMI\_OUT}}$	OD	Tri-stated	1–10 KΩ V_{DDH}	Open	Pull up if used.
$\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$	B	High, IRQ7INT=0 Otherwise: Tri-stated.	1–10 KΩ V_{DDH}	Open	Pull up if used.
$\overline{\text{TRST}}$	I	Internal pull-up resistor	1 KΩ to GND		See **Table 7**.
TCK	I	Tri-stated	1–10 KΩ to GND		See **Table 7**.
TMS	I	Internal pull-up resistor	1–10 KΩ to V_{DDH}		See **Table 7**.
TDI	I	Internal pull-up resistor	1–10 KΩ to V_{DDH}		See **Table 7**.
TDO	O	Tri-stated	As needed	Open	See **Table 7**.
TEST	I	Tri-stated	0Ω to V_{SS}		See **Table 7**.
$\overline{\text{PORESET}}$	I	Tri-stated	1–10 KΩ to V_{SS}		Weak pull down.

Table 8. Signal States and Recommended Termination (Continued)

Signal	Function[1]	State at Hard Reset	Connection		Notes
			If Used	If Not Used	
NOTES: 1. I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they can be used as inputs or outputs.					
$\overline{\text{HRESET}}$	OD	Low	1–10 KΩ to V_{DDH}		Pull up.
$\overline{\text{SRESET}}$	OD	Low	1–10 KΩ το V_{DDH}		Pull up.
$\overline{\text{RSTCONF}}$	I	Tri-stated	As required by reset configuration mode	—	$\overline{\text{RSTCONF}}$ and CNFGS define the MSC8126 reset configuration mode and should be either pulled-up or pulled-down as appropriate for reset mode. See **Section 4** for details.
EE1	O	Active	As needed	Open	
EE0	I	Active	1–10 KΩ to V_{SS}		Pull down.
BM[0–2/TC[0–2]/ BNKSEL[0–2]	B	Tri-stated	As needed	—	Pull up or pull down per desired boot mode configuration.
CLKIN	I	Tri-stated	As needed	—	Provide appropriate clock.
CLKOUT	O	Active	As needed	Open	

9 Related Reading

The reference materials listed in **Table 9** can be obtained at the web site listed on the back cover of this document. Visit the relevant product summary page or search by title or document identification number.

Table 9. Related Reading

Document Category	Document Title	Document ID
Data Sheet (Hardware Specifications)	*MSC8126 Technical Data* sheet	MSC8126
Errata (device)	MSC8126 Silicon Errata	
Manuals	*MSC8126 Reference Manual*	MSC8126RM
	MSC8126 User's Guide	MSC8126UG
	SC140 DSP Core Reference Manual	MNSC140CORE
Application Notes	List available on the website on the back cover of this document	
Reference Design	*MSC8126 Application Development System User's Manual*	MSC8126ADSUM

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