Altima Communications Inc.

AC108 RM/RU/RN
Ultra Low Power 10/100 Bridge Repeater

GENERAL DESCRIPTION

The **AC108R** is a family of fully integrated multi port dual speed hubs with support for an SRAM interface, a single MII port, both 10M and 100M cascadable buses, stacking capability and SNMP and RMON statistics.

- **AC108RM** – 8 port, management, stack
- **AC108RU** – 8 port, no management, stack
- **AC108RN** – 8 port, no management, no stack

AC108R products are fully compliant IEEE 802.3(u) Class II Repeaters. The device provides 8 ports of 10 Base-T/100 Base-TX interface. All ports support either auto-negotiation (ANEG), parallel detection or selected media when configure accordingly. Port 7 supports 100BASE-FX fiber media via PECL interfaces. The MII interface can be connected to any MII compliant MAC at either 10M or 100M.

Once a port's technology is set, the port automatically connects to one of the two internal repeaters, one operating at 10 Mbps and the other one at 100 Mbps. Two integrated back-planes, one operating at 10 Mbps and one at 100 Mbps, allow port expansion up to 288 ports.

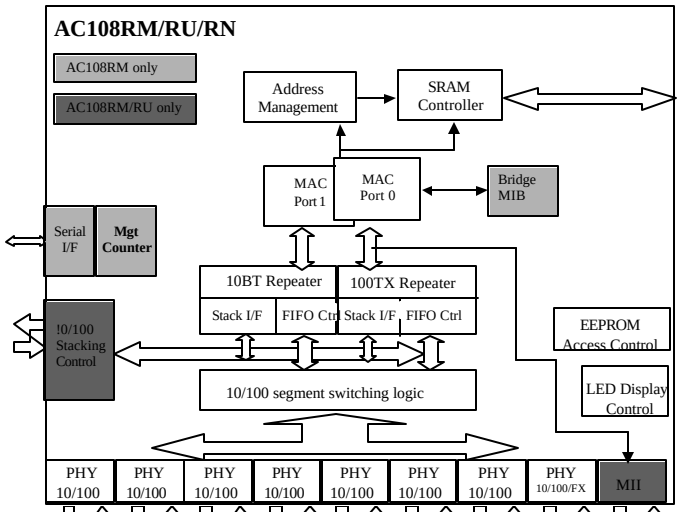
An internal two port switch connects either the 10M and 100M repeater segments, or the 100M segment with an isolated port 7. External SRAM is used for address table and packet buffering.

64 and 32-bit SNMP and RMON management counters are accessible via a high-speed serial management bus.

FEATURES

- 8 10/100 TX or 7 10/100TX and 1 100FX ports
  - Embedded TX PHYs
  - Half Duplex
  - FEFI on 100FX
- 10M or 100M MII for MAC connection
- Very small package - 272PBGA
  - 729 sq. mm footprint
- Very low power - TYP < 3W (Total)
  - Selectable TX drivers for 1:1 or 1.25:1 transformers allowing for additional power reduction
  - Cable Detect mode - TYP < 1.4W (Total)
  - Power Down mode - TYP < 1W (Total)
- Fully compliant with
  - IEEE 802.3 / 802.3u
  - MII
  - HDLC Management Bus (RMON/SNMP)
  - UNH test labs (future)
- Stackable to 288 ports
- Non-blocking 10/100M bridge with MAC controller and switching engine
- SRAM support as the external buffer memory up to 512K x 16.
- Unique, per port, scrambler seed for reduced emissions
- Baseline Wander Compensation
- Highly efficient LED outputs
- Cable length indicator
- Reverse polarity detection and correction with settable Register Bit indication
- 8 interrupts per port

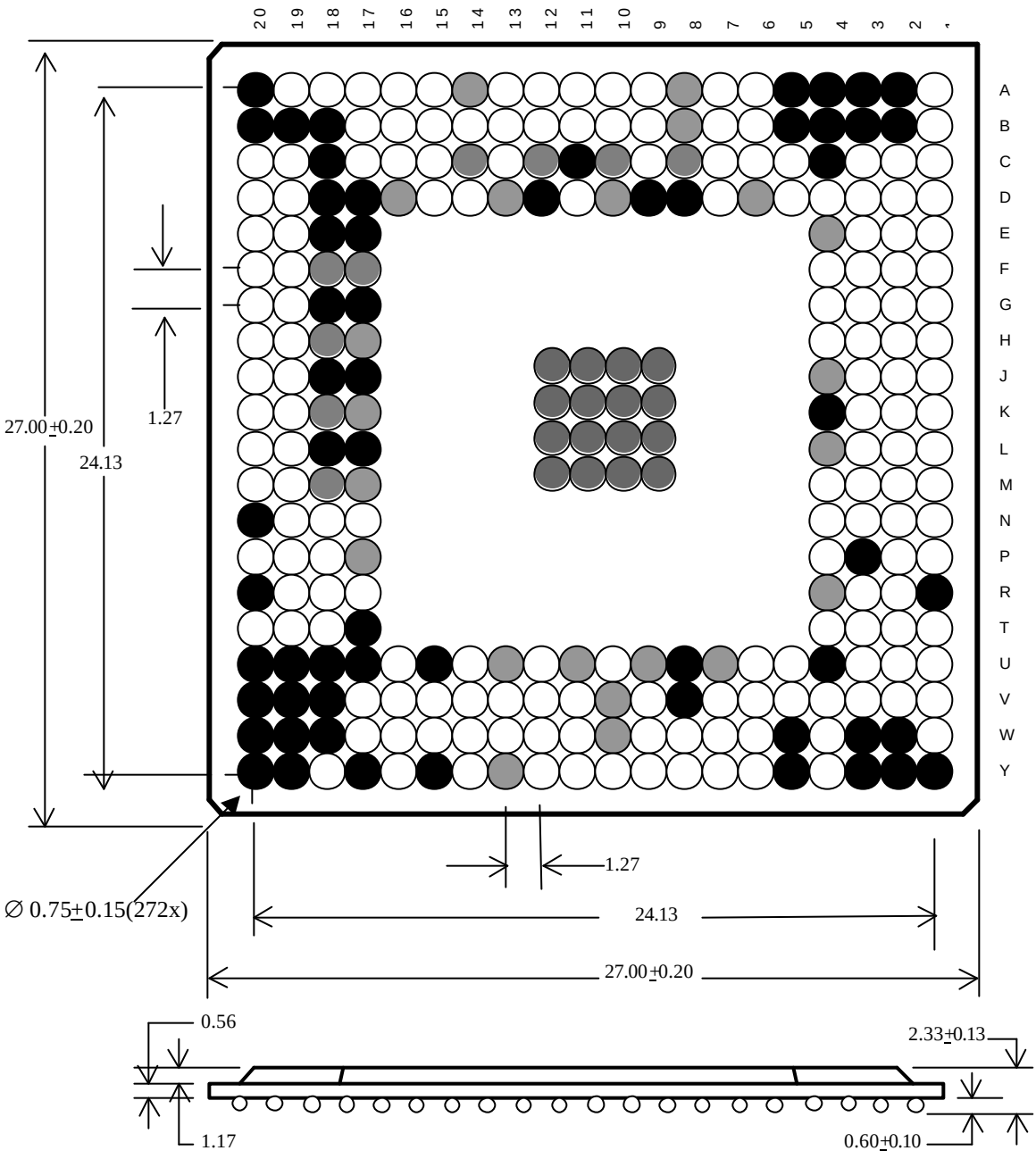
BLOCK DIAGRAM



PIN DIAGRAM - AC108RM/RU/RN

Bottom VIEW:

- Standard I/O
- Ground
- Digital VCC
- Analog VCC
- G/T



Pin Descriptions

Many of the pins of these devices have multiple functions. The multi-function pins will be designated by **bolding** of the pin number. The separate descriptions of these pins will be listed in the proper sections. Designers must assure that they have identified all modes of operation prior to final design.

NOTES:
The pin assignment shown below and in the pin description table is subjected to change without notice. The user is advised to contact **Altima Communications Inc.** before implement any design based on the information provided in this data sheet.

Signals types:
'I' = input
'O' = output
'Z' = high impedance
'U' = pull up with 10k ohm
'D' = pull down with 10k ohm
'A' = analog signal
'*' = Active Low Signal

MDI (Media Dependent Interface) Pins (TX)

Pin Name	BGA #	Type	Description
RXIP_7	C19	AI	Receiver Input Positive for both 10Base-T and 100Base-TX.
RXIP_6	F20	AI	
RXIP_5	G19	AI	
RXIP_4	K20	AI	
RXIP_3	L19	AI	
RXIP_2	N17	AI	
RXIP_1	P19	AI	
RXIP_0	T18	AI	
RXIN_7	C20	AI	Receiver Input Negative for both 10Base-T and 100Base-TX.
RXIN_6	F19	AI	
RXIN_5	G20	AI	
RXIN_4	K19	AI	
RXIN_3	L20	AI	
RXIN_2	N18	AI	
RXIN_1	P18	AI	
RXIN_0	T19	AI	
TXOP_7	D20	AO	Transmitter Output Positive for both 10Base-T and 100Base-TX.
TXOP_6	E19	AO	
TXOP_5	H20	AO	
TXOP_4	J19	AO	
TXOP_3	M19	AO	
TXOP_2	P20	AO	
TXOP_1	R19	AO	
TXOP_0	R18	AO	
TXON_7	D19	AO	Transmitter Output Negative for both 10Base-T and 100Base-TX.
TXON_6	E20	AO	
TXON_5	H19	AO	
TXON_4	J20	AO	
TXON_3	M20	AO	
TXON_2	N19	AO	
TXON_1	T20	AO	
TXON_0	R17	AO	

MDI (Media Dependent Interface) Pins (FX)

Pin Name	BGA #	Type	Description
FXIP_7	**A17**	AI	Receiver Input Positive for 100Base-FX**.**
FXIN_7	**C17**	AI	Receiver Input Negative for 100Base-FX**.**
FXOP_7	**C16**	AO	Transmitter Output Positive for 100Base-FX.
FXON_7	**B17**	AO	Transmitter Output Negative for 100Base-FX.
SDP7	**A18**	AI	FX Signal Detect Positive**.**
SDN7	**A19**	AI	FX Signal Detect Negative**.**

MII (Media Independent Interface) Pins

Pin Name	BGA #	Type	Description
MII_TXD3 MII_TXD2 MII_TXD1 MII_TXD0	V16 W16 Y16 V15	I,D	MII Transmit Data. The MAC will source TXD[3:0] synchronous with MII_TXCLK when TX_EN is asserted.
MII_TXCLK	W15	O	MII Transmit Clock. Continuous (25MHz/2.5MHz) clock output used by MAC to synchronize MII_TXEN, MII_TXD[3:0], and MII_TXER.
MII_TXEN	U14	I,D	MII Transmit Enable. Indicates MAC has presented valid data on the MII_TXD[3:0].
MII_TXER	V14	I,D	MII Transmit Error. Indicates MAC has presented invalid data on the MII_TXD[3:0]. Phy will generate error symbol /E/ on the wire.
MII_RXD3 MII_RXD2 MII_RXD1 MII_RXD0	V13 W13 U12 V12	O	MII Receive Data. The Phy will source RXD[3:0] synchronous with MII_RXCLK when RX_EN is asserted.
MII_RXCLK	W12	O	MII Transmit Clock. Continuous (25MHz/2.5MHz) clock output used by MAC to synchronize MII_RXEN, MII_RXD[3:0], and MII_RXER.
MII_RXDV	Y12	O	MII Receive Data-Valid. Phy has presented valid recovered on the MII_RXD[3:0].
MII_RXER	V11	O	MII Receive Error. Indicates Phy has received invalid symbol data.
MII_CRS	W14	O	MII Carrier Sense. Active when carrier has been sensed. During full duplex mode, CRS only responses to received carrier.
MII_COL	Y14	O	MII Collision Detection. Active when collision is detected.
MII_SPDSEL	U16	I,U	MII port speed selection. 1 = 100 Mb. 0 = 10 Mb.

Serial Configuration Prom

Pin Name	BGA #	Type	Description
PROM_CS	B11	O	PROM chip select. (For use with 93C46 serial EEPROM)
PROM_CLK	**C13**	O	PROM Clock.
PROM_OUT	**A13**	O	PROM Data Out.
PROM_IN	**B12**	I,D	PROM Data In.

100Mbps Stacked Bus for back-plane (Stack Master mode)

Pin Name	BGA #	Type	Description
100CRSU_IN*	D3	I,U	100M Carrier Sense Up In. Active when carrier is sensed from upper stacks. Only ChipID 00 needs to be connected.
100CRSD_IN*	C2	I,U	100M Carrier Sense Down In. Active when carrier is sensed from lower stacks. Only ChipID 00 needs to be connected.
100CRSU_OUT*	D2	O,Z	100M Carrier Sense Up Out. Active when receive activity detected on the current stack. This pin is to be daisy chained with upper stack. The last stack can leave this pin unconnected.
100CRSD_OUT*	B1	O,Z	100M Carrier Sense Down Out. Active when receive activity detected on the current stack. This pin is to be daisy chained with lower stack. The last stack can leave this pin unconnected.
100COLBP*	C1	I,O	100M Collision. Active when collision is detected. All 100COLBP* pins on the stack must be tied together. 150 ohm pull up to 3.3v on first stack. This pin is monitored to detect collisions on other devices.
100CRSBP*	C3	I,O,U	100 Carrier Sense BackPlane. Active when CRS is detected. All 100CRSBP* pins on the stack must be tied together. This pin is monitored to detect CRS on other devices.
100OE*	A1	O	100M Output-enable. Control pin to enable an external buffer.
100DIR	D4	O	100M Direction. Control pin for the direction of an external buffer. 0=Input (default), 1=Output.

100Mbps Internal Repeater Bus

Pin Name	BGA #	Type	Description
M100COL_LOCAL*	J1	I/O,Z,U	100M Local Collisions. Input on ChipID 00. Active low to indicate collision on all other ChipIDs.
M100ACTO*	**J3**	I/O,U	Output to ChipID 00 to signal local activity. (see next 3 signals)
M100ACTI_0*	**J3**	I/O,U	Connected from ChipID 00 to ChipID 01 M100ACTO* to sense activities. Open on all other ChipIDs.
M100ACTI_1*	J2	O,U	Connected from ChipID 00 to ChipID 10 M100ACTO* to sense activities. Open on all other ChipIDs.
M100ACTI_2*	K3	O,U	Connected from ChipID 00 to ChipID 11 M100ACTO* to sense activities. Open on all other ChipIDs.
M100COL_SYS*	H1	I/O,U	ChipID 00 will drive this pin the same as 100COLBP* to indicate local collision.
M100CRS_SYS*	K2	I/O,U	ChipID 00 will drive this pin the same as 100CRSBP* to indicate local activity.
MS100D4 MS100D3 MS100D2 MS100D1 MS100D0	H4 G1 G2 G3 G4	I/O I/O I/O I/O I/O	Multiple/Stacked Data Group. Transmit and receive data in de-scrambled 5B data groups for multiple devices. Data is sampled at the rising edge of MS100D_CLK and driven out on falling edge of MS100D_CLK.
MS100D_EN*	H2	I/O,U	Multiple/Stacked Data Enable. Active when data is valid.
MS100D_CLK	H3	I/O	Multiple/Stacked Data Clock The bi-directional non-continuous 25 MHz recovered clock for synchronizing with MS100D[4:0], & MS100D_EN*.

10Mbps Stacked Bus for back-plane (Stack Master mode)

Pin Name	BGA #	Type	Description
10CRSU_IN*	E2	I,U	10M Carrier Sense Up In. Active when carrier is sensed from upper stacks. Only ChipID 00 needs to be connected.
10CRSD_IN*	E1	I,U	10M Carrier Sense Down In. Active when carrier is sensed from lower stacks. Only ChipID 00 needs to be connected.
10CRSU_OUT*	D1	O,Z	10M Carrier Sense Up Out. Active when receive activity detected on the current stack. This pin is to be daisy chained with upper stack. The last stack can leave this pin unconnected.
10CRSD_OUT*	F4	O,Z	10M Carrier Sense Down Out. Active when receive activity detected on the current stack. This pin is to be daisy chained with lower stack. The last stack can leave this pin unconnected.
10COLBP*	E3	I/O	10M Collision. Active when collision is detected. All 10COLBP* pins on the stack must be tied together. 330 ohm pull up to 3.3v on first stack. This pin is monitored to detect collisions on other devices.
10CRSBP*	F3	I/O,U	10 Carrier Sense BackPlane. Active when CRS is detected. All 100CRSBP* pins on the stack must be tied together. This pin is monitored to detect CRS on other devices.
10OE*	F1	O	10M Output-enable. Control pin to enable an external buffer.
10DIR	F2	O	10M Direction. Control pin for the direction of an external buffer. 0=Input (default), 1=Output.

10Mbps Internal Repeater Bus

Pin Name	BGA #	Type	Description
M10COL_LOCAL*	M1	I/O,Z, U	100M Local Collisions. Input on ChipID 00. Active low to indicate collision on all other ChipIDs.
M10ACTO*	**M2**	I/O,U	Output to ChipID 00 to signal local activity. (see next 3 signals)
M10ACTI_0*	**M2**	I/ O,U	Connected from ChipID 00 to ChipID 01 M10ACTO* to sense activities. Open on all other ChipIDs.
M10ACTI_1*	M3	O,U	Connected from ChipID 00 to ChipID 10 M10ACTO* to sense activities. Open on all other ChipIDs.
M10ACTI_2*	M4	O,U	Connected from ChipID 00 to ChipID 11 M10ACTO* to sense activities. Open on all other ChipIDs.
M10COL_SYS*	L3	I/O,U	Chip ID 00 will drive this pin the same as 10COLBP* to indicate local collision.
M10CRS_SYS*	N1	I/O,U	Chip ID 00 will drive this pin the same as 10CRSBP* to indicate local activity.
MS10D	L1	I/O	Multiple/Stacked Data Group. Transmit and receive data in 10BT for multiple devices. Data is sampled at the rising edge of MS10D_CLK and driven out on falling edge of MS10D_CLK.
MS10D_EN*	L2	I/O,U	Multiple/Stacked Data Enable. Active when data is valid.
MS10D_CLK	K1	I/O	Multiple/Stacked Data Clock The bi-directional non-continuous 10 MHz recovered clock for synchronizing with MS10D, & MS10D_EN*.

Serial Management port

Pin Name	BGA #	Type	Description
RECONFIG	A7	I,D	Re-arbitration. When this pin toggles (0-1-0), "RequestID" will be sent to Agent to restart arbitration to get a new hubID.
SER_MATCH	B7	O	Active High output indicated serial address match occurred.
SRX	C7	I	Serial Receive is sampled on the rising edge of SERCLK
STX	D7	O,Z	Serial Transmit is driven on the falling edge of SERCLK. When not driven, it is tri-stated.
SERCLK	A6	I	Clock for serial management interface.
ARBIN	B6	I	Daisy Chain Arbitration input This signal requires a 10K Ohms pulled low.
ARBOUT	C6	O	Daisy Chain Arbitration output. Default high upon power up.
INT*	D5	O	Interrupt.
MGR_PRES*	C5	I,U	Manager Present.

LED Display

Pin Name	BGA #	Type	Description
LED_LN7 LED_LN6 LED_LN5 LED_LN4 LED_LN3 LED_LN2 LED_LN1 LED_LN0	A9 B9 C9 A10 B10 A11 D11 A12	O	Enable corresponding LED display line in the display matrix, active low output. The detail of how to program and connect the LEDs is in the LED Setup section.
LED_DATA7 **LED_DATA6** **LED_DATA5** **LED_DATA4** **LED_DATA3** **LED_DATA2** **LED_DATA1** **LED_DATA0**	**B12** **C13** **A13** **B13** **B14** **D14** **A15** **B15**	I/O,D	Output for LED display information of each column in the display matrix. Active high output. The LED pins are shared with reset-read configuration pins, test pins and EEPROM interface. The value applied on the reset-read pins is only valid at the end of the reset cycle. The EEPROM interface is active after the reset cycle. Once the data in the EEPROM is read the same pins are used for LED display.

Control and Setup

Pin Name	BGA #	Type	Description
Mode[0] Mode[1]	**B15** **A15**	I,D	Mode 1 - Mode 0 Domain "A" Domain "B" 0 0 10M Rptr 100M Rptr (Master) 0 1 10M Rptr 100M Rptr (Stand Alone) 1 0 Port 7 100M Rptr 1 1 Illegal configuration. Pulled up or down through 10K Ohm resistor.
ChipID[0] ChipID[1]	**D14** **B14**	I,D	To assign chip ID for 4 devices in a single box. One and only one device in the box must be assigned with ChipID=0. Pulled up or down through 10K Ohm resistor.
IBREF	A16	I	Reference bias resistor. Connected to analog ground through a 10k (1%) resistor.
FX_SEL7	**B13**	I, D	Select FX mode for Port 7. 0=TX, 1=FX

Clock, Reset & Misc.

Pin Name	BGA #	Type	Description
RESET*	N2	I,U	Reset to initial and defaulted state.
CLK	P4	I	25MHz-System-clock reference input. This pin shall be connected to an external 25MHz-clock source. Multiple devices should be synchronous to the same external clock source.
RAMTest[0] **RAMTest[1]**	**Y6 W6**	I/O,D	Read during reset. 00 = normal mode, no ram test 01 = reserved 10 = reserved 11 = normal mode, ram test

SRAM Interface

The SRAM Interface is designed to support low cost 2*32K*8 or 2*64K*8 asynchronous memory.

Pin Name	BGA #	Type	Description
CE0*	N3	O	Chip Enable for SRAM 0 chip. CE0* is inverted from CE1*.
CE1*	N4	O	Chip Enable for SRAM 1 chip. CE1* is inverted from CE0*.
GW*	P1	O	Global Write, active low signal.
OE*	P2	O	Output Enable, active low signal.
RAM_SIZE[1] **RAM_SIZE[0]**	**Y7** **W7**	I/O,U	External SRAM size per chip, Read during Reset. 00 = 128k x2 - 01 = invalid - 10 = 256k x2 - 11 = 512k x2
RAMA_17 RAMA_16 RAMA_15 RAMA_14 RAMA_13 RAMA_12 RAMA_11 RAMA_10 RAMA_9 **RAMA_8** **RAMA_7** RAMA_6 **RAMA_5** **RAMA_4** RAMA_3 RAMA_2 RAMA_1 RAMA_0	W11 Y11 Y10 U10 Y9 W9 V9 Y8 W8 **Y7** **W7** V7 **Y6** **W6** V6 U6 V5 Y4	I/O	SRAM Address output.
RAMD_15 RAMD_14 RAMD_13 RAMD_12 RAMD_11 RAMD_10 RAMD_9 RAMD_8 RAMD_7 RAMD_6 RAMD_5 RAMD_4 RAMD_3 RAMD_2 RAMD_1 RAMD_0	W4 U5 V4 V3 W1 V2 V1 U3 U2 U1 T4 T3 T2 T1 R3 R2	I/O,D	SRAM Data Input and Output

Power and Ground

Pin Name	BGA #	Type	Description
Power 1	A8,A14 B8 D6,D10,D13,D16 E4 H17 J4 K17 L4 M17 R4 U7,U9,U11,U13 V10 W10 Y13	VCCD	Digital VCC Total of 21 digital Vcc pins.
Power 2	C8,C10,C12,C14 F17-18 H18 K18 M18 P17	VCCA	Analog VCC Total of 10 digital Vcc pins.
Ground	A2-5,A20 B2-5,B18-20 C4,C11,C18 D8,D9,D12,D17,D18 E17-18 G17-18 J9-12, J17-18 K4,K9-12 L9-12,L17-18 M9-12 N20 P3 R1,R20 T17 U4,U8,U15,U17-20 V8,V18-20 W2-3,W5,W18-20 Y1-3,Y5,Y15,Y17,Y19-20	GND	Ground Total of 75 ground pins.
N/C	B16, C15, D15, V17, W17, Y18	N/C	Total of 6 No Connect pins

FUNCTIONAL DESCRIPTION

The **AC108R** is a single chip 10/100Mbps repeater controller with bridge function. The device provides 8 10BASE-T/100BASE-TX twisted pair interface ports supporting ANEG, parallel detection and force media operation.

Upon technology selection, each port is logically attached to either the internal 10Mbps repeater or the internal 100Mbps repeater. All ports running at the same speed will repeat among themselves. 10M and 100M stacking buses are available to allow port expansion up to 288 ports in one collision domain at each speed on the **AC108R**.

In addition to the two internal repeaters the **AC108R** includes a built-in 2-segment switch for connection between the 10M and the 100M repeater segments, or between the 100M repeater and an isolated port 7, depending on the setting of the Mode[1:0] bits.

SNMP and RMON statistic can be gathered through a high speed HDLC serial management interface for Intelligent HUB applications.

The **AC108R's** ultra low power architecture consumes ~1A maximum @ 3.3Volts when all ports are running 100Base-TX full speed. A built-in power management function will power down the individual ports when no cable is detected which helps further drive down the power consumption and improve long-term reliability.

Functions:

- 4B/5B
- MLT3
- NRZI
- Manchester Encoding and Decoding
- Clock and Data Recovery
- Stream Cipher Scrambling / De-Scrambling
- Adaptive Equalization
- Line Transmission
- Carrier Sense
- Link Integrity Monitor
- Auto-Negotiation (ANeg)/Parallel Detection
- 10Mbps and 100Mbps repeating
- 2 port switching
- MII MAC connection
- HDLC Management Interface
- SNMP/RMON statistics tables

MAC INTERFACE

MII

The Media Independent Interface (MII) is an 18 wire MAC/Phy interface described in 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100Mbps or 10Mbps, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and Phy, synchronous with Enable and Error signals.

MII data is received from and transmitted to the internal repeater determined by the MII_SPDSEL pin.

On receipt of valid data from the wire interface, RX_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TX_EN is presented to the Phy indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the Phy synchronous to TX_CLK during the time that TX_EN is valid.

SMI

The Serial Management Interface (SMI) provides system access to the SNMP, RMON and port status registers of the device. A single, daisy chain connection can be use to read and/or write the registers of multiple devices. The interface consists of two digital signals; clock and data. HDLC formatted packets, with a start/stop flag, header and CRC field for error checking, are use for all reads and writes. Zero-bit insertion/removal is used. Operation speed can range from 0 to 2 Mbps.

Interrupt

The INTR pin on the Phy will be asserted whenever one of 8 selectable interrupt events occur. Assertion state is programmable to either high or low through the INTR_LEVL register bit. Selection is made by setting the appropriate bit in the Interrupt Mask register. When the INTR bit goes active, the MAC

interface is required to read the Interrupt Status register to determine which event caused the interrupt. The Status bits are read only and clear on read. When INTR is not asserted, the pin is held in a high impedance state.

Carrier Sense / RX_DV

Carrier sense is asserted asynchronously on the CRS pins as soon as activity is detected on the receive data stream of any port connected to the repeater to which the MII is connected. RX_DV is asserted as soon as a valid SSD (Start-of-Stream Delimiter) is detected. Carrier sense and RX_DV are de-asserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. However, if the carrier sense is asserted and a valid SSD is not detected immediately, RX_ER is asserted instead of RX_DV.

In 10Base-T mode, CRS is asserted asynchronously when the valid preamble and data activity is detected on the RXIP and RXIN pins.

Since the device is always in half duplex mode, the CRS is activated during both the transmission and reception of data.

MEDIA INTERFACE

10BASE-T

When configured to run in 10Base-T mode, either through hardware configuration, software configuration or ANeg, the Phy will support all the features and parameters of the industry standards.

Transmit Function

Parallel to Serial logic is used to convert the 4-bit (MII) data into the serial stream. The serialized data goes directly to the Manchester encoder where it is synthesized through the output waveshaping driver. The waveshaper reduces any EMI emission by filtering out the harmonics, therefore eliminating the need for an external filter.

Receive Function

The received signal passes through a low-pass filter, which filters out the noise from the cable, board, and transformer. This eliminates the need for a 10Base-T external filter. A Manchester decoder converts the incoming serial stream. Serial to Parallel logic is used to generate the 4-bit (MII) data.

Link Monitor

The 10-Base-T link-pulse detection circuit will constantly monitor the RXIP/RXIN pins for the presence of valid link pulses. In the absence of valid link pules, the Link Status bit will be cleared and the Link LED will de-assert.

100BASE-TX

When configured to run in 100Base-TX mode, either through hardware configuration, software configuration or ANeg, the Phy will support all the features and parameters of the industry standards.

Transmit Function

In 100Base-TX mode, the Phy transmit function converts synchronous 4-bit (MII) data to a pair of 125 Mbps differential serial data streams. The serial data is transmitted over network twisted pair cables via an isolation transformer. Data conversion includes 4B/5B encoding, scrambling, parallel to serial, NRZ to NRZI, and MLT-3 encoding. The entire operation is synchronous to 25 MHz and 125 MHz clock. Both clocks are generated by an on-chip PLL clock synthesizer that is locked on to an external 25 MHz clock source.

The transmit data is transmitted from the MAC to the Phy via the TXD[3:0] signals. The 4B/5B encoder replaces the first two nibbles of the preamble from the MAC frame with a /J/K/ code-group pair Start-of-Stream Delimiter (SSD), following the onset of TX_EN signal. The 4B/5B encoder appends a /T/R/ code-group pair End-of-Stream Delimiter (ESD) to the end of transmission in place of the first two IDLE code-groups that follow the negation of the TX_EN signal. The encapsulated data stream is converted from 4-bit nibbles to 5-bit code-groups. During the inter-packet gap, when there is no data present, a continuous stream of IDLE code-groups are transmitted. When TX_ER is asserted while TX_EN is active, the Transmit Error code-group /H/ is substituted for the translated 5B code word. The 4B/5B encoding is bypassed when Scramble Disable is set.

In 100Base-TX mode, the 5-bit transmit data stream is scrambled as defined by the TP-PMD Stream Cipher function in order to reduce radiated emissions on the twisted pair cable. The scrambler encodes a

plain text NRZ bit stream using a key stream periodic sequence of 2047 bits generated by the recursive linear function:

$$X[n] = X[n-11] + X[n-9] \text{ (modulo 2)}$$

The scrambler reduces peak emissions by randomly spreading the signal energy over the transmitted frequency range, thus eliminating peaks at any single frequency. For repeater applications, where all ports transmit the same data simultaneously, signal energy is spread further by using a non-repeating sequence for each Phy, i.e., the scrambled seed is unique for each different Phy based on the Phy address.

Parallel to Serial, NRZ to NRZI, and MLT3 Conversion

The 5-bit NRZ data is clocked into Phy's shift register with a 25 MHz clock, and clocked out with a 125 MHz clock to convert it into a serial bit stream. The serial data is converted from NRZ to NRZI format, which produces a transition on Logic 1 and no transition on Logic 0. To further reduce EMI emissions, the NRZI data is converted to an MLT-3 signal. The conversion offers a 3dB to 6dB reduction in EMI emissions. This allows system designers to meet the FCC Class B limit. Whenever there is a transition occurring in NRZI data, there is a corresponding transition occurring in the MLT-3 data. For NRZI data, it changes the count up/down direction after every single transition. For MLT-3 data, it changes the count up/down direction after every two transitions. The NRZI to MLT-3 data conversion is implemented without reference to the bit timing or clock information. The conversion requires detecting the transitions of the incoming NRZI data and setting the count up/down direction for the MLT-3 data. Asserting FX_SEL high will disable this encoding.

Receive Function

The 100Base-TX receive path functions as the inverse of the transmit path. The receive path includes a receiver with adaptive equalization and DC restoration in the front end. It also includes a MLT-3 to NRZI converter, 125 MHz data and clock recovery, NRZI/NRZ conversion, Serial-to-Parallel conversion, de-scrambler, and 5B/4B decoder. The receiver circuit starts with a DC bias for the differential RX+/- inputs, followed with a low-pass filter to filter out high frequency noise from the transmission channel media. An energy detect circuit is also added to determine whether there is any signal energy on the media. This is useful in the power-saving mode. The amplification ratio and slicer's threshold is set by the on-chip bandgap reference.

Baseline Wander Compensation

The 100Base-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion. This creates jitter and possible increase in the bit error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of the DC component. This Phy implements a patent-pending DC restoration circuit. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. This design simplifies the circuit design and eliminates any random/systematic offset on the receive path. In the 10BaseT and the 100Base-FX modes, the baseline wander correction circuit is not required, and therefore is disabled.

Clock/Data Recovery

The equalized MLT-3 signal passes through the slicer circuit, and gets converted to NRZI format. The Phy uses a proprietary mixed-signal phase locked loop (PLL) to extract clock information from the incoming NRZI data. The extracted clock is used to re-time the data stream and set the data boundaries. The transmit clock is locked to the 25 MHz clock input while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to the data stream, extracts the 125 MHz clock, and uses it for the bit framing for the recovered data. The recovered 125 MHz clock is also used to generate the 25 MHz MII_RXCLK (MII). The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase alignment and locks to data in one transition. Its data/clock acquisition time after power-on is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, i.e. when the SD is de-asserted, the PLL will switch and lock on to MII_TXCLK. This provides a continuously running MII_RXCLK (MII). At the PCS interface, the 5 bit data RXD[4:0] is synchronized to the 25 MHz RX_CLK.

Decoder/De-scrambler

The de-scrambler detects the state of the transmit Linear Feedback Shift Register (LFSR) by looking for a sequence representing consecutive idle codes. The de-scrambler acquires lock on the data stream by recognizing IDLE bursts of 30 or more bits and locks its frequency to its de-ciphering LFSR.

Once lock is acquired, the device can operate with an inter-packet-gap (IPG) as low as 40 nS. However, before lock is acquired, the de-scrambler needs a minimum of 270 nS of consecutive idles in between packets in order to acquire lock.

The de-ciphering logic also tracks the number of consecutive errors received while the RX_DV is asserted. Once the error counter exceeds its limit currently set to 64 consecutive errors, the logic assumes that the lock has been lost, and the de-cipher circuit resets itself. The process of regaining lock will start again.

Stream cipher de-scrambler is not used in the 100Base-FX and the 10Base-T modes.

Link Monitor

Signal level is detected through a squelch detection circuitry. A signal detect (SD) circuit allows the equalizer to assert high whenever the peak detector detects a post-equalized signal with peak to ground voltage greater than 400 mV. This is approximately 40% of a normal signal voltage level. In addition, the energy level must be sustained for longer than 2~3 µS in order for the signal detect signal to stay on. The SD gets de-asserted approximately 1~2 µs after the energy level drops consistently below 300 mV from peak to ground.

The link signal is forced low during a local loopback operation (Loopback register bit is set) and forced to high when a remote loopback is taking place (EN_RPBK is set).

In forced 100Base-TX mode, when a cable is unplugged or no valid signal is detected on the receive pair, the link monitor enters in the “link fail” state and NLP's are transmitted. When a valid signal is detected for a minimum period of time, the link monitor enters Link Pass State and transmits MLT-3 signal.

100BASE-FX

When port 7 is configured to run in 100Base-FX mode, either through hardware configuration or software configuration (100Base-FX does not support ANeg) the Phy will support all the features and parameters of the industry standards.

Transmit Function

The serialized data bypasses the scrambler and 4B/5B encoder in FX mode. The output data is NRZI PECL signals. The PECL level signals are used to drive the Fiber-transmitter.

Receive Function

In 100Base-FX mode, signal is received through the PECL receiver inputs, and directly passed to the clock recovery circuit for data/clock extraction. In FX mode, the scrambler/de-scrambler cipher function is bypassed.

Link Monitor

In 100Base-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the Phy’s SDP pin.

Far-End-Fault-Insertion (FEFI)

ANeg provides the mechanism to inform the link partner that a remote fault has occurred. However, ANeg is disabled in the 100Base-FX applications. An alternative in-band signaling function (FEFI) is used to signal a remote fault condition. FEFI is a stream of 84 consecutive ones followed by one logic zero. This pattern is repeated 3 times. A FEFI will signal under 3 conditions:

- When no activity is received from the link partner
- When the clock recovery circuit detects a signal error or PLL lock error
- When management entity sets the transmit Far-End-Fault bit.

The FEFI mechanism is enabled by default in the 100Base-FX mode, and is disabled in 100Base-TX or 10Base-T modes. The register setting can be changed by software after reset.

10BASE-T/100BASE-TX/FX

Multi-Mode Transmit Driver

The multi-mode driver transmits the MLT-3 coded signal in 100Base-TX mode, NRZI coded signal in 100Base-FX mode, and Manchester coded signal in 10Base-T mode.

In 100Base-FX mode, no filtering is performed. The transmit driver utilizes a current drive output which is well balanced and produces a low noise PECL signal. PECL voltage levels are produced with resistive terminations.

In 10BaseT mode, high frequency pre-emphasis is performed to extend the cable-driving distance without the external filter. The FLP and NLP pulses are also drive out through the 10BaseT driver.

The 10BaseT and 100BaseTX transmit signals are multiplexed to the transmit output driver. This arrangement results in using the same external transformer for both the 10BaseT and the 100BaseTX. The driver output level is set by a built-in bandgap reference and an external resistor connected to the RIBB pin. The resistor sets the output current for all modes of operation. The TXOP/N outputs are open drain devices with a serial source to I/O pad resistance of 10 Ω max. When the 1:1 transformer is used, the current rating is 40 mA for the $2V_{p-p}$ MLT-3 signal, and 100 mA for the $5V_{p-p}$ Manchester signal. One can use a 1.25:1 transmit transformer for a 20% output driver power reduction. This will decrease the drive current to 32 mA for 100Base-TX operation, and 80 mA for 10Base-T operation.

Adaptive Equalizer

The Phy is designed to accommodate a maximum of 150 meters UTP CAT-5 cable. An AT&T 1061 CAT-5 cable of this length typically has an attenuation of 31 dB at 100 MHz. A typical attenuation of 100-meter cable is 21 dB. The worst case cable attenuation is around 24-26 dB as defined by TP-PMD specification.

The amplitude and phase distortion from the cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pair cable. The equalizer has the ability to changes its equalizer frequency response according to the cable length. The equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

PLL Clock Synthesizer

The Phy includes an on-chip PLL clock synthesizer that generate 25 MHz and 125 MHz clocks for the 100Base-TX circuitry. It also generates 20 MHz and 100 MHz clocks for the 10BaseT and ANeg circuitry. The PLL clock generator uses a fully differential VCO cell that introduces very low jitter. The Zero Dead Zone Phase Detection method implemented in the Phy design provides excellent phase tracking. A charge pump with charge sharing compensation is also included to further reduce jitter at different loop filter voltages. The on-chip loop filter eliminates the need for external components and minimizes the external noise sensitivity. Only one external 25 MHz clock source is required as a reference clock.

After power-on or reset, the PLL clock synthesizer generates the 20 MHz clock output until the 100Base-X operation mode is selected.

Jabber and SQE (Heartbeat)

After the MAC transmitter exceeds the jabber timer (46mS), the transmit and loopback functions will be disabled and COL signal get asserted. After TX_EN goes low for more than 500 ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse with 5-15BT is asserted after each transmitted packet. SQE is enabled in 10Base-T by default, and can be disabled via SQE Test Inhibit.

Reverse Polarity Detection and Correction

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the Phy has the ability to detect the fact that either 8 NLPs or a burst of FLPs are inverted and automatically reverse the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

If the Auto Polarity Disable bit is set, then the Reverse Polarity bit can be written to force the polarity reversal of the receiver.

INTER-REPEATER INTERFACE

Two busses are provided to allow connection between multiple **AC108Rs,** or combinations of **AC108Rs and AC105s**. The two busses connect directly to the internal repeaters, one at 10M and one at 100M. All necessary CSMA/CD parameters are met on the internal repeater busses. In addition to the internal repeater busses, both 10M and 100M data can be transferred between multiple boxes in a stacked configuration. At power on, reset and stack change times, configuration of multiple devices occurs.

10M INTERNAL REPEATER BUS

Up to 4 **AC108Rs** can be configured to run within a single box. Chip ID's are selected through external pins.

100M INTERNAL REPEATER BUS

INITIALIZATION AND SETUP

HARDWARE CONFIGURATION

Several different states of operation can be chosen through hardware configuration. External pins may be pulled either high or low at reset time. The combination of high and low values determines the power on state of the device.

Many of these pins are multi-function pins which change their meaning when reset ends.

SOFTWARE CONFIGURATION

Several different states of operation can be chosen through software configuration. Please refer to the **SMI** section as well as the **Register Descriptions**.

LEDS

The AC108Rx has an intricate, yet efficient LED scheme allowing up to 64 different LED outputs while only using 16 I/O pins on an 8 x 8 matrix. 8 of the I/O pins, labeled LED_DATA[0:7] drive a single pulse on a consistently timed interval. These 8 signals are the enable signals for the LEDs. The other 8 I/O pins, labeled LED_LN[0:7] drive the actual LED information on the line. When an LED_LN[n] signal is true during the period that the corresponding LED_DATA[n] signal is active, then the LED will light. In all other cases, the LED will not light.

The information contained in LED_LN[0:2] is programmable (See register descriptions.) The default state of these outputs is as follows:

- LED_LN[7] – Alert Coditions
  - LED_DATA[7] – Utilization Domain A
  - LED_DATA[6] – Utilization Domain B
  - LED_DATA[5] – Collision Domain A
  - LED_DATA[4] – Collision Domain B
  - LED_DATA[3] – Memory Domain A
  - LED_DATA[2] – Memory Domain B
  - LED_DATA[1] – Partition Domain A
  - LED_DATA[0] – Partition Domain B
- LED_LN[6] – Collision Histogram Domain A
- LED_LN[5] – Collision Histogram Domain A
- LED_LN[4] – Utilization Histogram Domain B
- LED_LN[3] – Utilization Histogram Domain A
- LED_LN[2] – Programmable
  - Synchronous to LED_Data[n]
- LED_LN[1] –- Port Speed / Partition
  - Synchronous to LED_Data[n]
- LED_LN[0] – Port Link / Activity
  - Synchronous to LED_Data[n]

The histogram features allow an 8-segment bar graph LED to be attached to the corresponding outputs to show the utilization percentage of the specified condition.

Collision Histogram							
66%	32%	16%	8%	4%	2%	1%	1 event
Utilization Histogram							
80%	66%	32%	16%	8%	4%	2%	1%

AUTO-NEGOTIATION

The 10/100 Transceiver is able to run at either 10Mbps over Twisted Pair Copper (10Base-T), 100Mpbs over Twisted Pair Copper (100Base-TX) or 100Mpbs over Fiber Optics (100Base-FX) (port 7 only). Because the Phy sections are all attached to

the internal repeaters, they will only advertise and operate in half duplex mode. To determine the operational state, the Phy has hardware selects and software selects while also supporting Auto-Negotiation and Parallel Detection. To run in 100Base-FX mode, the selection must be done through hardware configuration. There is no support for Auto-Negotiation of the FX interface.

Legitimate operating states are:
- 10Base-T Half Duplex
- 100Base-TX Half Duplex
- 100Base-FX Half Duplex (Port 7 only)

The Phy can be hardware configured to force any one of the above mentioned modes. By forcing the mode, the Phy will only run in that mode, hence limiting the locations where the product will operate.

The Phy is able to negotiate its mode of operation in the twisted pair environment using the Auto-Negotiation mechanism defined in the clause 28 of IEEE 802.3u specification. ANeg can be enabled or disabled by hardware or software control. When the ANeg is enabled, the Phy chooses its mode of operation by advertising its abilities and comparing them with the ability received from its link partner. It can be configured to advertise 100Base-TX or 10Base-T operating in half duplex.

The Auto-Negotiation Advertisement Register contains the current capabilities of each Phy, determined through hardware selects or chip defaults. This information is sent to its link partner during the ANeg process using Fast Link Pulses (FLPs). An FLP is a string of 1s and 0s, each of which has a particular meaning, the total of which is called a Link Code Word. After reset, software can change any of these bits from 1 to 0 and back to 1, but not from 0 to 1. Therefore, the hardware has priority over software.

When ANeg is enabled, the Phy sends out FLPs during the following conditions:
- power on
- link loss
- restart ANEG command

During this period, the Phy continually sends out FLPs while monitoring the incoming FLPs from the link partner to determine their optimal mode of operation. If FLPs are not detected during this phase of operation, Parallel Detection mode is entered (see below).

When the Phy receives 3 identical link code words (ignoring acknowledge bit) from its link partner, it stores these code words, sets the acknowledge bit in the generated FLPs, and waits to receive 3 identical code word with the acknowledge bit set from the link partner. Once this occurs the Phy configures itself to the highest technology that is common to both ends. The technology priorities are:
1. 100Base-TX, half-duplex
2. 10Base-T half-duplex.

Once the ANeg is complete, Auto-Negotiate Complete is set, the Status Register reflects negotiated speed, and the Phy enters the negotiated transmission and reception state. This state will not change until link is lost or the Phy is reset through either hardware or software, or the restart negotiation bit (Reg. 0.9) is set.

PARALLEL DETECTION

Because there are many devices in the field that do not support the ANeg process, but must still be communicated with, it is necessary to detect and link through the Parallel Detection process.

The parallel detection circuit is enabled in the absence of FLPs. The circuit is able to detect:
- Normal Link Pulse (NLP)
- 10Base-T receive data
- 100Base-TX idle

The mode of operation gets configured based on the technology of the incoming signal. If any of the above is detected, the device automatically configures to match the detected operating speed in the half duplex mode. This ability allows the device to communicate with the legacy 10Base-T and 100Base-TX systems, while maintaining the flexibility of Auto-Negotiation.

DIAGNOSTICS

Loopback Operation

Local Loopback and Remote Loopback are provided for testing purpose. They can be enabled through software.

The Local Loopback routes transmitted data through the transmit path back to the receiving path's clock and data recovery module. The loopback data are presented to the PCS in 5 bits symbol format. This loopback is used to check the operation of the 5-bit

symbol decoder and the phase locked loop circuitry. In Local Loopback, the SD output is forced to logic one and TXOP/N outputs are tri-stated.

In Remote Loopback, incoming data is passed through the equalizer and clock recovery, then looped back to the NRZI/MLT3 converter and then to the transmit driver. This loopback is used to ensure the device's connection on the media side. It also checks the operation of the device's internal adaptive equalizer, phase locked loop circuit, and wave-shaper synthesizer. During Remote Loopback, signal detect (SD) output is forced to logic zero.

Cable Length Indicator

The Phy can detect the length of the cable it's attached and display the result in Reg. 20.[7:4]. A reading of [0000] translates to < 10m cable used, [0001] translates to ~ 10 meter of cable, and [1111] translates to 150 meter cable. The cable length value can be used by the network manage to determine the proper connectivity of the cable and to manage the cable plant distribution

RESET AND POWER

The Phy can be reset in three ways:

- During initial power on.
- Hardware Reset: A logic low signal of 150 μs pulse width is applied to RST* pin.
- Software Reset: Write to the Control Register.

Directly following reset, the device will run a memory test on the external ram, and download its initial configuration from the EEPROM.

The power consumption of the device is significantly reduced due to its built-in power management features. Separate power supply lines are used to power the 10BaseT circuitry and the 100BaseTX circuitry. Therefore, the two circuits can be turned-on and turned-off independently. When the Phy is set to operate in 100Base-TX mode, the 10Base-T circuitry is powered down, and vice versa.

The following power management features are supported:

1. Power down mode: This can be achieved by writing to the Control Register. During power down mode, the device is still be able to interface through the SMI.
2. Energy detect / power saving mode: Energy detect mode turns off the power to select internal circuitry when there is no live network connected. Energy Detect (ED) circuit is always turned on to monitor if there is a signal energy present on the media. The SMI circuitry is also powered on and ready to respond to any management transaction. The transmit circuit still send out link pulses with minimum power consumption. If a valid signal is received from the media, the device will power up and resume normal transmit/receive operation. (Patent Pending)
3. Reduced Transmit Drive Strength mode: Additional power saving can be gained at the Phy level by designing with 1.25:1 turns ration magnetic and asserting the TP125 pin at reset.

CLOCK

The clock input must a TTL clock oscillator measured at 25 MHz-100PPM.

BRIDGE FUNCTION

BUFFER INTERFACE

Port B is always connected to 100 Mb repeater core. Port A of the Bridge is connected to 10 Mb repeater core in Mode 00, or to Port 7 in Mode 01. Two collision domain are called Domain "A", and Domain "B" respectively.

The switch engine interface presents an 18-bit address bus for memory access. The SRAM buffer for the two-port switch contains address look-up table and output data queue. The address look-up table consists of 1K entries, 2 layers with each entry occupies 8 words; totaling 8K words. The remaining memory is devoted to output data queueing. For buffer management, each packet occupies 1.5K, 1536 bytes.

FORWARDING SCHEME

The switch supports Store-and-Forward scheme only. It does not support Cut-Through-Forward. With Store-and-forward, the incoming packet must be completely received into the buffer without error before it can be forwarded.

ADDRESS RECOGNITION

The self-learning bridge function is based on source address field of packets. The switch uses 2-layer look-up table and XOR hashing.

Each port of the switch engine will read, store and compare the contents of the Destination Address (DA) and the Source Address (SA) on all incoming packets. If the DA matches a previously stored SA on the same port of the bridge, then the packet will not be forwarded. If the DA does not match, then the packet will be forwarded to the other port of the bridge. All Broadcast packet will be forwarded without comparison.

Too remove the possibility of the SA and DA tables saturating, all entries are marked to be removed after a certain period of time. On reception of a packet on the same port with the same SA, the aging marker is revised. Programmable aging time and fast aging control is supported.

NETWORK MANAGEMENT

Management statistics are maintained on a per port, per repeater and per switch basis. All management information will be retrieved through a simple HDLC interface.

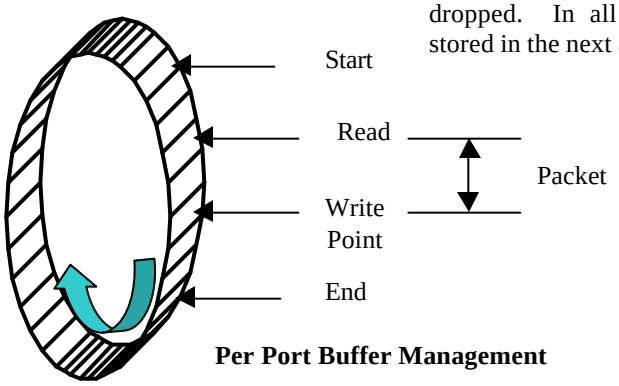
MEDIA ACCESS CONTROL

The switch engine implements all functions of IEEE 802.3 MAC protocol such as frame formatting, collision handling, etc. It generates 56-bit preamble and Start of Frame delimiter while a packet is being sent. In half duplex mode, the switch will perform all required functions of CSMA/CD.

BUFFER MANAGEMENT

The switch buffering management requires 1.5k, 1536 bytes, memory to store one packet. The buffer size of each port is decided by Mode[1:0] and external RAM size[1:0]. Mode 10 sets both sides of bridge to 100M mode, therefore the buffer are made equal. In all other modes it is assumed that the low speed port will need more storage for outgoing packets.

The switch uses the five pointers to control per port buffer status. Start Address is the beginning point of memory address for each port and End Address point is the last entry. These two registers are determined at reset. The Read/Write Pointers are dynamically changed depending on the current outgoing and incoming packets in the storage. If Packet Counter is equal to maximum number of the packets that can be stored, then the buffer is full and the packet is dropped. In all other occurrences, the packet is stored in the next available buffer.



Per Port Buffer Management

BUFFER ALLOCATION

Buffer Allocation						
SRAM Size[1:0]	00(128K)		01(256K)		10(512K)	
Mode[1:0]	10	others	10	others	10	others
Lookup Table	2K Entries					
Maximum Packets for Port 0 (IBQA)	80	100	165	200	336	400
Maximum Packets for Port 1 (IAQB)	80	60	165	130	336	272

REGISTER DESCRIPTIONS

The internal register sets are listed below. Each register contains 32-bit data. The addresses shown below are hexadecimal.

Bold Definitions indicate a group heading, Grayed Definitions indicates the members of the Bolded group. Several Bolded groups do not show the members because they are the same as a previously define group.

Descriptions of the individual registers follows this table.

NOTE: When writing to registers it is recommended that a read/modify/write operation be performed, as unintended bits may get set to unwanted states. This applies to all register, including those with reserved bits.

NOTE: For all registers define as SA5-SA4 and SA3-SA0 for the value 12-34-56-78-9a-bc:

- Example: SA5-SA4 = **xx-xx-bc-9a**
- Example: SA3-SA0 = **78-56-34-12**

Bank	Base Addresss	Definition	Type
0	000 - 00f	**Port 0 Repeater MIB**	
0	000	Readable Frame Count	R
0	001	Readable Byte Count (Lower)	R
0	002	Readable Byte Count (Upper)	R
0	003	CRC Count	R
0	004	Alignment Error Count	R
0	005	Long Frame Count	R
0	006	Short Event Count	R
0	007	Runt Count	R
0	008	Collision Count	R
0	009	Late Event Count	R
0	00a	Very Long Event Count	R
0	00b	Data Rate Mismatch Count	R
0	00c	Auto Partition Count	R
0	00d	SA Change Count	R
0	00e	Broadcast Count	R
0	00f	Multicast Count	R
0	010 - 01f	**Port 1 Repeater MIB**	
0	020 - 02f	**Port 2 Repeater MIB**	
0	030 - 03f	**Port 3 Repeater MIB**	
0	040 - 04f	**MII Port Repeater MIB**	
0	050 – 058	**100XCVR Counters - Port 0-3**	
	050	Port Isolate – Port 0	R
	051	Port Isolate – Port 1	R
	052	Port Isolate – Port 2	R
	053	Port Isolate – Port 3	R
	055	Symbol Error - Port 0	R
	056	Symbol Error - Port 1	R
	057	Symbol Error - Port 2	R
	058	Symbol Error - Port 3	R
0	05c - 06f	**RMON Statistic Counter - Segment 0**	
0	05c	Byte Count (Lower)	R
0	05d	Byte Count (Upper)	R
0	05e	Packet Count	R
0	05f	Broadcast Count	R

Bank	Base Addresss	Definition	Type
0	060	Multicast Count	R
0	061	CRC Alignment Error Count	R
0	062	Undersize Pkt Count	R
0	063	Oversize Pkt Count	R
0	064	Fragment Count	R
0	065	Jabber Count	R
0	066	Collision Count	R
0	067	64 Byte Pkt Count	R
0	068	65-127 Byte Pkt Count	R
0	069	128-255 Byte Pkt Count	R
0	06a	256-511 Byte Pkt Count	R
0	06b	512-1023 Byte Pkt Count	R
0	06c	1024-1522 Byte Pkt Count	R
0	06d	Not Used	
0	06e	Good Byte Count (Lower)	R
0	06f	Good Byte Count (Upper)-	R
0	070	Port 0 Last New SA3~SA0	R
0	071	Port 0 Last New SA5~SA4	R
0	072	Port 1 Last New SA3~SA0	R
0	073	Port 1 Last New SA5~SA4	R
0	074	Port 2 Last New SA3~SA0	R
0	075	Port 2 Last New SA5~SA4	R
0	076	Port 3 Last New SA3~SA0	R
0	077	Port 3 Last New SA5~SA4	R
0	078	MII Port Last New SA3~SA0	R
0	079	MII Port Last New SA5~SA4	R
0	080	Port 0 Authorized SA3~SA0	R/W
0	081	Port 0 Authorized SA5~SA4	R/W
0	082	Port 1 Authorized SA3~SA0	R/W
0	083	Port 1 Authorized SA5~SA4	R/W
0	084	Port 2 Authorized SA3~SA0	R/W
0	085	Port 2 Authorized SA5~SA4	R/W
0	086	Port 4 Authorized SA3~SA0	R/W
0	087	Port 4 Authorized SA5~SA4	R/W
0	088	MII Port Authorized SA3~SA0	R/W
0	089	MII Port Authorized SA5~SA4	R/W
0	08a	Search SA3~SA0	R/W
0	08b	Search SA5~SA4	R/W
0	090	Search Port Match Register	R
0	095	Port Enable Control Register	R/W
0	096	Port Authorized Address Learning Control Register	R/W
0	098	Port Link Status	R
0	099	Port Polarity Status	R
0	09A	Port Partition Status	R
0	09C	Port Speed Status	R
0	09D	Port Isolation Status (Fast Ethernet only)	R
0	09E	Port SA Change Status	R
0	09F	Reserved	R
0	0AB	Repeater Configuration	R/W

Bank	Base Addresss	Definition	Type
0	0AC	Repeater Serial Configuration	R
0	0AD	Device/Revision ID	R
0	0AE	Interrupt Status	R/W
0	0AF	Interrupt Mask	R/W
0	0B4	MII Port Status	R
0	0B5	Repeater Reset Register	R
0	0B6	Software Reset Register	R
0	0BA	Bridge Configuration Register 1	R/W
0	0BB	Bridge Configuration Register 2	R/W
0	0C0 – 0DF	**Phy 0 Registers**	
0	0C0	Control Register	R/W
0	0C1	Status Register	R/W
0	0C2	Phy Identifier 1 Register	R/W
0	0C3	Phy Identifier 2 Register	R/W
0	0C4	Auto-Neg Advertisement Register	R/W
0	0C5	Auto-Neg Link Partner Register	R/W
0	0C6	Auto-Neg Expansion Register	R/W
0	0C7	Auto-Neg Next Page Register	R/W
0	0D0	Extended Control Register	R/W
0	0D1	Adaptation Control Register	R/W
0	0D2	Auto-Neg Test Register	R/W
0	0D3	Reserved	R/W
0	0D4	DLOCK Drop Counter Register	R/W
0	0D5	Receive Error Counter Register	R/W
0	0D6	Power Management Register	R/W
0	0E0 – 0FF	**Phy 1 Registers**	
0	100 – 11F	**Phy 2 Registers**	
0	120 – 13F	**Phy 3 Registers**	
0	140 – 15F	**Phy 4 Registers**	
0	160 – 17F	**Phy 5 Registers**	
0	190	EEPROM Address 1	
0	191	EEPROM Address 2	
0	1A0 – 1BF	**Phy 6 Registers**	
0	1C0 – 1DF	**Phy 7 Registers**	
0	1E0 – 1EF	**Led Effect Register**	
0	1E0	Reserved	R
0	1E1	LED Effect With Port Enable Event	R
0	1E2	LED Effect With Partition/Isolation Event	R
0	1E3	LED Effect With Link Event	R
0	1E4	LED Effect With Activity (CRS) Event	R
0	1E5	LED Effect With Autoneg Event	R
0	1E6	LED Effect With Speed100 Event	R
0	200 - 207	**Ether-Like/Bridge MIB - Segment 0**	
0	200	Single Col Frame	R
0	201	Multiple Col Frame	R
0	202	Deferred Transmission	R
0	203	Late Col Frame	R
0	204	Excessive Col Frame	R
0	205	Delay Exceeded Discard Frame	R

Bank	Base Addresss	Definition	Type
0	206	Drop Event Count	R
0	207	Drop Packet Count	R
0	300 – 31F	**Phy Global Register**	
1	000 - 00f	**Port 4 Repeater MIB**	
1	010 - 01f	**Port 5 Repeater MIB**	
1	020 - 02f	**Port 6 Repeater MIB**	
1	030 - 03f	**Port 7 Repeater MIB**	
1	040 - 04f	**Not Used**	
1	050 - 058	**100XCVR Counters - Port 4-7**	
1	05c - 06f	**RMON Statistic Counter - Segment 1**	
1	05c	Byte Count(Lower)	R
1	05d	Byte Count(Upper)	R
1	05e	Packet Count	R
1	05f	Broadcast Count	R
1	060	Multicast Count	R
1	061	Crc Alignment Error Count	R
1	062	Undersize Pkt Count	R
1	063	Oversize Pkt Count	R
1	064	Fragment Count	R
1	065	Jabber Count	R
1	066	Collision Count	R
1	067	64 Byte Pkt Count	R
1	068	65-127 Byte Pkt Count	R
1	069	128-255 Byte Pkt Count	R
1	06a	256-511 Byte Pkt Count	R
1	06b	512-1023 Byte Pkt Count	R
1	06c	1024-1522 Byte Pkt Count	R
1	06d	Not Used	R
1	06e	Good Byte Count(Lower)	R
1	06f	Good Byte Count(Upper)-	R
1	070	Port 4 Last New SA3~SA0	R
1	071	Port 4 Last New SA5~SA4	R
1	072	Port 5 Last New SA3~SA0	R
1	073	Port 5 Last New SA5~SA4	R
1	074	Port 6 Last New SA3~SA0	R
1	075	Port 6 Last New SA5~SA4	R
1	076	Port 7 Last New SA3~SA0	R
1	077	Port 7 Last New SA5~SA4	R
1	078 - 079	**Not Used**	
1	080	Port 4 Authorized SA3~SA0	R/W
1	081	Port 4 Authorized SA5~SA4	R/W
1	082	Port 5 Authorized SA3~SA0	R/W
1	083	Port 5 Authorized SA5~SA4	R/W
1	084	Port 6 Authorized SA3~SA0	R/W
1	085	Port 6 Authorized SA5~SA4	R/W
1	086	Port 7 Authorized SA3~SA0	R/W
1	087	Port 7 Authorized SA5~SA4	R/W
1	088 - 089	Not Used	R/W

Bank	Base Addresss	Definition	Type
1	200 - 207	**Ether-Like/Bridge MIB - Segment 1**	R
1	200	Single Col Frame	
1	201	Multiple Col Frame	
1	202	Deferred Transmission	
1	203	Late Col Frame	
1	204	Excessive Col Frame	
1	205	Delay Exceeded Discard Frame	
1	206	Drop Event Count	
1	207	Drop Packet Count	

GLOBAL REGISTERS

Repeater MIB

Name	Description
Readable frame count	Counts valid (error free) packets. Unicast-only (Reg.0ab) = 0: counts all packets. Unicast-only (Reg.0ab) = 1: counts Unicast Packets only.
Readable byte count (lower)	Counts the number of Octets in all valid packets, not including preamble and framing bits. This counter is not affected by Unicast-only bit.
Readable byte count (upper)	
CRC count	Counts valid length, collision-free packets that had FCS error, but were correctly framed (had an integral number of octets).
Alignment error count	Counts valid length, collision-free packets that had FCS error and were incorrectly framed (had an non-integral number of octets).
Long frame count	Counts packets (good or bad) that had a length greater than 1518 octets.
Short event count	Counts events that lasted for less than ShortEventMaxTime.. 100M : ShortEventMaxTime = 84 bit times, 10M : ShortEventMaxTime = 77 bit times.
Runt count	Counts events longer than ShortEventMaxTime, but shorter than ValidPacketMinTime; or packets longer than ShortEventMaxTime, but octets less than 64 bytes. ValidPacketMinTime = 560 bit times.
Collision count	Counts the number of collisions that occurred, including late collision.
Late event count	Counts the number of collisions detected after the LateEventThreshold. 100M: LateEventThreshold = 484 bit times. 10M: LateEventThreshold = 500 bit times.
Very long event count	Counts events that lasted for longer than 4 to 7.5 ms.
Data rate mismatch count	Counts the number of times the incoming data rate mismatched the local clock source enough to cause a FIFO underflow or overflow.
Auto partition count	Counts the number of times this port has been partitioned by the Auto-partition Algorithm.
SA change count	Counts the number of times the source address has changed.
Broadcast count	Counts the number of good broadcast packets received by this port.
Multicast count	Counts the number of good multicast packets received by this port.

100XCVR Counters

Name	Description
Port Isolate – Port n	Counts the number of times a port auto isolates.
Port Isolate – Port n	
Port Isolate – Port n	
Port Isolate – Port n	
Symbol Error - Port n	Counts the number of time a packet contained at least one symbol error.
Symbol Error - Port n	
Symbol Error - Port n	
Symbol Error - Port n	

RMON Statistic Counter

Name	Description
Byte count(lower)	The number of data octets including those in good and bad packets and octets in FCS fields, but does not include preamble or other framing bits.
Byte count(upper)	
Packet count	The number of packets received from the network, including good and bad packets.
Broadcast count	The number of good broadcast packets received.
Multicast count	The number of good multicast packets received.
CRC Alignment error count	The number of valid-length packets that had a bad Frame Check Sequence.
Undersize pkt count	The number of well-formed packets that were smaller than 64 octets.
Oversize pkt count	The number of well-formed packets that were longer than 1518 octets.
Fragment count	The number of ill-formed packets less than 64 octets. Any event without a SFD (0-octet oacket, e.g., jamed packets caused by collision) will be count as a fragment, no matter how long it is.
Jabber count	The number of ill-formed packets longer than 1518 octets. An ill-formed packet is one with FCS error.
Collision count	The best estimate of the total number of collision on this interface.
64 byte pkt count	The number of packets (good and bad) that were 64 octets long.
65-127 byte pkt count	The number of packets (good and bad) that were 65 to 127 octets long.
128-255 byte pkt count	The number of packets (good and bad) that were 128 to 255 octets long.
256-511 byte pkt count	The number of packets (good and bad) that were 256 to 511 octets long.
512-1023 byte pkt count	The number of packets (good and bad) that were 512 to 1023 octets long.
1024-1518 byte pkt count	The number of packets (good and bad) that were 1024 to 1518 octets long.
Not used	
Good byte count (lower)	The total number of octets contained in valid frames received on this segment.
Good byte count (upper)	

Port n Last New Address Registers

Name	Description
Port n last new SA3~SA0	Last received source address.
Port n last new SA5~SA4	

Port n Authorized Address Registers

Name	Description
Port n Authorized SA3~SA0	Address comparison. (see Port Learn Control Register)
Port n Authorized SA5~SA4	

Search Address Registers

Name	Description
Search SA3~SA0	Address used for search function. Default to 00-00-00-00-00-00
Search SA5~SA4	
Search Port Match Register	Bit 0-8 indicate which port matched the Search Address.

31:9	8	7	6	5	4	3	2	1	0
RSV	MII Port	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1	Port 0

Port Status Registers

Name	Description
Port Enable Control Register	1 = Port Enabled If pin MGR_PRES_ is low during reset, all ports will be disabled until the management software re-enables them. Otherwise, all ports will power on enabled.
Port Link Status	1= LINK GOOD, default = 0
Port Polarity Status	1= the polarity has been crossed, default = 0
Port Partition Status	1= the port has been partitioned, default = 0
Port Speed Status	1= 100M, 0:10M, default = 0
Port Isolation Status (Fast Ethernet only)	1= port has been isolated, default = 0
Port SA Change Status	1= source address changed, default = 0
Reserved MII Port Status	Reserved Bits 31:2 Reserved Bit 1 0=10M, 1=100M Bit 0 1=Phy Mode (Always 1)

Port Enable Control Register

Bit	Name	Description	Mode	Default
31	LFSR_TEST	1: Reduce LFSR timer for Jabber, Partition.	R/W	0
30:19	Reserved		R	0
18	RAMBIST_STATUS	Internal SSRAM BIST Result. 0=Pass, 1=Fail.	R	0
17:16	auth_cntl9	MII port Authorized Address Learning Mode.	R/W	00
15:14	auth_cntl8	Port 7 Authorized Address Learning Mode.	R/W	00
13:12	auth_cntl7	Port 6 Authorized Address Learning Mode.	R/W	00
11:10	auth_cntl6	Port 5 Authorized Address Learning Mode.	R/W	00
9:8	auth_cntl5	Port 4 Authorized Address Learning Mode.	R/W	00
7:6	auth_cntl4	Port 3 Authorized Address Learning Mode.	R/W	00
5:4	auth_cntl3	Port 2 Authorized Address Learning Mode.	R/W	00
3:2	auth_cntl2	Port 1 Authorized Address Learning Mode.	R/W	00
1:0	auth_cntl1	Port 0 Authorized Address Learning Mode. 0 0 Learn Each new SA. 0 1 Learn the first SA only, then change these two bits to “10” thus locking down the address. 1 0 Lock. Hardware has locked down the address, only software can now write to this address. 1 1 Reserved.	R/W	00

Interrupt Registers

Name			Description							
Interrupt Status			Default = 0							
Interrupt Mask			1= Mask, 0=UnMask							
31	30	29:8	7	6	5	4	3	2	1	0
RSV	SA Match	RSV	Far End Fault	RSV	Jabber	Isolation	Partition	FCC	SA Change	Speed Change

Repeater Configuration Register

Bit	Name	Description	Mode	Default
31:15	Reserved		R/W	N/A
14:13	Mode	00 = Stack Master 8 Port + Bridge 01 = Stand Alone 8 Port 10 = Stand Alone 7 Port + Bridge + 1 Port. Port 7 is connected to the bridge port in this mode. The other bridge port is connected to 100 segment. 11 = Illegal configuration	R/W	MODE pins
12	Late enable	0 = enable Late Event counter. 1 = disable Late Event counter.		
11	Write clear enable	0 = causes Interrupt Status Register, Search Port Match Register, and SA Change status registers to auto-clear when read. 1= requires that the appropriate register bit be written to be clear. This is done by writing a '1' to the bit(s) that are to be cleared.		
10	MIB enable	1 = enable statistics gathering, 0 = disable.		
9	Send T/R	Not function.	R/W	0
8	Isolate 100	1 = disable 100M stack signals and external backplane transceiver. 0 = enable.	R/W	0
7	Isolate 10	1 : disable 10M stack signals and external backplane transceiver. 0 : enable.	R/W	1
6	Unicast only	Changes the definition of ReadFrames counter to count Unicast packets only. 1 = counts unicast only. 0 = counts all packets.	R/W	0
5	Arbit Input Value	As read from Arbit input pin.	R	0
4	Reset MIB Counter	Writing a 1 will reset all MIB counters, this bit will reset to '0' after all counters have been cleared.	R/W	0
3	Reserved		R/W	0
2	Reserved		R	N/A
1	100M repeater Partition Alternative	0 = un-partition a port only when data can be transmitted out from the port for 560 bit-time without a collision. 1 = un-partition a port when data can be either transmitted from the port or received from the port for 560 bit-time without a collision.	R/W	0
0	10M repeater Partition Alternative	0 = un-partition a port when data can be either transmitted from the port or received from the port for 560 bit-time without a collision. 1 = un-partition a port only when data can be received from the port for 560 bit-time without a collision	R/W	0

Miscellaneous Registers

Name	Description
Repeater Serial Configuration	This 8-bit register holds user-defined data
Device/Revision ID	
Repeater Reset Register	Any write to this register causes repeater logic Reset.
Software Reset Register	Any write to this register is identical to hardware reset.
EEPROM Address 1	Bits 47:16 of EEPROM serial number.
EEPROM Address 2	Bits 15:0 of EEPROM serial number.

Bridge Configuration Register 1

Bit	Name	Description	Mode	Default
31:15	Reserved		R/W	N/A
10	Disable Switch	0=enable, 1=disable switch function	R/W	0
9	Disable Aging	0=enable, 1=disable Aging function	R/W	0
8	Fast Aging Enable	0 = 300 Seconds per Unit, 1=6 Seconds per Unit	R/W	0
7:0	Aging Timer	This count times the Seconds per unit equals Aging Timout. EG. 010h * 300 Seconds per unit = 4800 Seconds 010h * 6 Seconds per unit = 96 Seconds	R/W	01h

Bridge Configuration Register 2

Bit	Name	Description	Mode	Default
31:16	Reserved		R/W	N/A
15:8	IPG Timer1	10/100M segment IPG adjustment. Bit 15 is the sign bit. When the value is 0, the IPG is set to 96BT. One unit will increase or decrease 1BT for SNI mode and 4BT for MII mode.	R/W	0
7:0	IPG Timer0	10/100M segment IPG adjustment. Bit 15 is the sign bit. When the value is 0, the IPG is set to 96BT. One unit will increase or decrease 1BT for SNI mode and 4BT for MII mode.	R/W	01h

LED Effect with Port Enable Event.

Bit	Name	Description	Mode	Default
15:12	Blink Rate [3:0]	Set the blink rate bits [3:0]	RW	0000
11	Reserved		RO	0
10:8	LED On with Port Enable Event	When Port Enable, turn on corresponding LED 2:0.	RW	011
7	Reserved		RO	0
6:4	LED Blink with Port Enable Event	When Port Enable, blink corresponding LED 2:0.	RW	011
3	Reserved		RO	0
2:0	LED Off with Port Enable Event	When Port Enable, turn off corresponding LED 2:0.	RW	000

LED Effect with Partition/Isolation Event.

Bit	Name	Description	Mode	Default
15:12	Blink Rate [7:4]	Set the blink rate bits [7:4].	RW	0001
19	Reserved		RO	0
10:8	LED On with Part/ISO Event	When Partition/Isolation, turn on corresponding LED 2:0.	RW	000
7	Reserved		RO	0
6:4	LED Blink with Part/ISO Event	When Partition/Isolation, blink corresponding LED 2:0.	RW	010
3	Reserved		RO	0
2:0	LED Off with Part/ISO Event	When Partition/Isolation, turn off corresponding LED 2:0.	RW	000

LED Effect with Link Event.

Bit	Name	Description	Mode	Default
15:11	Reserved		RO	00000
10:8	LED On with Link Event	When Link Up, turn on corresponding LED 2:0.	RW	011
7	Reserved		RO	0
6:4	LED Blink with Link Event	When Link Up, blink corresponding LED 2:0.	RW	011
3	Reserved		RO	0
2:0	LED Off with Link Event	When Link Up, turn off corresponding LED 2:0.	RW	000

LED Effect with Activity (CRS) Event.

Bit	Name	Description	Mode	Default
15:11	Reserved		RO	00000
10:8	LED On with Activity Event	When Activity, turn on corresponding LED 2:0.	RW	000
7	Reserved		RO	0
6:4	LED Blink with Activity Event	When Activity, blink corresponding LED 2:0.	RW	001
3	Reserved		RO	0
2:0	LED Off with Activity Event	When Activity, turn off corresponding LED 2:0.	RW	000

LED Effect with Auto-Negotiating Event.

Bit	Name	Description	Mode	Default
15:11	Reserved		RO	00000
10:8	LED On with Auto-negotiating Event	When Auto-negotiating, turn on corresponding LED 2:0.	RW	000
7	Reserved		RO	0
6:4	LED Blink with Auto-negotiating Event	When Auto-negotiating, blink corresponding LED 2:0.	RW	000
3	Reserved		RO	0
2:0	LED Off with Auto-negotiating Event	When Auto-negotiating, turn off corresponding LED 2:0.	RW	000

LED Effect with Speed100 Event.

Bit	Name	Description	Mode	Default
15:11	Reserved		RO	00000
10:8	LED On with Speed100 Event	When Speed100, turn on corresponding LED 2:0.	RW	010
7	Reserved		RO	0
6:4	LED Blink with Speed100 Event	When Speed100, blink corresponding LED 2:0.	RW	000
3	Reserved		RO	0
2:0	LED Off with Speed100 Event	When Speed100, turn off corresponding LED 2:0.	RW	000

LED Register Control Mode.

Bit	Name	Description	Mode	Default
15:8	LED Data	Set value shown on the LED_DATA [7:0].	RW	0
7:0	LED Column	Control which lane of the LED_DATA should be turned on.	RW	0

PHY REGISTERS

The following registers are defined for each PHY port. The register addresses are offset addresses. The actual address has to be calculated with their base address. The base addresses of PHY-0 to PHY-7 are 0C0, 0E0, 100, 120, 140, 160, 1A0, and 1C0 respectively. All of the addresses are hexadecimal.

Control Register

Bit	Name	Description	Mode	Default
15	Reserved		RO	0
14	Loopback	1 = Loopback mode, which internally loops the transmit to the receive, thus it will ignore all the activity on the cable media. 0 = Normal operation.	RW	0
13	Speed Select	1 = 100Mbps 0 = 10Mbps. This bit will be ignored if Auto-Negotiation is enabled. It will no longer reflect auto-negotiation result.	RW	0 (Port 7 depends on fxsel & mode)
12	Auto-Neg Enable	1 = Enable auto-negotiate process (overrides 0.13 and 0.8) 0 = Disable auto-negotiate process. In force mode, speed is selected via bit 0.13.	RW	1 (Port 7 depends on fxsel & mode)
11	Power Down	1 = Power down mode, which puts device in low-power stand-by mode, which only react to management transaction. 0 = Normal operation.	RW	0
10	Isolate	1 = Electrical isolation of PHY from MII ***and cable medi***a. 0 = Normal operation.	RW	0
9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process. 0 = Normal operation.	RW/ SC	0
8	Duplex Mode	1 = Full duplex. 0 = Half duplex. Full duplex is not supported on this chip. It will no longer reflect auto-negotiation result.	RO	0
7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal. 0 = Disable COL test.	RW	0
6:0	Reserved		R0	000000

Status Register

Bit	Name	Description	Mode	Default
15	100Base-T4	Tied to zero indicates no 100BaseT4 capability.	RO	0
14	100Base-TX Full Duplex	Tied to zero indicates no 100BaseTX full duplex support.	RO	0
13	100Base-TX Half Duplex	1 = 100BaseTX with half duplex. 0 = No TX Half-Duplex ability.	RO	1
12	10Base-T Full Duplex	Tied to zero indicates no 10Base-T full duplex support.	RO	0
11	10Base-T Half Duplex	1 = 10BaseT with half duplex. 0 = No 10BaseT Half-Duplex ability.	RO	1
10:6	Reserved		RO	00000
5	Auto-Negotiate Complete	1 = Auto-negotiate process completed, indicates Reg. 4, 5, 6 are valid. 0 = Auto-negotiate process not completed.	RO	N/A
4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. After this bit is set, it will remain set until it is clear by reading register 1 via management interface.	SC/LH	N/A
3	Auto-Negotiate Ability	1 = Able to perform auto-negotiation function, its value is determined by ANEGA pin. 0 = Unable to perform auto-negotiation function.	RO	1
2	Link Status	1 = Link is established, however, if link fails, this bit will become cleared and remain cleared until register is read via management interface. 0 = Link is down, or have been dropped.	SC/LL	0
1	Jabber Detect	1 = Jabber condition detect. 0 = No Jabber condition detected.	SC/LH	0
0	Extended Capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

PHY Identifier 1 Register

Bit	Name	Description	Mode	Default
15:0	OUI*	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022 (HEX)

PHY Identifier 2 Register

Bit	Name	Description	Mode	Default
15:10	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	010101
9:4	Model Number	Six bit manufacturer's model number; 101 is encoded as 010001.	RO	011000
3:0	Revision Number	Four bits manufacturer's revision number. 0001 stands for Rev. A, etc.	RO	0001

Auto-Negotiation Advertisement Register

Bit	Name	Description	Mode	Default
15	Next Page	1 = Desire Next Page. 0 = Next Page is not desired.	RW	0
14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
13	Remote Fault	1 = Remote fault detected. 0 = No remote fault.	RW	0
12:10	Reserved	For future technology.	RW	000
9	100Base-T4	Tied to zero indicates no 100Base-T4 support.	RO	0
8	100Base-TX Full Duplex	1 = 100BaseTX with full duplex. 0 = No 100BaseTX full duplex ability.	RO	0
7	100Base-TX	1 = 100BaseTX capable. 0 = No 100BaseTX capability.	RW	1
6	10Base-T Full Duplex	1 = 10Mbps with full duplex. 0 = No 10Mbps with full duplex capability.	RO	0
5	10Base-T	1 = 10Mbps capable. 0 = No 10Mbps capability.	RW	1
4:0	Selector Field	[00001] = IEEE 802.3.	RO	00001

Auto-Negotiation Link Partner Ability Register

Bit	Name	Description	Mode	Default
15:0	Technology	Technology capability field, which indicates the technology capability of link partner. The bit definition is the same as Reg. 4.15:0.	RO	0001(H)

Auto-Negotiation Expansion Register

Bit	Name	Description	Mode	Default
15:5	Reserved		RO	0000 0000 000
4	Parallel Detection Fault	1 = Fault detected by parallel detection logic. This is caused by unstable link, or concurrent link up condition. 0 = No fault detected by parallel detection logic.	SC/LH	0
3	Link Partner Next Page Able	1 = Link partner supports next page function. 0 = Link partner does not support next page function.	RO	0
2	Next Page Able		RO	1
1	Page Received	1 = A new link code word has been received. The contains of the received link code word is located in Register 5.	SC/LH	0
0	Link Partner Auto-Negotiation Able	1 = Link partner is auto-negotiation able. 1 = Link partner is not auto-negotiation able.	RO	0

Auto-Negotiation Next Page Transmit Register

Bit	Name	Description	Mode	Default
15	NP	1 = Another Next Page is desired.	RW	0
14	Reserved		RO	0
13	Message Page	1 = Message page. 0 = Un-formatted Page.	RW	1
12	ACK2	Acknowledge2. 1 = Will comply with message. 0 = Can not comply with message.	RW	0
11	Toggle	1 = Previous value of transmitted Link Code Word equal to 0. 0 = Previous value of transmitted Link Code Word equal to 1.	RO	N/A
10:0	Code	Message/Un-formatted Code Field.	RW	0001

Extended Control Register

Bit	Name	Description	Mode	Default
15	Repeater	1 = Repeater mode. CRS only responds to receive activity. 0 = DTE mode.	RW	1
14	CIM Disable	1 = Disable carrier integrity monitor function. Default is 1 when autoneg is enable. Once speed is set to 100mbps, this bit will be set to '0'.	RW	1
13	FEF Enable	1 = Enable FEF generation and detection. 0 = Enable FEF generation and detection. When FX is selected, FEF should be enabled. Otherwise, it should be disabled.	RW	0
12	FX SEL	1 = Enable FX mode. 0 = Disable FX mode.	RW	0/Port 7 depend on fxsel
11	TP125	1 = Uses 1.25:1 transformer. 0 = Uses 1:1 transformer.	RW	0
10	SDN Select	1 = Select internal common voltage setting. 2 = Select external common voltage setting.	RW	0
9	Scramble Disable	1 = Disable scramble. 0 = Enable scramble.	RW	0
8:0	Reserved		RO	0 0000 0000

Auto-Negotiation Test Register.

Bit	Name	Description	Mode	Default
15	LP loop back	1 = Link pulse loop back mode. 0 = Normal operation.	RW	0
14	Force Send NLP	1 = Force link control state machine to send NLP even in auto-negotiation mode. 0 = Normal operation.	RW	0
13	Force BT Link Up	1 = Force NLP link integrity state machine to link up state. 0 = Normal operation.	RW	0
12	Force TX Link Up	1 = Force link monitor to link up state. 0 = Normal operation.	RW	0
11:10	Reserved		RO	00
9	Arb_Speed	1 = Auto-Negotiation result is 100 TX. 2 = Auto-Negotiation result is 10 BT.	RO	Depends on ANeg result
8	Arb_Duplex	1 = Auto-Negotiation result is full duplex. 0 = Auto-Negotiation result is half-duplex.	RO	Depends on ANeg result
7:4	Arbitration State High	Highest state of Auto-Negotiation State Machine since reset or last read operation.	SC/RO	0000 Depends on ANeg state
3:0	Arbitration State Low	Lowest state of Auto-Negotiation State Machine since reset or last read operation.	SS/RO	1111 Depends on ANeg state

Receive Error Counter

Bit	Name	Description	Mode	Default
15:0	Receive Error Counter	Number of Receive Error Event.	RO	0000

EEPROM TABLE

Table of locations and information required for initial setup of Bridge, Repeater and Transceiver.

Address	Description	Assign to…
0	First Word	
1	Port Enable	Reg 095
2	MII port Authorized Address Learning Mode.	Reg 096
3	Port 0-7 Authorized Address Learning Mode.	Reg 096
4	Initial Repeater Configuration Registers	Reg 0AB
5	Initial Repeater Serial Configuration	Reg 0AC
6	Bridge Configuration Register 1	Reg 0BA
7	Bridge Configuration Register 2	Reg 0BB
8	Reserved	Reg 0BF[17:9]
9	Reserved	Reg 0BF[8:0]
10	Initialize Port 0 Control Register	Reg 0C0
11	Initialize Port 0 Extended Control Register	Reg 0D0
12	Initialize Port 1 Control Register	Reg 0E0
13	Initialize Port 1 Extended Control Register	Reg 0F0
14	Initialize Port 2 Control Register	Reg 100
15	Initialize Port 2 Extended Control Register	Reg 110
16	Initialize Port 3 Control Register	Reg 120
17	Initialize Port 3 Extended Control Register	Reg 130
18	Initialize Port 4 Control Register	Reg 140
19	Initialize Port 4 Extended Control Register	Reg 150
20	Initialize Port 5 Control Register	Reg 160
21	Initialize Port 5 Extended Control Register	Reg 170
22	Initialize Port 6 Control Register	Reg 1A0
23	Initialize Port 6 Extended Control Register	Reg 1B0
24	Initialize Port 7 Control Register	Reg 1C0
25	Initialize Port 7 Extended Control Register	Reg 1D0
26	Test Control Register	Reg 1E0
27	LED Effect with Port Enable Event	Reg 1E1
28	LED Effect with Partition/Isolation Event	Reg 1E2
29	LED Effect with Link Event	Reg 1E3
30	LED Effect with Activity (CRS) Event	Reg 1E4
31	LED Effect with AutoNeg Event	Reg 1E5
32	LED Effect with Speed100 Event	Reg 1E6
33	Bits 47:32 of EEPROM serial number.	Reg 190[31:16]
34	Bits 31:16 of EEPROM serial number.	Reg 190[15:0]
34	Bits 15:0 of EEPROM serial number.	Reg 191[15:0]

4B/5B CODE-GROUP TABLE

PCS Code Group[4:0]	SYMBOL Name	MII (TXD/RXD [3:0])	Description
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F
Idle and Control Code			
11111	I	0000	Inter-Packet Idle; used as inter-stream fill code.
11000	J	0101	Start of stream delimiter, part 1 of 2; always use in pair with K symbol.
10001	K	0101	Start of stream delimiter, part 2 of 2; always use in pair with J symbol.
01101	T	Undefined	End of stream delimiter, part 1 of 2; always use in pair with R symbol.
00111	R	Undefined	End of stream delimiter, part 2 of 2; always use in pair with T symbol.
Invalid Code			
00100	H	Undefined	Transmit Error; used to send HALT code-group
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

ELECTRICAL CHARACTERISTICS

NOTE: The following electrical characteristics are design goals rather than characterized numbers.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature..... -55^{o}C to +150^{o}C
Vcc Supply Referenced to GND..... -0.5V to +5.0V
Digital Input Voltage..... -0.5V to Vcc
DC Output Voltage..... -0.5V to Vcc

OPERATING RANGE

Operating Temperature(Ta) ..... 0^{o}C to +70^{o}C
Vcc Supply Voltage Range(Vcc) ..... 2.97V to 3.63V

Total Power Consumption

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current (per port)	Icc	10 Base-T, Idle		25	30	mA
		10 Base-T, Normal activity		41	75	mA
		100 Base-TX		85	100	mA
		100 Base-FX		30	40	mA
		10/100 Base-TX, low power without cable		12	15	mA
		Power down			1	mA
Supply Current (dual speed hub)	Icc	Mode 00		175	200	mA
		Mode 01		140	180	mA
		Mode 10		175	200	mA

TTL I/O Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage High	Vih		2.0			V
Input Voltage Low	Vil				0.8	V
Input Current	Ii		-10		10	mA
Output Voltage High	Voh		VCC-0.4			V
Output Voltage Low	Vol				0.4	V
Output Current High	Ioh				8	mA
Output Current Low	Iol		-8			mA
Input Capacitance	Ci			10		pF
Output Transition Time		3.15V < VCC < 3.45V		5		ns
Tristate Leakage Current	|Ioz|				10	uA

REFCLK and XTAL Pins

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0			V
Input Clock Frequency Tolerance	F				±50	ppm
Input Clock Duty Cycle	Tdc		40		60	%
Input Capacitance	Cin			3.0		pF

I/O Characteristics – LED/CFG Pins

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Voltage	Vol				0.4	V
Output High Voltage	Voh		2.4			V
Input Current	Ii		-8		8	mA
Output Current	Io		-10		10	mA

100 BASE-TX Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak to Peak Differential Output Voltage	Vp	Note 1	1.9	2.0	2.1	V
Output Voltage Symmetry	Vss	Note 1	.98		1.02	mV
Signal Rise/Fall Time	Trf	Note 1	3.0		5.0	ns
Rise/Fall Time Symmetry	Trfs	Note 1	3	4	4	ns
Duty Cycle Distortion	Dcd				±250	ps
Overshoot/Undershoot	Vos				5	%
Output Jitter		Scrambled Idle			1.4	ns
Receive Jitter Tolerance					4	ns
Output Current High	Ioh	1:1 Transformer			40	mA
Output Current High	Ioh	1.25:1 Transformer			32	mA
Common Mode Input Voltage				1.8		V
Common Mode Input Current					10	uA
Differential Input Resistance				5		KΩ
Note 1: 50Ω (± 1%) resistor to VCC on each output						

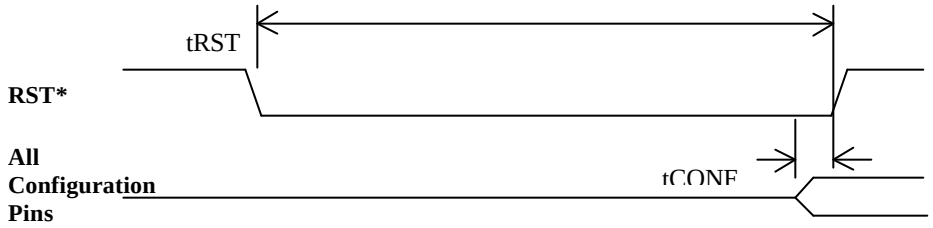
10 BASE-T Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak to Peak Differential Output Voltage	Vop	Note 1	4.5	5	5.5	V
Signal Rise/Fall Time			1		4	ns
Output Current Sink				15	16	mA
Output Current High	Ioh	1:1 Transformer			100	mA
Output Current High	Ioh	1.25:1 Transformer			80	mA
Start of Idle Pulse Width			300		350	ns
Output Jitter					1.4	ns
Receive Jitter Tolerance					32	ns
Receive Input Impedance	Zin		3.6			KΩ
Differential Squelch Threshold	Vds		300	400	500	mV
Common Mode Rejection				25		V
Differential Input Resistance			25			KΩ
Note 1: 50Ω (± 1%) resistor to VCC on each output						

DIGITAL TIMING CHARACTERISTICS

Power on Reset

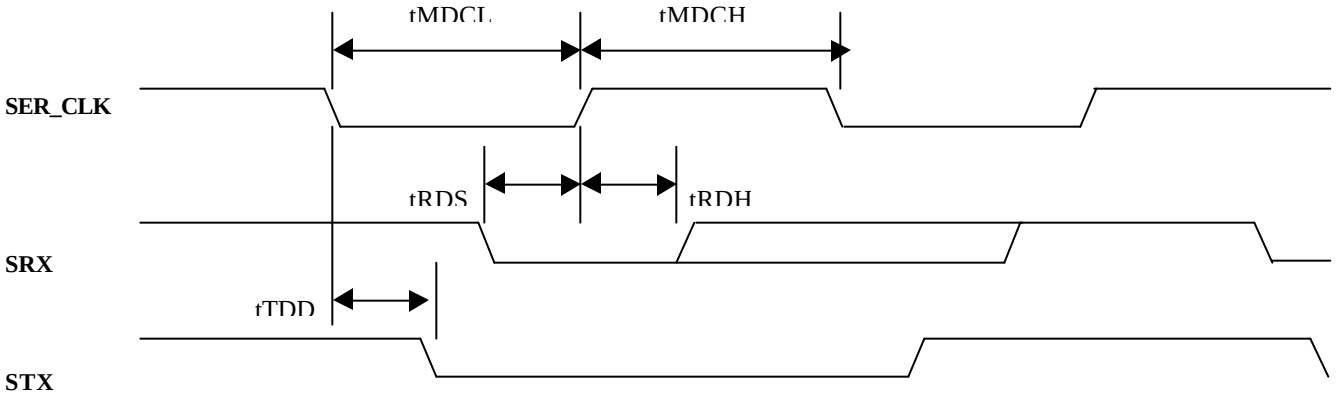
Parameter	SYM	Conditions	Min	Typ	Max	Units
RST* Low Period	tRST		150	-	-	µs
Configuration	tCONF		100	-	-	ns



Power on Reset Timing

Management Data Interface

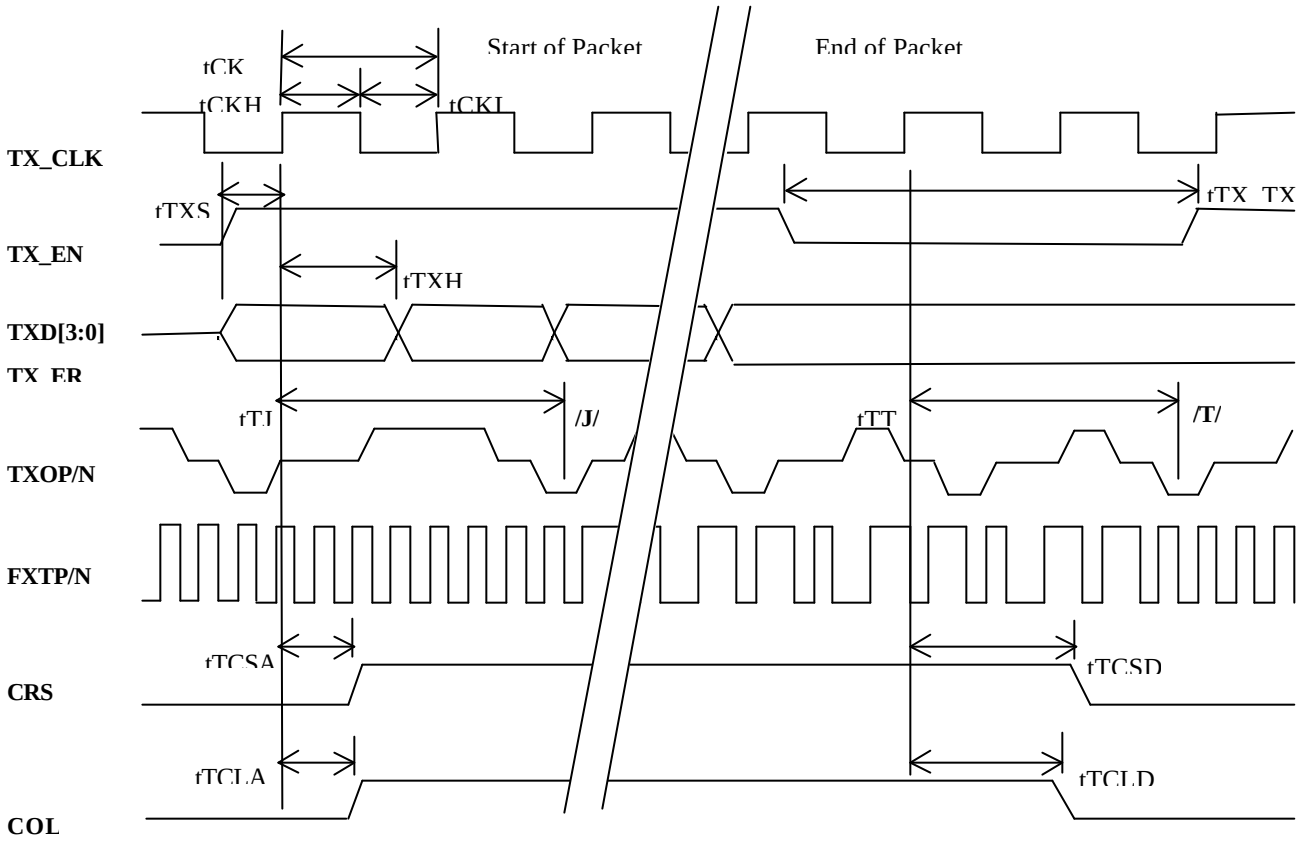
Parameter	SYM	Conditions	Min	Typ	Max	Units
Mgt CLOCK	tMDCL		-	-	-	ns
Mgt CLOCK	tMDCH		-	-	-	ns
Receive Data Setup	tRDS	Setup on Read Cycle	-	-	-	ns
Receive Data Hold	tRDH	Hold on Read Cycle	-	-	-	ns
Transmit Data Delay	tTDD	Delay on Write Cycle	-	-	-	ns



Management Data Interface Timing

100Base-TX/FX MII Transmit System Timing

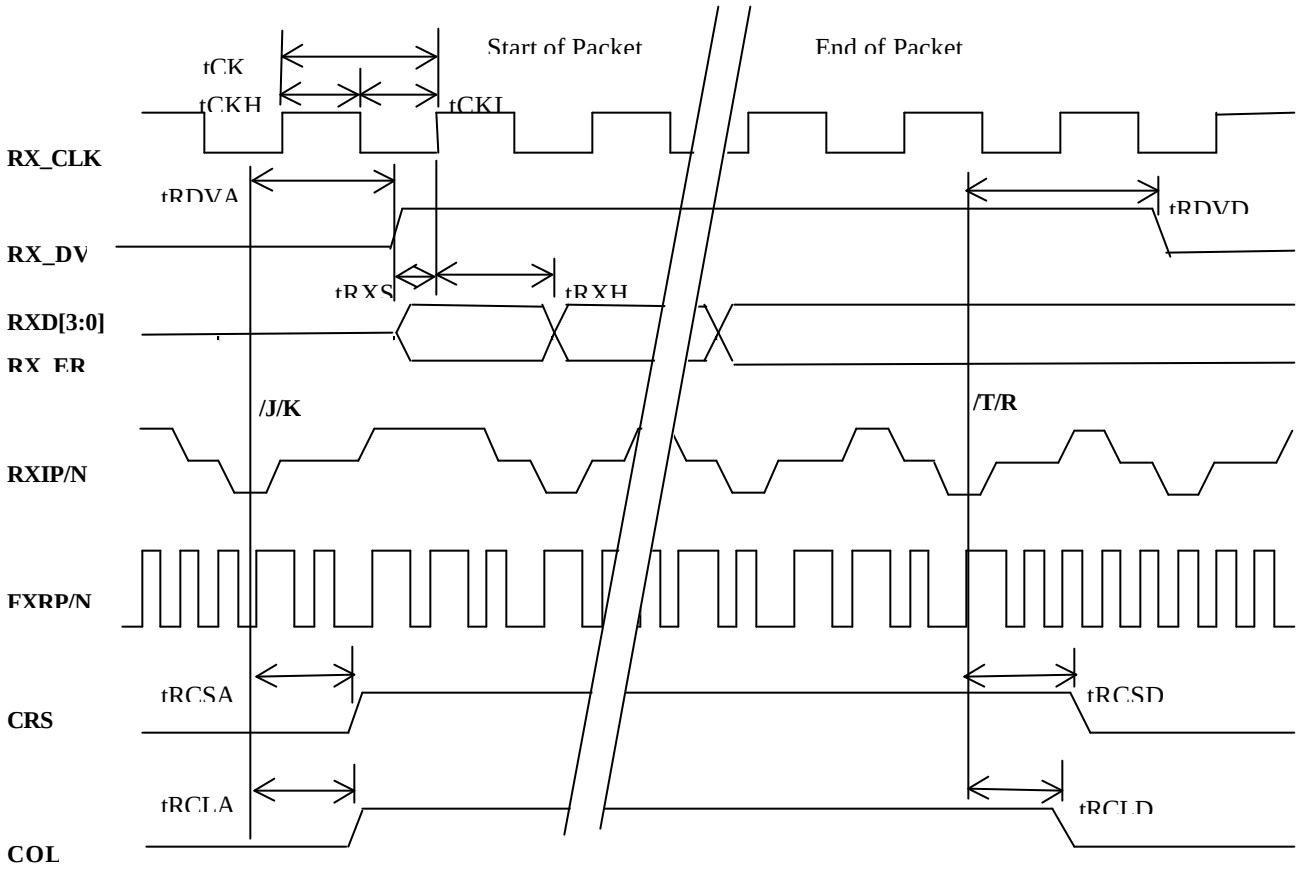
Parameter	SYM	Conditions	Min	Typ	Max	Units
TX_CLK period	tCK		39.998	40.000	40.002	ns
TX_CLK High period	tCKH		18.000	20.000	22.000	ns
TX_CLK Low period	tCKL		18.000	20.000	22.000	ns
TX_EN to /J/	tTJ		-	40	180	ns
TX_EN sampled to CRS	tCSA	RPTR is logic low	-	40	180	ns
TX_EN sampled to COL	tCLA	RPTR is logic low	-	40	180	ns
!TX_EN to /T/	tTT		-	40	180	ns
!TX_EN sampled to !CRS	tCSD	RPTR is logic low	-	40	180	ns
!TX_EN sampled to !COL	tCLD	RPTR is logic low	-	40	180	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N(FXTP/N)	-	40	180	ns
TXD[3:0], TX_EN, TX_ER Setup	tTXS	From rising edge of TX_CLK	10	-	-	ns
TXD[3:0], TX_EN, TX_ER Hold	tTXH	From rising edge of TX_CLK	0	-	-	ns
!TX_EN to TX_EN	tTX_TX		120	-	-	ns



100Base-TX/FX MII Transmit Timing

100Base-TX/FX MII Receive System Timing

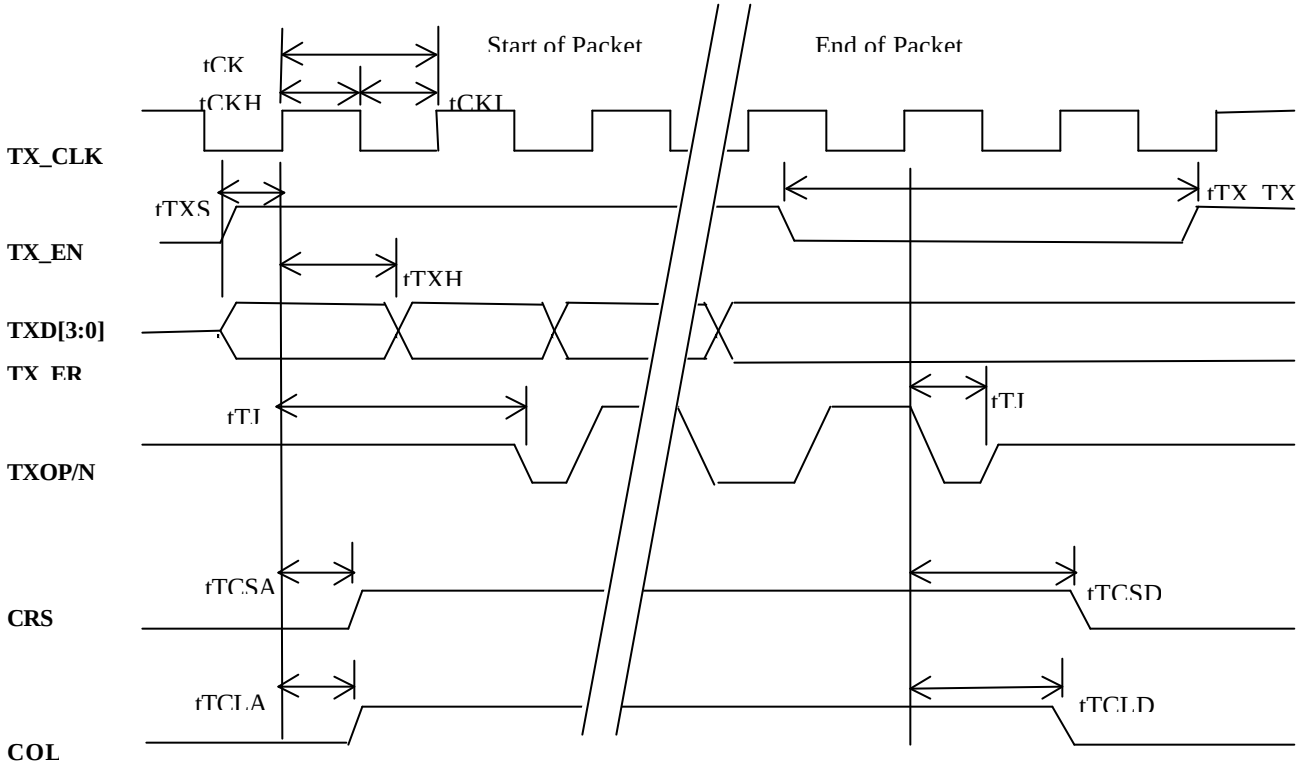
Parameter	SYM	Conditions	Min	Typ	Max	Units
RX_CLK period	tCK		39.998	40.000	40.002	ns
RX_CLK High period	tCKH		18.000	20.000	22.000	ns
RX_CLK Low period	tCKL		18.000	20.000	22.000	ns
/J/K to RX_DV assert	tRDVA		-	40	180	ns
/J/K to CRS assert	tRCSA		-	40	180	ns
/J/K to COL assert	tRCLA	RPTR is logic low	-	40	180	ns
/T/R to !RX_DV	tRDVD	RPTR is logic low	-	40	180	ns
/T/R to !CRS	tRCSD	RPTR is logic low	-	40	180	ns
/T/R to !COL	tRCLD	RPTR is logic low	-	40	180	ns
RX Propagation Delay	tRDVA	From RXIP/N(FXRP/N) to RXD[3:0]	-	40	180	ns
RXD[3:0], RX_DV, RX_ER Setup	tRXS	From rising edge of RX_CLK	10	-	-	ns
RXD[3:0], RX_DV, RX_ER Hold	tRXH	From rising edge of RX_CLK	10	-	-	ns



100Base-TX/FX MII Receive Timing

10Base-T MII Transmit System Timing

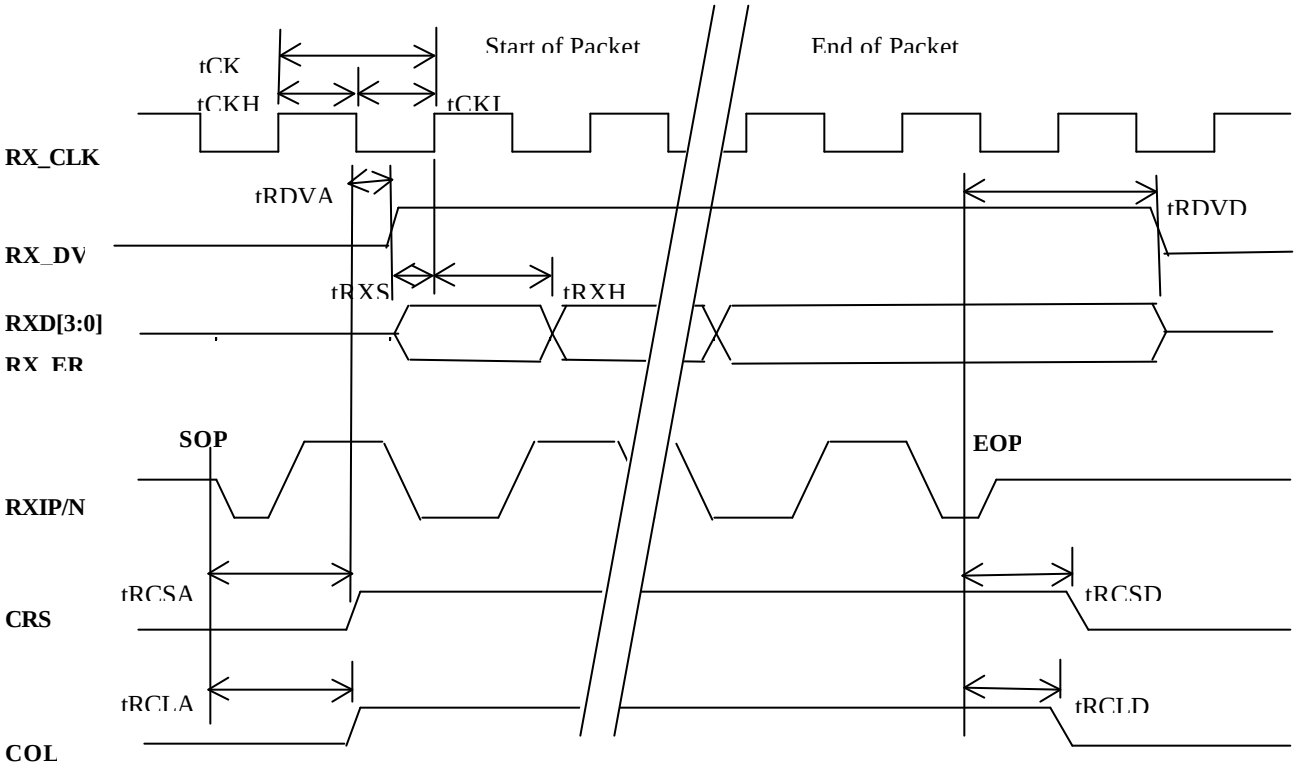
Parameter	SYM	Conditions	Min	Typ	Max	Units
TX_CLK period	tCK		399.98	400.00	400.02	ns
TX_CLK High period	tCKH		180.00	200.00	220.00	ns
TX_CLK Low period	tCKL		180.00	200.00	220.00	ns
TX_EN to SOP	tTJ		240	-	360	ns
TX_EN sampled to CRS	tTCSA	RPTR is logic low	-	-	130	ns
TX_EN sampled to COL	tTCLA	RPTR is logic low	-	-	300	ns
!TX_EN to EOP	tTJ		240	-	360	ns
!TX_EN sampled to !CRS	tTCSD	RPTR is logic low	-	-	130	ns
!TX_EN sampled to !COL	tTCLD	RPTR is logic low	-	-	300	ns
TX Propagation Delay	tTJ	From TXD[3:0] to TXOP/N	240	-	360	ns
TXD[3:0], TX_EN, TX_ER Setup	tTXS	From rising edge of TX_CLK	10	-	-	ns
TXD[3:0], TX_EN, TX_ER Hold	tTXH	From rising edge of TX_CLK	0	-	-	ns
!TX_EN to TX_EN	tTX_TX		300	-	-	ns



10Base-T MII Transmit Timing

10Base-T MII Receive System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
RX_CLK period	tCK		399.98	400.00	400.02	ns
RX_CLK High period	tCKH		180.00	200.00	220.00	ns
RX_CLK Low period	tCKL		180.00	200.00	220.00	ns
CRS to RX_DV	tRDVA		100	100	100	ns
SOP to CRS	tRCSA		80	-	150	ns
SOP to COL	tRCLA	RPTR is logic low	80	-	150	ns
EOP to !RX_DV	tRDVD	RPTR is logic low	120	-	140	ns
EOP to !CRS	tRCSD	RPTR is logic low	130	-	190	ns
EOP to !COL	tRCLD	RPTR is logic low	125	-	185	ns
RX Propagation Delay	tRDVA	From RXIP/N to RXD[3:0]	180	-	250	ns
RXD[3:0], RX_DV, RX_ER Setup	tRXS	From rising edge of RX_CLK	16	-	-	ns
RXD[3:0], RX_DV, RX_ER Hold	tRXH	From rising edge of RX_CLK	12	-	-	ns

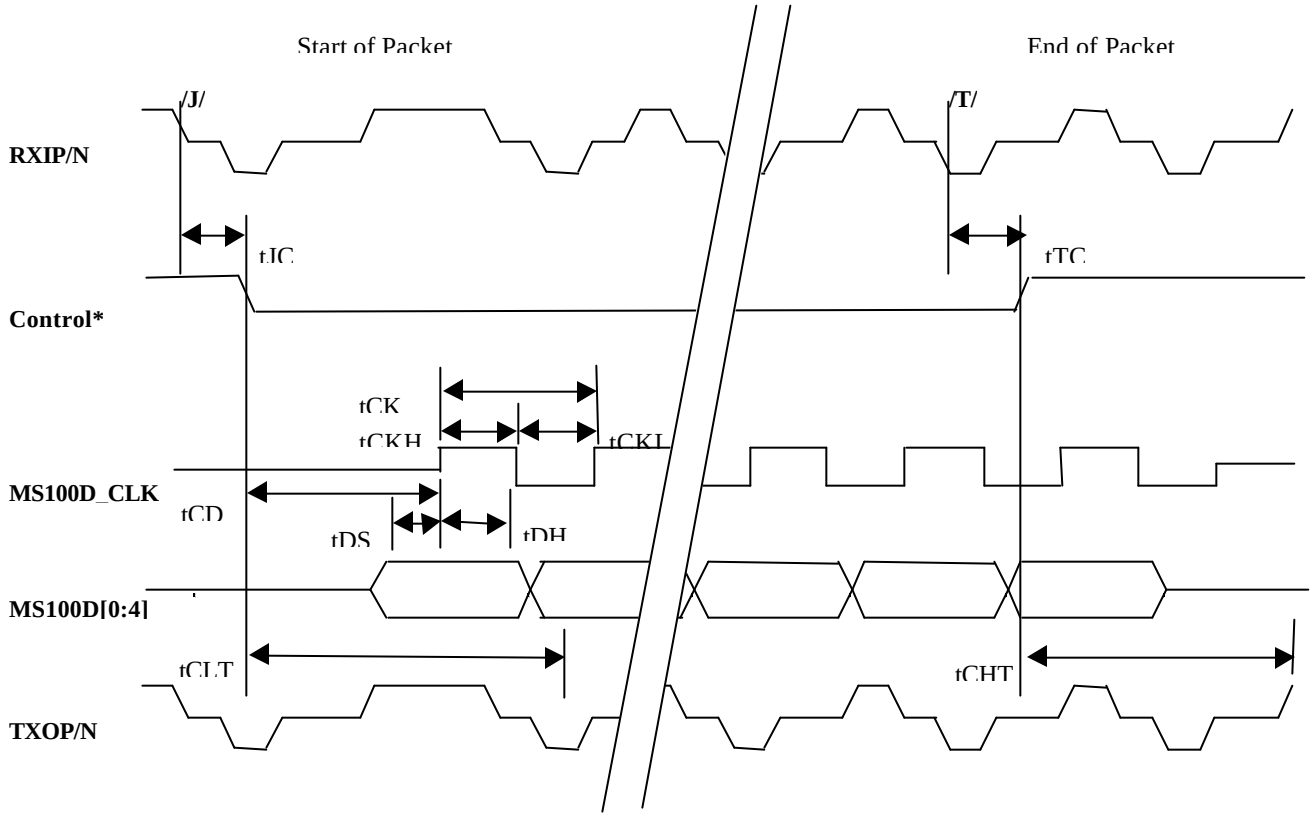


10Base-T MII Receive Timing

100Mbps Internal / Stacked Repeater Bus Receive / Transmit System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
MS100D_CLK period	tCK					ns
MS100D_CLK High period	tCKH					ns
MS100D_CLK Low period	tCKL					ns
/J/K (SOP) to Control	tJC					ns
/T/R (EOP) to !Control	tTC					ns
Control to MS100D_CLK	tCD					ns
MS100D[0:4] Setup	tDS					ns
MS100D[0:4] Hold	tDH					ns
Control to TXOP/N	tCLT					ns
!Control to !TXOP/N	tCHT					ns

Control is the combination of the following signals:
100CRSU_IN*, 100CRSD_IN*, 100CRSU_OUT*, 100CRSD_OUT*, 100COLBP*, 100CRSBP*, 100OE*, 100DIR*, M100COL_LOCAL*, M100ACT0*, M100ACT1_0*, M100ACT1_1*, M100ACT1_2*, M100COL_SYS*, M100CRS_SYS*, MS100D_EN*
Different signals are valid due to different scenarios, but the active time is the same.

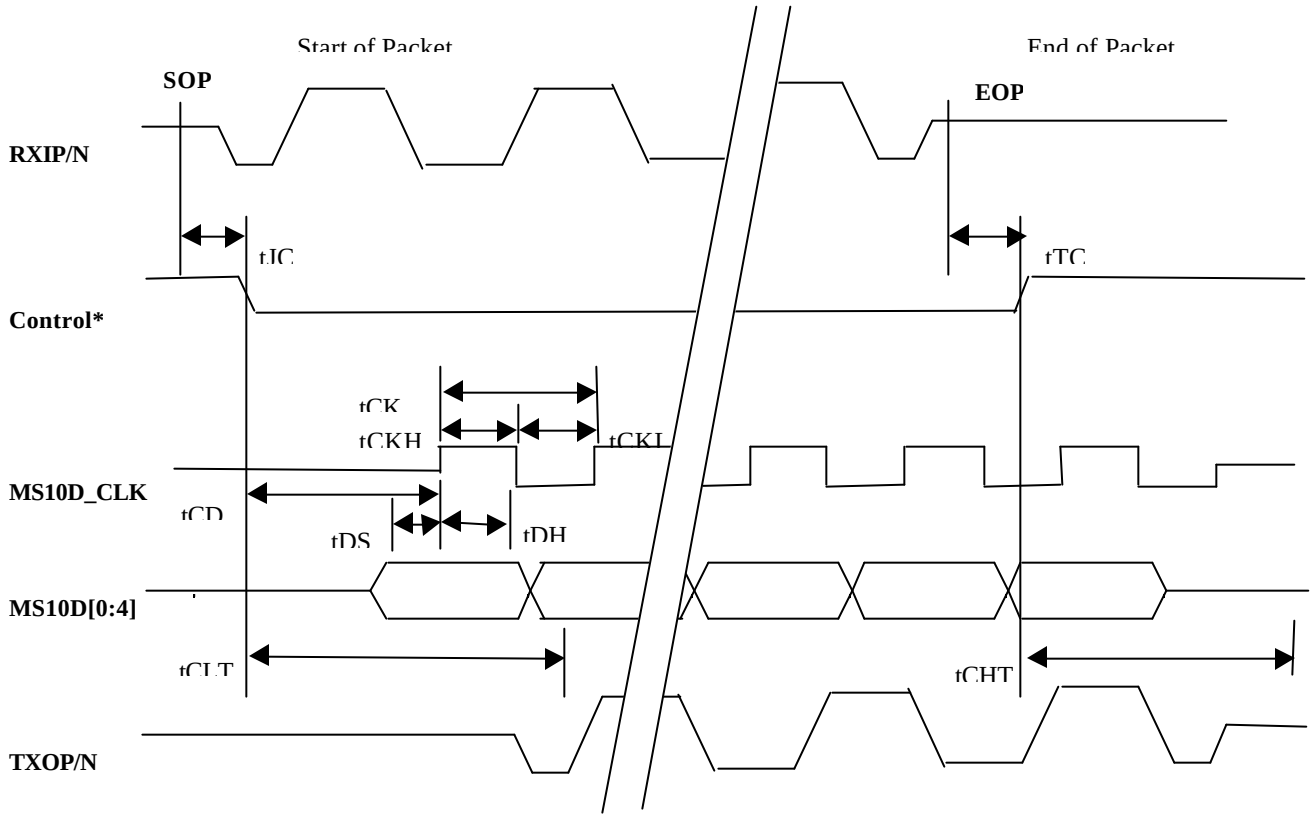


100Mbps I/SRB Receive / Transmit Timing

10Mbps Internal / Stacked Repeater Bus Receive / Transmit System Timing

Parameter	SYM	Conditions	Min	Typ	Max	Units
MS10D_CLK period	tCK					ns
MS10D_CLK High period	tCKH					ns
MS10D_CLK Low period	tCKL					ns
/J/K (SOP) to Control	tJC					ns
/T/R (EOP) to !Control	tTC					ns
Control to MS10D_CLK	tCD					ns
MS10D[0:4] Setup	tDS					ns
MS10D[0:4] Hold	tDH					ns
Control to TXOP/N	tCLT					ns
!Control to !TXOP/N	tCHT					ns

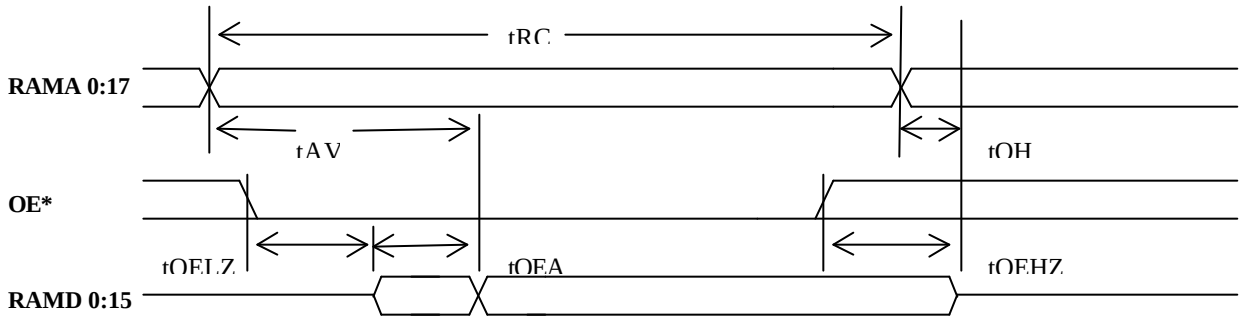
Control is the combination of the following signals:
10CRSU_IN*, 10CRSD_IN*, 10CRSU_OUT*, 10CRSD_OUT*, 10COLBP*, 10CRSBP*, 10OE*, 10DIR*, M10COL_LOCAL*, M10ACT0*, M10ACT1_0*, M10ACT1_1*, M10ACT1_2*, M10COL_SYS*, M10CRS_SYS*, MS10D_EN*
Different signals are valid due to different scenarios, but the active time is the same.



10Mbps I/SRB Receive / Transmit Timing

SRAM Read Cycle

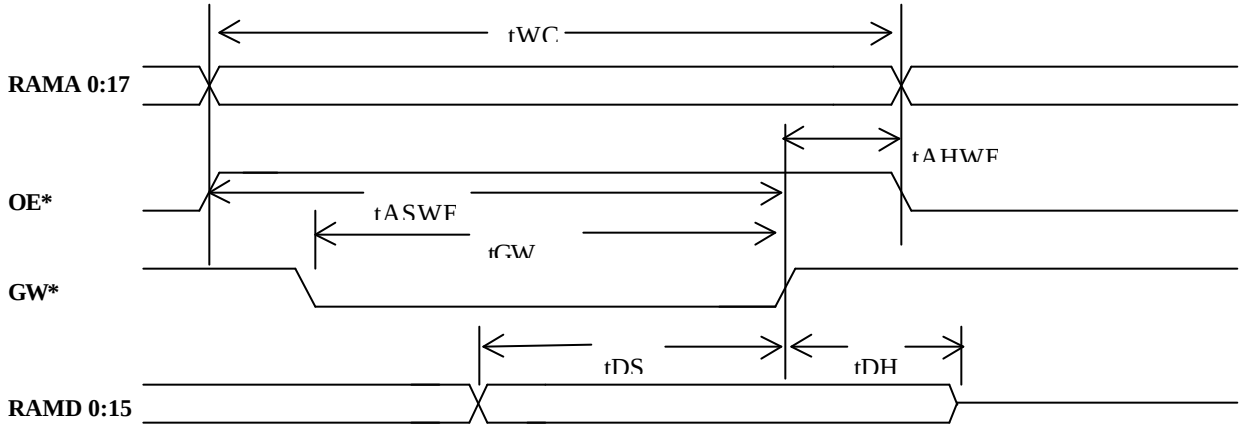
Parameter	SYM	Conditions	Min	Typ	Max	Units
Read Cycle	tRC		15		-	ns
Address - OE Valid	tAV		-		15	ns
Output Hold	tOH		3		-	ns
OE* Access	tOEA		-		6	ns
OE* to Low Z	tOELZ		0		-	ns
OE* to High Z	tOEHZ		0		6	ns



SRAM Read Cycle

SRAM Write Cycle

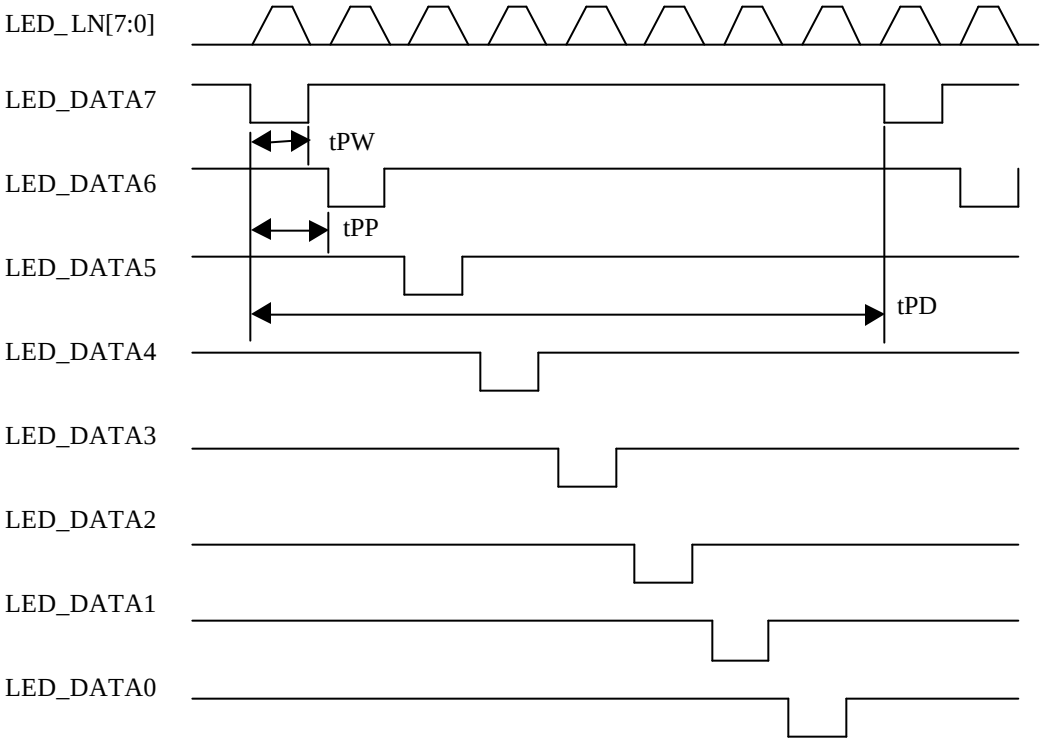
Parameter	SYM	Conditions	Min	Typ	Max	Units
Write Cycle	tWC		15		-	ns
GW* Pulse Width	tGW		10		-	ns
Address Setup to GW	tASWE		10		-	ns
Address Hold from GW	tAHWE		0		-	
Data Setup	tDS		7		-	ns
Data Hold	tDH		0		-	ns



SRAM Write Cycle

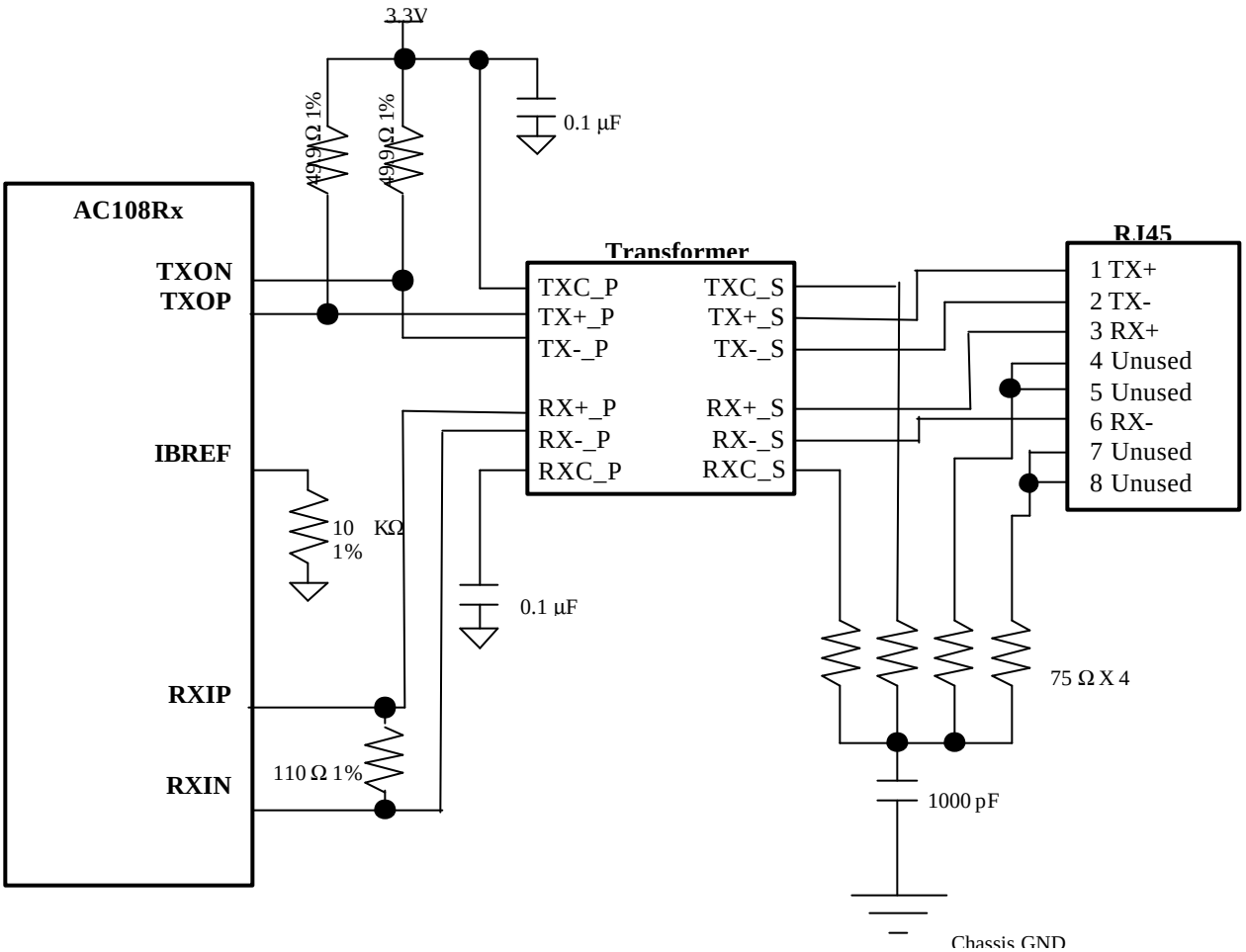
SRAM Write Cycle

Parameter	SYM	Conditions	Min	Typ	Max	Units
Pulse Width	tPW			2		ms
DATA[n] to DATA[n+1]	tPP			2		ms
DATA[n] to DATA[n]	tPD			16		ms



TX APPLICATION TERMINATION

Please contact Altima Communications Inc. for the latest component value recommendation



FX APPLICATION TERMINATION

Please contact Altima Communications Inc. for the latest component value recommendation

To enable the FX mode, FX_SEL7 pin must be pulled high by a 1 KW resistor.