GigaBit Logic

10G010
10G010M

T-68-21-51

Dual 2:1 Multiplexed Fanout Buffer
1.5 GHz Rate
10G PicoLogic™ Family

FEATURES

- Enhanced Version of the 10G011B
- 150 ps output rise and fall times
- 750 ps max. prop. delay
- ECL and 10G PicoLogic compatible I/O
- Temperature and voltage compensated design
- Small output skew: 5 ps typ. for each side, 50 ps max. between sides
- Either inverting or non-inverting operation
- 70 mA output drive current
- Wire-OR output capability
- On-chip VBBS threshold reference voltage supply
- Available in 40 pin C-leaded or leadless chip carrier or die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- High Speed Logic
- Bi-Phase or Single Phase Clock Driver
- Capacitive Load Driver
- Address & Data Buffers

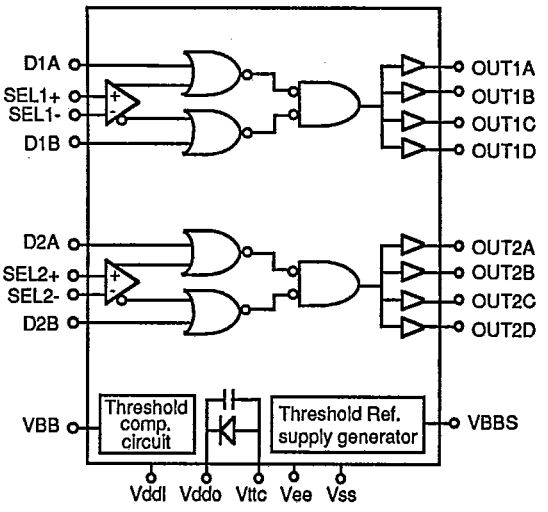
FUNCTIONAL DESCRIPTION

The 10G010 is an ECL and 10G PicoLogic™ I/O compatible ultra-fast dual 2:1 multiplexer with independent multiplexing controls and four output buffers. Due to its design, both true and complement clocks can be derived from a single ended clock input and buffered by one chip, minimizing clock skews. Four large source followers on each half can each drive two 50 ohm lines or the center of a 50 ohm bus with the option of wire-ORed outputs. Minimum 25°C operating frequency is 1.5 GHz. Typical propagation delay is 500ps for the data inputs and 575ps for the SEL+ and SEL- inputs.

For compatibility with other high speed logic families, the 10G010 features the PicoLogic™ family standard VBB input which allows the input logic threshold to be controlled by the driving logic family, thereby compensating for mismatches in threshold level due to temperature and power supply variation and providing high system noise immunity. An on-chip threshold voltage output (pin VBBS) is also provided for strapping to the VBB input when PicoLogic™ is used to drive the 10G010.

The 10G010 is a member of GigaBit's PicoLogic™ family of GaAs digital integrated circuits, and is fabricated using GigaBit's high volume GaAs MESFET process technology.

BLOCK DIAGRAM



10G010/10G010M ORDERING INFORMATION

PACKAGE TYPE	10G010 (0°C/85°C)		10G010M (-55°C/125°)	
	1.3 GHz	1.1 GHz	1.3 GHz	1.0 GHz
C-Leaded CC	10G010-2C	10G010-3C	10G010M-2C	10G010M-3C
Leadless CC	10G010-2L	10G010-3L	10G010M-2L	10G010M-3L
Die		10G010-3X		10G010M-3X

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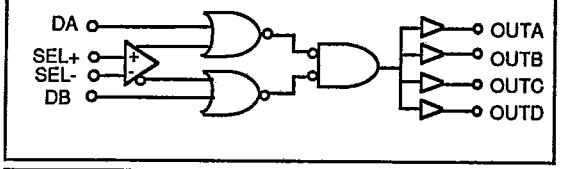
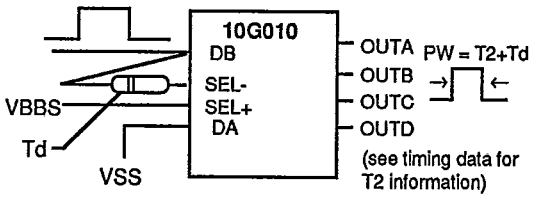
10G010 Operation

LOGIC DIAGRAM



TYPICAL APPLICATION - ONE SHOT



MULTIPLEXING TRUTH TABLE

SEL-	SEL+	DA	DB	OUTs
VBBS	1	X	1	1
VBBS	1	X	0	0
VBBS	0	1	X	1
VBBS	0	0	X	0
1	VBBS	1	X	1
1	VBBS	0	X	0
0	VBBS	X	1	1
0	VBBS	X	0	0

The operation of the 10G010 as a multiplexer is illustrated by referring to the logic diagram and truth table above. Each of the two multiplexers will select either the DA or DB input and direct it to the outputs in response to the individual SEL+ & SEL- controls. The SEL inputs may be driven either differentially or single ended with the unused input tied to VBBS or ECL derived VBB. It may also be wired as either an inverting or non-inverting Fanout Buffer with delays matched between the two halves within 50ps for either true or complement operation. Tying the B input high (VDDL) and the A input low (VSS) results in outputs which are inverted from the SEL-, and in phase with the SEL+ inputs, assuming that the unused SEL input is tied to the VBBS threshold reference voltage. This feature allows the generation of a two phase clock from a single ended clock input, buffering it for distribution with skews at all outputs typically less than 50 ps.

Above is shown an application which will shorten a posititve pulse similar to a one shot. This circuit can be configured to work on either the positive or negative edge of the input. Since the delay difference between A and SEL is minimal, the pulse width will be largely determined by the delay line.

Pin Descriptions

D1A, D2A	A data inputs
D1B, D2B	B data inputs
SEL1+,SEL2+	Positive select controls - high selects B (differential input)
SEL1-,SEL2-	Negative select controls - high selects A (differential input)
OUT1A - D	Multiplexer 1 outputs
OUT2A - D	Multiplexer 2 outputs
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G010 circuit, and is typically tied to VTT (nominally -2.0V)
VDCH	Output driver high level clamp voltage. When not used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G010's input threshold compensation circuit. Connect to the VBB supplied from ECL when driving from ECL. Otherwise connect to VBBS pin.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic.

NOTE: Neither VBB nor the signal inputs may be left unconnected.

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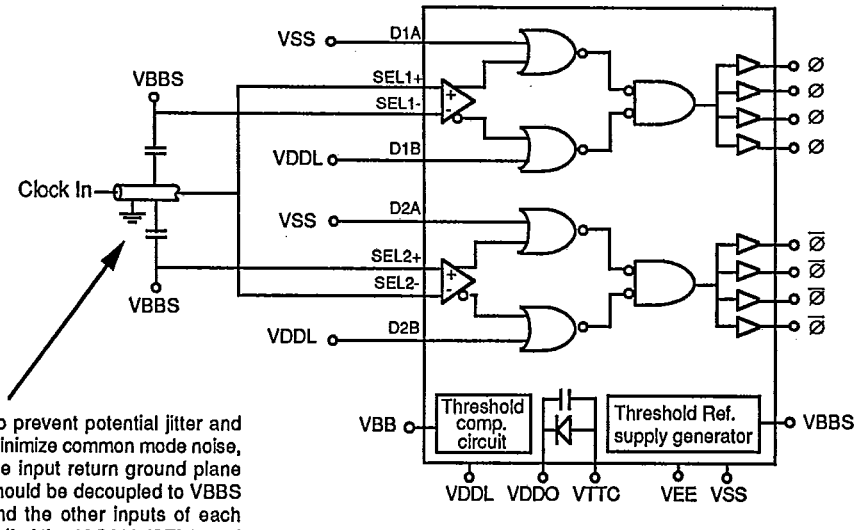
SPECIAL USAGE PRECAUTIONS

Typically, the 10G010 is used with multiple outputs loaded. Each source-follower output is capable of sourcing up to 70 mA of current depending on the load. Coupled with high output slew rates of 7V/ns, the result is very high instantaneous output switching currents. Following the relation for induced voltage transients, V = L dI/dt, considerable noise voltage can be induced in the power supply lines. Therefore, diligent attention to power supply decoupling and continuous power plane layout (refer to Application Note 2) is absolutely essential when using the 10G010. Given the limitations of real board designs, the 10G010 can exhibit phase jitter of the output signal, resulting in output duty cycle variation, under the following specific conditions: A input tied high (to VDD); SEL- set at threshold (-1.3V; ECL VBB or VBBS) and the signal applied to the SEL+ input in the approximate frequency range of 400 MHz to 600 MHz.

If the input signal is outside this frequency range, any tendency for the output to exhibit phase jitter is absent. No other operating mode is problematic. Given this operating sensitivity, GigaBit recommends that the A input be tied low (to VSS) in any application where the data multiplexing feature of the 10G010 is not used; i.e. for fan-out or inverting fan-out buffer applications or when the 10G010 is driven differentially. If the multiplexing capability of the 10G010 is to be used, the signal should be applied to the SEL- input with the SEL+ input tied to threshold to preclude the possibility of output phase jitter. These restrictions do not limit the range of logic functions the 10G010 can perform. They provide a preferred connection scheme where there is more than one way to wire a given function. Refer to Applications Brief 2 for additional discussion of these issues.

TWO PHASE CLOCK DISTRIBUTION



To prevent potential jitter and minimize common mode noise, the input return ground plane should be decoupled to VBBS and the other inputs of each half of the 10G010 (SEL1- and SEL2+ in the example above).

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DC CHARACTERISTICS

TC = -55°C to +125°C, VSS = -3.5 V to -3.3 V, VEE = -5.5 V to -5.1 V, VDDL = VDDO = 0 V, unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ISS	Power Supply Current		125	200	mA
IEE	Power Supply Current		50	80	mA
PD	Power Dissipation		690	1100	mW

NOTE: The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

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SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.5		1.5	1.8		1.3		GHz	
T1	SEL+, SEL- to output delay	400	700	400	575	700	425	750	ps	
T2	Data inputs to output delay	360	625	360	500	625	385	675	ps	
T3	Output rise and fall times		175		125	175		195	ps	2
T4	Skew between OUT pins		50		30	50		50	ps	

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SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.3		1.3	1.5		1.1		GHz	
T1	SEL+, SEL- to output delay	425	750	425	625	750	450	800	ps	
T2	Data inputs to output delay	385	675	385	550	675	410	725	ps	
T3	Output rise and fall times		200		150	200		225	ps	2
T4	Skew between OUT pins		50		30	50		50	ps	

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SYMBOL	PARAMETER	Tc = -55°C		Tc = +25°C			Tc=125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.4		1.5	1.8		1.3		GHz	
T1	SEL+, SEL- to output delay	400	700	400	575	700	450	800	ps	
T2	Data inputs to output delay	360	625	360	500	625	410	725	ps	
T3	Output rise and fall times		175		125	175		210	ps	2
T4	Skew between OUT pins		50		30	50		50	ps	

10G010M-3

SYMBOL	PARAMETER	Tc = -55°C		Tc = +25°C			Tc=125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
F	Operating frequency	1.2		1.3	1.5		1.0		GHz	
T1	SEL+, SEL- to output delay	425	750	425	625	750	460	825	ps	
T2	Data inputs to output delay	385	675	385	550	675	435	775	ps	
T3	Output rise and fall times		200		150	200		250	ps	2
T4	Skew between OUT pins		50		30	50		50	ps	

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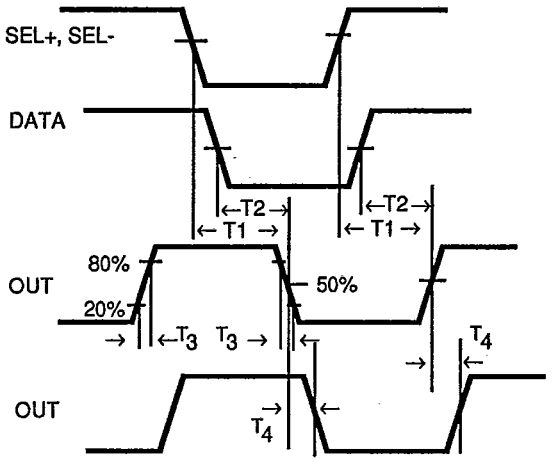
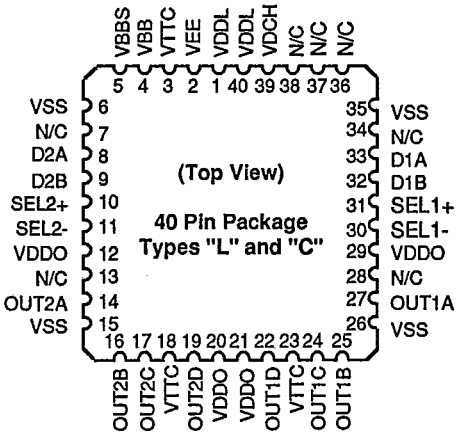
NOTES TO AC CHARACTERISTICS TABLE:

1. Test conditions (unless otherwise noted): VBB = -1.2V, VTT = -2.0V, VTTC = VTT, Rload = 50Ω to VTT, VDCH = VDDO, VIH = -0.7 V, VIL = -1.7 V, VOH ≥ -0.7 V, VOL ≤ -1.7 V. Input signal rise and fall times <150ps.
2. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

SWITCHING WAVEFORMS



40 PIN PACKAGE PINOUT



Pin 1 is marked for orientation. N/C = no connection.

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24 PIN HYBRID 18 PIN PACKAGE

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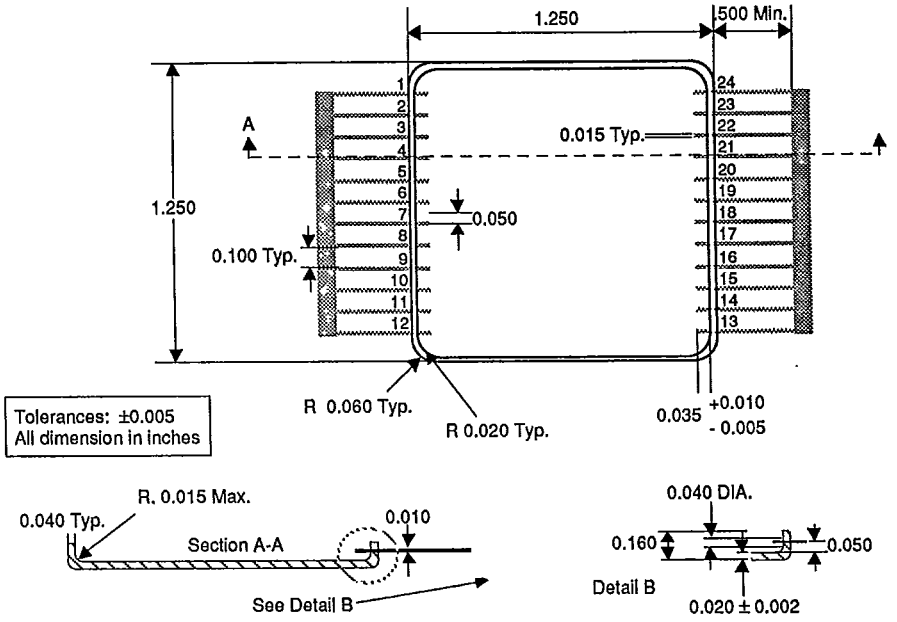
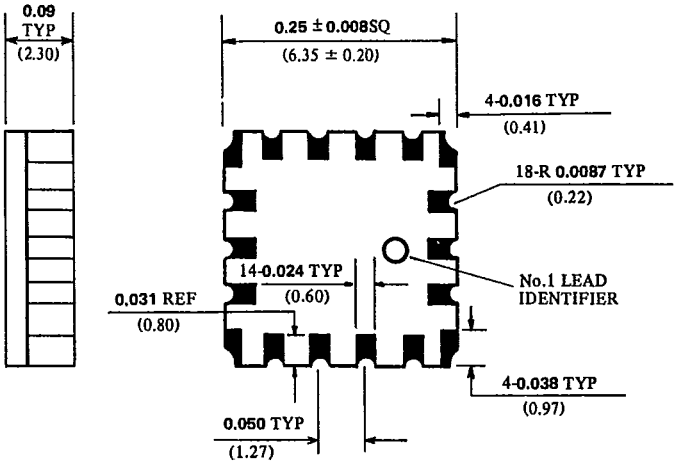
24 PIN HYBRID PACKAGE

Type H



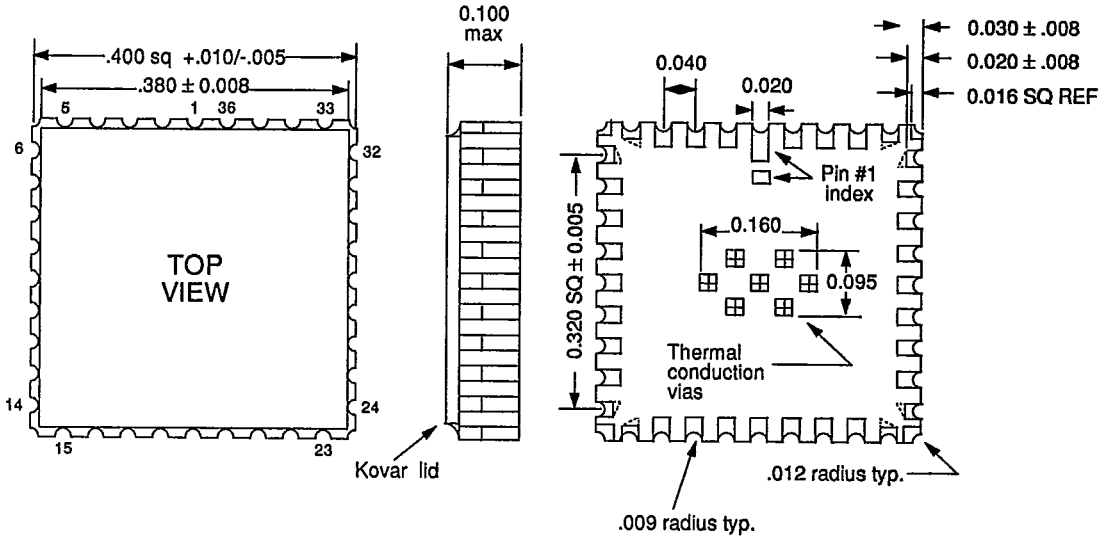
18 PIN LEADLESS CHIP CARRIER

TYPE L1



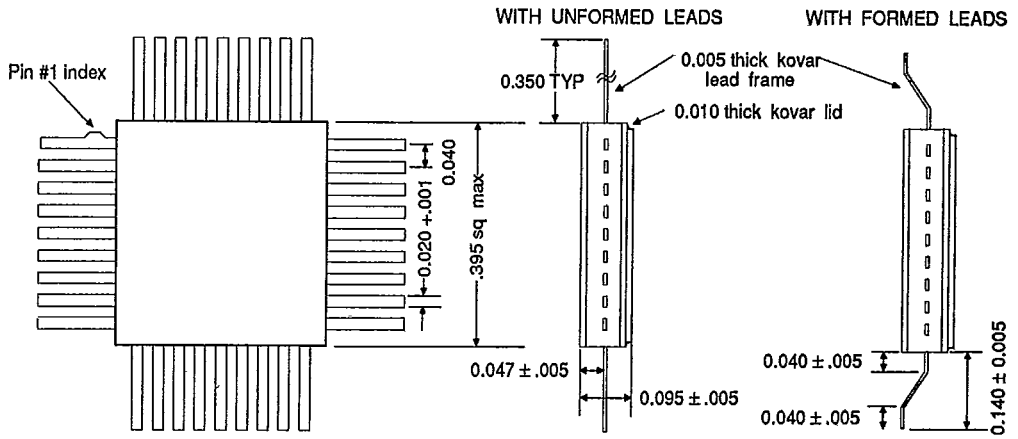
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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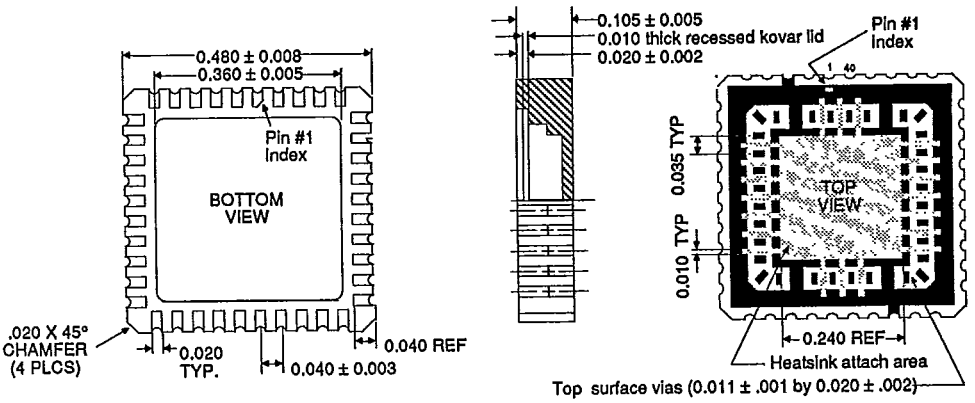
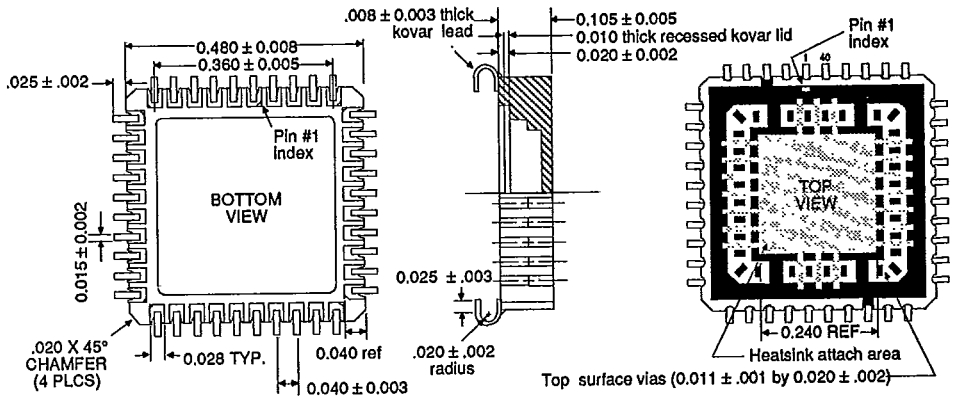
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

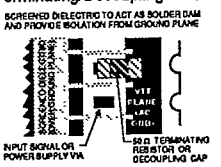


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail



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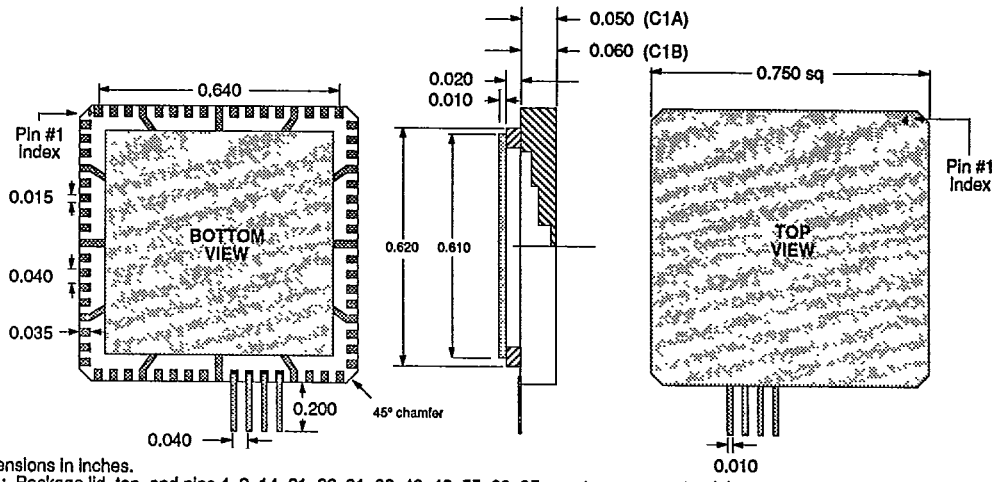
68 & 132 PIN PACKAGES

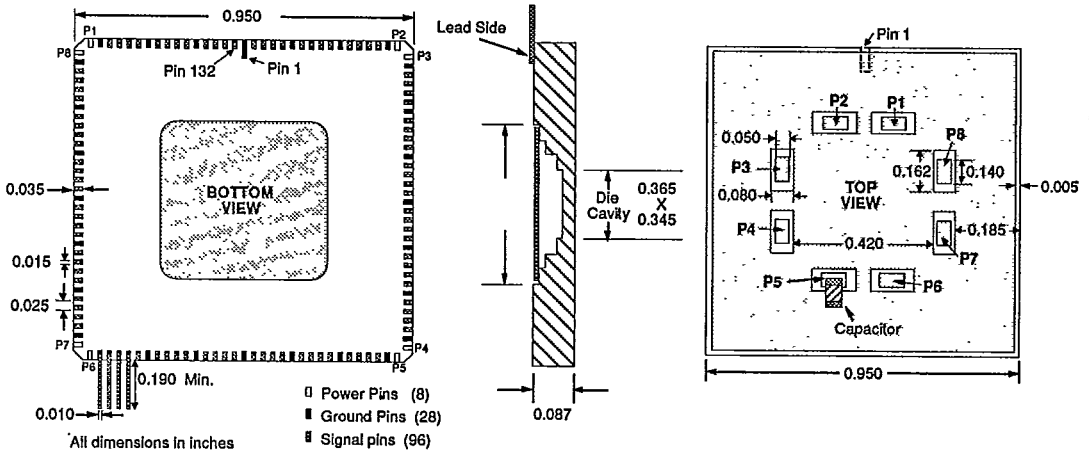
T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



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