5. ELECTRIC CHARACTERISTICS

Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Test condition	Ratings	Units
Power supply voltage	V_{DD}		-0.5 to +7.0	V
	AV_{REF}		-0.5 to V_{DD}+0.5	V
	AV_{SS}		-0.5 to +0.5	V
Input voltage	V_{I1}		-0.5 to V_{DD}+0.5	V
	V_{I2}	(Note)	-0.5 to AV_{REF}+0.5	V
Output voltage	V_O		-0.5 to V_{DD}+0.5	V
Output low current	I_{OL}	Per pin	15	mA
		Total, all outputs	100	mA
Output high current	I_{OH}	Per pin	-10	mA
		Total, all outputs	-50	mA
Operation temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

Note: Pins of P70/ANI0-P75/ANI5, P66/$\overline{WAIT}$/ANI6, and P67/$\overline{REFRQ}$/ANI7 are used as A/D converter input pins. However, the absolute maximum rating of V_{I1} must also be satisfied.

Caution: If even one parameter exceeds the absolute maximum rating, even instantaneously, the quality of the product may be damaged. The absolute maximum rating is a rated threshold value at which the product can be physically damaged. Be sure to use the product within the absolute maximum ratings.
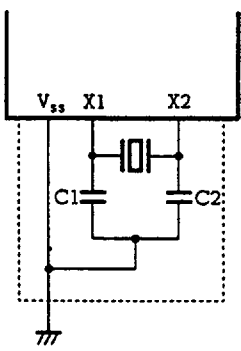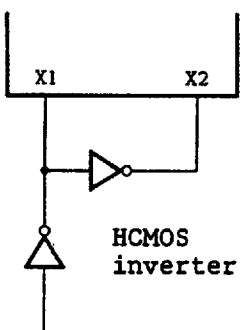
Operation conditions

Clock frequency	Operation temperature (T_{opt})	Power supply voltage(V_{DD})
4MHz$\leqq f_{XX} \leqq$12MHz	-10 to +70°C	+5V±10%

Capacitance (Ta=25°C, $V_{DD}=V_{SS}=0$ V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Input capacitance	C_I	f=1MHz Unmeasured pins returned to 0 V			20	pF
Output capacitance	C_0				20	pF
Input/output capacitance	C_{I0}				20	pF

Oscillator Characteristics (Ta=-40 to +85°C, V_{DD}=+5V±10%, V_{SS}=0V)

Resonator	Recommended constants	Item	MIN.	MAX.	Units
Ceramic oscillator or cristal resonator	V$_{ss}$ X1 X2 C1 C2	Oscillation frequency (fxx)	4	12	MHz
External clock	X1 X2 HCMOS inverter	X1 input frequency (fx)	4	12	MHz
		X1 input rise time/ fall time(t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Caution: To use the clock oscillator, wire the   portions   sur-
         rounded by [_ _ _] to avoid wiring capacitance affection,
         etc., as follows:

- Make wiring as extremely short as possible.
- Do not cross the oscillator and any other signal line over each other.
- Do not put the oscillator near any line where high current fluctuates.
- Be sure to place oscillator capacitor ground point in the same potential as the V_{SS} pin.
  Do not connect to any ground pattern where high current flows.
- Do not take out any signal from the oscillator.

Recommended oscillator constants

Ceramic oscillator

Manufacturer	Frequency [MHz]	Product name	Recommended constants	
			C1[pF]	C2[pF]
MURATA	12	CSA12.0MTZ	30	30
		CST12.0MTW	Contained a condenser	

DC characteristics (Ta=-10°C to +70°C, V_{DD}=+5V±10%, V_{SS}=0 V)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Units
Input low voltage	V_{IL}			0		0.8	V
Input high voltage	V_{IH1}	Pins except for listed in Note 1 or 2		2.2		V_{DD}	V
	V_{IH2}	Pins listed in Note 1		2.2		AV_{REF}	V
	V_{IH3}	Pins listed in Note 2		$0.8V_{DD}$		V_{DD}	V
Output low voltage	V_{OL1}	I_{OL}=2.0mA				0.45	V
	V_{OL2}	I_{OL}=8.0mA (Note 3)				1.0	V
Output high voltage	V_{OH1}	I_{OH}=-1.0mA		V_{DD}-1.0			V
	V_{OH2}	I_{OH}=-100uA		V_{DD}-0.5			V
	V_{OH3}	I_{OH}=-5.0mA (Note 4)		2.0			V
X1 input low current	I_{IL}	$0 \leq V_I \leq V_{IL}$				-100	uA
X1 input high current	I_{IH}	$V_{IH3} \leq V_I \leq V_{DD}$				100	uA
Input leakage current	I_{LI}	$0V \leq V_I \leq V_{DD}$				±10	uA
Output leakage current	I_{LO}	$0 V \leq V_O \leq V_{DD}$				±10	uA
AV_{REF} current	AI_{REF}	Operation mode fxx=12MHz			1.5	5.0	mA
V_{DD} supply current power	I_{DD1}	Operation mode fxx=12MHz			20	40	mA
	I_{DD2}	HALT mode fxx=12MHz			7	20	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR}=2.5V		2	20	uA
			V_{DDDR}=5V±10%		5	50	uA
Pull-up resistor	R_L	V_I=0 V		15	40	80	kΩ
EEPROM write voltage		4MHz≦fxx≦12MHz		4.5		5.5	V

Notes 1: Pins of P70/ANI0-P75/ANI5, P66/$\overline{WAIT}$/ANI6, and P67/$\overline{REFRQ}$/ANI7 except are used as A/D converter input pins.

2: X1, X2, $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, and $\overline{EA}$ pins.

3: P40/AD0-P47/AD7 and P50/A8-P57/A15 pins.

4: P00-P07 pins.

AC characteristics (Ta=-10°C to +70°C, V_{DD}=+5V±10%, V_{SS}=0 V)

Read/write operation (1/2)

Parameter	Symbol	Test condition	MIN.	MAX.	Units
X1 input clock cycle time	t_{CYX}		82	250	ns
Address setup time to ASTB↓	t_{SAST} *		52		ns
Address hold time from ASTB↓ (Note)	t_{HSTA}		25		ns
Address hold time from $\overline{RD}$↑	t_{HRA}		30		ns
Address hold time from $\overline{WR}$↑	t_{HWA}		30		ns
Address → $\overline{RD}$↓ delay time	t_{DAR} *		129		ns
Address float time $\overline{RD}$↓	t_{FAR} *		11		ns
Address → data input time	t_{DAID} *	Wait count=0		228	ns
ASTB↓ → data input time	t_{DSTID} *	Wait count=0		181	ns
$\overline{RD}$↓ → data input time	t_{DRID} *	Wait count=0		100	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR} *		52		ns
Data hold time from $\overline{RD}$↑	t_{HRID}		0		ns
$\overline{RD}$↑ → address active time	t_{DRA} *		124		ns
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST} *		124		ns
$\overline{RD}$ low level width	t_{WRL} *	Wait count=0	124		ns
ASTB high level width	t_{WSTH} *		52		ns
Address → $\overline{WR}$↓ delay time	t_{DAW} *		129		ns
ASTB↓ → data output time	t_{DSTOD} *			142	ns
$\overline{WR}$↓ → data output time	t_{DWOD}			60	ns
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW1} *	When refresh is disabled.	52		ns
	t_{DSTW2} *	When refresh is enabled.	129		ns
Data setup time to $\overline{WR}$↑	t_{SODWR} *	Wait count=0	146		ns
Data setup time to $\overline{WR}$↓	t_{SODWF} *	When refresh is enabled.	22		ns
Data hold time from $\overline{WR}$↑ (Note)	t_{HWOD}		20		ns
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST} *		42		ns
$\overline{WR}$ low level width	t_{WWL1} *	Wait count=0 when refresh is disabled.	196		ns
	t_{WWL2} *	Wait count=0 when refresh is enabled.	114		ns
Address → $\overline{WAIT}$↓ input time	t_{DAWT} *			146	ns
ASTB↓ → $\overline{WAIT}$↓ input time	t_{DSTWT} *			84	ns

Note: The hold time contains the V_{OH}, V_{OL} holding time under the load conditions of C_L=100 pF and R_L=2kΩ.

Remarks 1: The numeric values listed in the table are values when f_{XX}=12 MHz and C_L=100 pF.
2: For the parameters with an asterisk under Symbol, also see T_{CYX}-dependent Bus Timing Definition.

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Read/write operation (2/2)

Parameter		Symbol	Test condition	MIN.	MAX.	Units
ASTB↓ — $\overline{WAIT}$ retention time		t_{HSTWT} *	External wait count=1	174		ns
ASTB↓ — $\overline{WAIT}$↑ delay time		t_{DSTWTH}*	External wait count=1		273	ns
$\overline{RD}$↓ — $\overline{WAIT}$↓ input time		t_{DRWTL} *			22	ns
$\overline{RD}$↓ — $\overline{WAIT}$ retention time		t_{HRWT} *	External wait count=1	87		ns
$\overline{RD}$↓ — $\overline{WAIT}$↑ delay time		t_{DRWTH} *	External wait count=1		186	ns
$\overline{WAIT}$↑ — data input time		t_{DWTID} *			62	ns
$\overline{WAIT}$↑ — $\overline{WR}$↑ delay time		t_{DWTW} *		154		ns
$\overline{WAIT}$↑ — $\overline{RD}$↑ delay time		t_{DWTR} *		72		ns
$\overline{WR}$↓ — $\overline{WAIT}$↓ input time (when refresh is disabled)		t_{DWWTL} *			22	ns
$\overline{WR}$↓ — $\overline{WAIT}$ retention time	When refresh is disabled	t_{HWWT1} *	External wait count=1	87		ns
	When refresh is enabled	t_{HWWT2} *	External wait count=1	5		ns
$\overline{WR}$↓ — $\overline{WAIT}$↑ delay time	When refresh is disabled	t_{DWWTH1}*	External wait count=1		186	ns
	When refresh is enabled	t_{DWWTH2}*	External wait count=1		104	ns
$\overline{RD}$↑ — $\overline{REFRQ}$↓ delay time		t_{DRRFQ} *		154		ns
$\overline{WR}$↑ — $\overline{REFRQ}$↓ delay time		t_{DWRFQ} *		72		ns
$\overline{REFRQ}$ low level width		t_{WRFQL} *		120		ns
$\overline{REFRQ}$↑ — ASTB↓ delay time		t_{DRFQST}*		280		ns

Remarks 1: The numeric values in the table apply when f_{XX}=12 MHz and C_L=100 pF.

2: For the parameters with an asterisk under the Symbol, also see t_{CYX}-dependent Bus Timing Definition.

Serial operation

Parameter	Symbol	Test condition		MIN.	MAX.	Units
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		us
		Output	Internal divide by 16	1.3		us
			Internal divide by 64	5.3		us
Serial clock low level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divide by 16	556		ns
			Internal divide by 64	2.5		us
Serial clock high level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divide by 16	556		ns
			Internal divide by 64	2.5		us
SI, SBO setup time to $\overline{SCK}\uparrow$	t_{SSSK}			150		ns
SI, SBO hold time from $\overline{SCK}\uparrow$	t_{HSSK}			400		ns
SO/SBO output delay time from $\overline{SCK}\downarrow$	t_{DSBSK1}	CMOS push-pull output (3-line serial I/O mode)		0	300	ns
	t_{DSBSK2}	Open drain output (SBI mode), $R_L = 1k\Omega$		0	800	ns
SBO high hold time from $\overline{SCK}\uparrow$	t_{HSBSK}	SBI mode		4		t_{CYX}
SBO low setup time to $\overline{SCK}\downarrow$	t_{SSBSK}			4		t_{CYX}
SBO low level width	t_{WSBL}			4		t_{CYX}
SBO high level width	t_{WSBH}			4		t_{CYX}

Remarks: The numeric values listed in the table are values when $f_{XX} = 12$ MHz and $C_L = 100$ pF.

Other operations

Parameter	Symbol	Test condition	MIN.	MAX.	Units
NMI low level width	t_{WNIL}		10		us
NMI high level width	t_{WNIH}		10		us
INTP0-INTP5 low level width	t_{WITL}		24		t_{CYX}
INTP0-INTP5 high level width	t_{WITH}		24		t_{CYX}
$\overline{RESET}$ low level width	t_{WRSL}		10		us
$\overline{RESET}$ high level width	t_{WRSH}		10		us

External clock timing

Parameter	Symbol	Test condition	MIN.	MAX.	Units
X1 input low level width	t_{WXL}		30	130	ns
X1 input high level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D converter characteristics (Ta=-10°C to +70°C, V_{DD}=+5V±10%, V_{SS}=AV_{SS}=0 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Resolution			8			bit
(Note 1) Total error		$4.0V \leq AV_{REF} \leq V_{DD}$			0.4	%
		$3.6V \leq AV_{REF} \leq V_{DD}$			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	$82ns \leq t_{CYX} < 125ns$ When ADM FR bit is 0	360			t_{CYX}
		$125ns \leq t_{CYX} < 250ns$ When ADM FR bit is 1	240			t_{CYX}
Sampling time	t_{SAMP}	$82ns \leq t_{CYX} < 125ns$ When ADM FR bit is 0	72			t_{CYX}
		$125ns \leq t_{CYX} < 250ns$ When ADM FR bit is 1	48			t_{CYX}
Analog input voltage	V_{IAN}		-0.3		$AV_{REF}+0.3$	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF}		3.6		V_{DD}	V
AV_{REF} current	AI_{REF}	fxx=12MHz		1.5	5.0	mA
		(Note 2)		0.2	1.5	mA

Notes 1: It does not contain a quantization error. It is repre-
sented by a ratio to the full scale value.
2: When the ADM register CS bit is 0.

t_{CYX}-dependent bus timing definition (1/2)

Parameter	Symbol	Test condition	MIN./MAX.	12MHz	Units
X1 input clock cycle time	t_{CYX}		MIN	82	ns
Address setup time to ASTB↓	t_{SAST}	$t_{CYX}-30$	MIN.	52	ns
Address hold time from $\overline{RD}$↑	t_{HRA}		MIN.	30	ns
Address hold time from $\overline{WR}$↑	t_{HWA}		MIN.	30	ns
Address → $\overline{RD}$↓ delay time	t_{DAR}	$2t_{CYX}-35$	MIN.	129	ns
Address float time to $\overline{RD}$↓	t_{FAR}	$t_{CYX}/2-30$	MIN.	11	ns
Address → data input time	t_{DAID}	$(4+2n)t_{CYX}-100$	MAX.	228[Note]	ns
ASTB↓ → data input time	t_{DSTID}	$(3+2n)t_{CYX}-65$	MAX.	181[Note]	ns
$\overline{RD}$↓ → data input time	t_{DRID}	$(2+2n)t_{CYX}-64$	MAX.	100[Note]	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}	$t_{CYX}-30$	MIN.	52	ns
$\overline{RD}$↑ → address active time	t_{DRA}	$2t_{CYX}-40$	MIN.	124	ns
$\overline{RD}$↑ → ASTB↓ delay time	t_{DRST}	$2t_{CYX}-40$	MIN.	124	ns
$\overline{RD}$ low level width	t_{WRL}	$(2+2n)t_{CYX}-40$	MIN.	124[Note]	ns
ASTB high level width	t_{WSTH}	$t_{CYX}-30$	MIN.	52	ns
Address → $\overline{WR}$↓ delay time	t_{DAW}	$2t_{CYX}-35$	MIN.	129	ns
ASTB↓ → data output time	t_{DSTOD}	$t_{CYX}+60$	MAX.	142	ns
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW1}	$t_{CYX}-30$ (When refresh is disabled.)	MIN.	52	ns
	t_{DSTW2}	$2t_{CYX}-35$ (When refresh is enabled.)	MIN.	129	ns
Data setup time to $\overline{WR}$↑	t_{SODWR}	$(3+2n)t_{CYX}-100$	MIN.	146[Note]	ns
Data setup time to $\overline{WR}$↑	t_{SODWF}	$t_{CYX}-60$ (When refresh is enabled.)	MIN.	22	ns
$\overline{WR}$↑ → ASTB↓ delay time	t_{DWST}	$t_{CYX}-40$	MIN.	42	ns
$\overline{WR}$ low level width	t_{WWL1}	$(3+2n)t_{CYX}-50$ (When refresh is disabled.)	MIN.	196[Note]	ns
	t_{WWL2}	$(2+2n)t_{CYX}-50$ (When refresh is enabled.)	MIN.	114[Note]	ns
Address → $\overline{WAIT}$↓ input time	t_{DAWT}	$3t_{CYX}-100$	MAX.	146	ns
ASTB↓ → $\overline{WAIT}$↓ input time	t_{DSTWT}	$2t_{CYX}-80$	MAX.	84	ns

Remarks: n denotes the number of wait states.

Note: When n=0.

t_{CYX}-dependent bus timing definition (2/2)

Parameter		Symbol	Test condition	MIN./MAX.	12MHz	Units
ASTB ↓ → $\overline{WAIT}$ retention time		t_{HSTWT}	$2Xt_{CYX}+10$	MIN.	174[Note]	ns
ASTB ↓ → $\overline{WAIT}$ ↑ delay time		t_{DSTWTH}	$2(1+X)t_{CYX}-55$	MAX.	273[Note]	ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time		t_{DRWTL}	$t_{CYX}-60$	MAX.	22	ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ retention time		t_{HRWT}	$(2X-1)t_{CYX}+5$	MIN.	87[Note]	ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↑ delay time		t_{DRWTH}	$(2X+1)t_{CYX}-60$	MAX.	186[Note]	ns
$\overline{WAIT}$ ↑ → data input time		t_{DWTID}	$t_{CYX}-20$	MAX.	62	ns
$\overline{WAIT}$ ↑ → $\overline{WR}$ ↓ delay time		t_{DWTW}	$2t_{CYX}-10$	NIM.	154	ns
$\overline{WAIT}$ ↑ → $\overline{RD}$ ↓ delay time		t_{DWTR}	$t_{CYX}-10$	MIN.	72	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↓ input time (when refresh is disabled)		t_{DWWTL}	$t_{CYX}-60$	MAX.	22	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ retention time	When refresh is disabled	t_{HWWT1}	$(2X-1)t_{CYX}+5$	MIN.	87[Note]	ns
	When refresh is enabled	t_{HWWT2}	$2(X-1)t_{CYX}+5$	MIN.	5[Note]	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↑ delay time	When refresh is disabled	t_{DWWTH1}	$(2X+1)t_{CYX}-60$	MAX.	186[Note]	ns
	When refresh is enabled	t_{DWWTH2}	$2Xt_{CYX}-60$	MAX.	104[Note]	ns
$\overline{RD}$ ↓ → $\overline{REFRQ}$ ↓ delay time		t_{DRRFQ}	$2t_{CYX}-10$	MIN.	154	ns
$\overline{WR}$ ↓ → $\overline{REFRQ}$ ↓ delay time		t_{DWRFQ}	$t_{CYX}-10$	MIN.	72	ns
$\overline{REFRQ}$ low level width		t_{WRFQL}	$2t_{CYX}-44$	MIN.	120	ns
$\overline{REFRQ}$ ↓ → ASTB ↓ delay time		t_{DRFQST}	$4t_{CYX}-48$	MIN.	280	ns

Remarks 1: X: Number of external wait cycles (1, 2, ...)

2: $t_{CYX} \fallingdotseq 82ns$ ($f_{XX}=12MHz$)
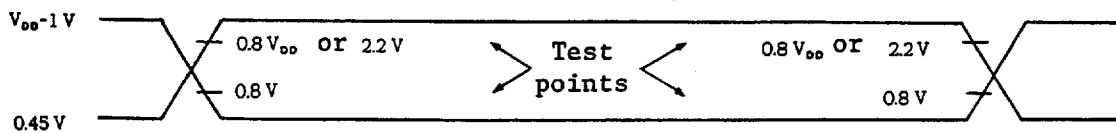
3: n denotes the number of wait cycles.

Note: When X=1.

Data retention characteristics (Ta = -10°C to 70°C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Units
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR}=2.5V		2	20	uA
		V_{DDDR}=5V±10%		5	50	uA
V_{DD} rise time	t_{RVD}		200			us
V_{DD} fall time	t_{FVD}		200			us
V_{DD} retention time from STOP mode setting	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stable wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic oscillator	5			ms
Input low voltage	V_{IL}	Specific pins (Note)	0		$0.1\ V_{DDDR}$	V
Input high voltage	V_{IH}		$0.9\ V_{DDDR}$		V_{DDDR}	V

Note: $\overline{RESET}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{SCK}$, P33/SO/SB0, and $\overline{EA}$ pins

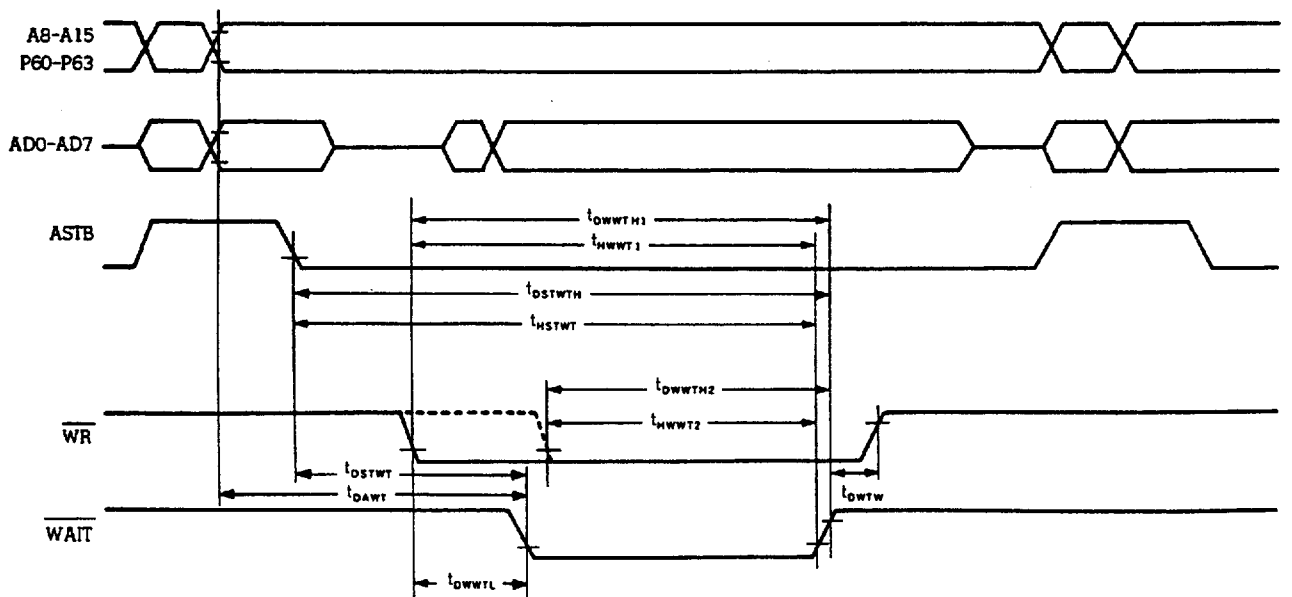## AC Timing Test Points

Timing Waveforms

Read operation

t_{CYX}

X1

A8-A15

t_{DAID}

t_{DAR}

t_{HRA}

AD0-AD7

t_{HRID}

t_{SAST} t_{HSTA} t_{FAR}

t_{DSTID}

t_{DRA}

ASTB

t_{WSTH} t_{DSTR} t_{DRID} t_{DRST}

t_{WRL}

$\overline{RD}$

Write operation

t_{CYX}

X1

A8-A15

t_{HWA}

t_{DAW}

AD0-AD7

t_{SAST} t_{HSTA}

t_{HWOD}

t_{DSTOD} t_{DWOD} t_{SODWF}

t_{SODWR}

ASTB

t_{WSTH}

t_{WWL1} t_{DWST}

t_{WWL2}

$\overline{WR}$

t_{DSTW1}

t_{DSTW2}
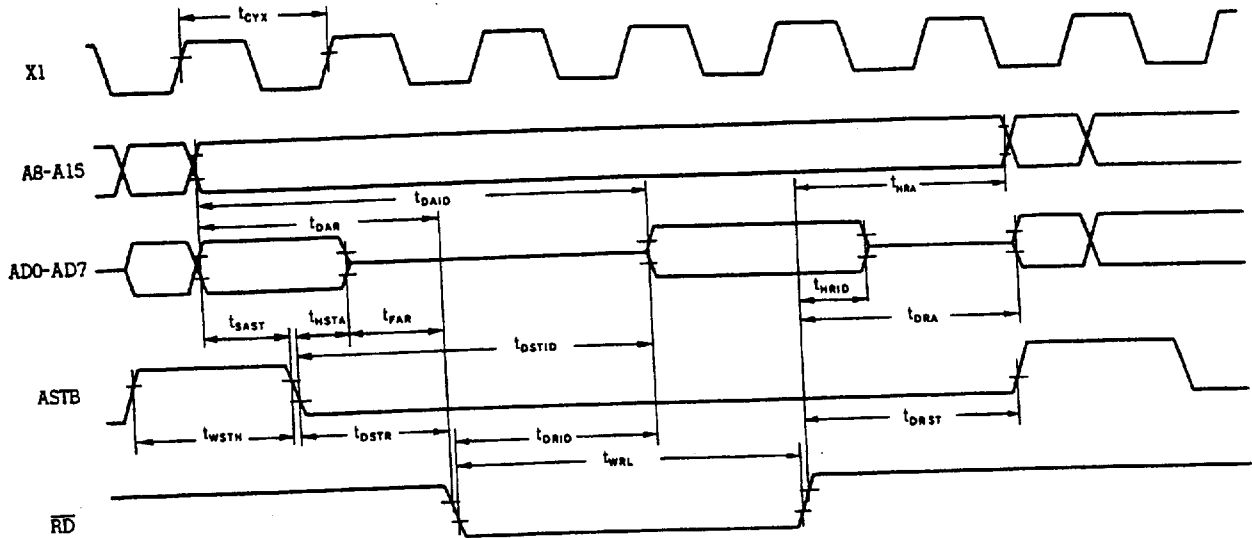
External WAIT Signal Input Timing

Read operation
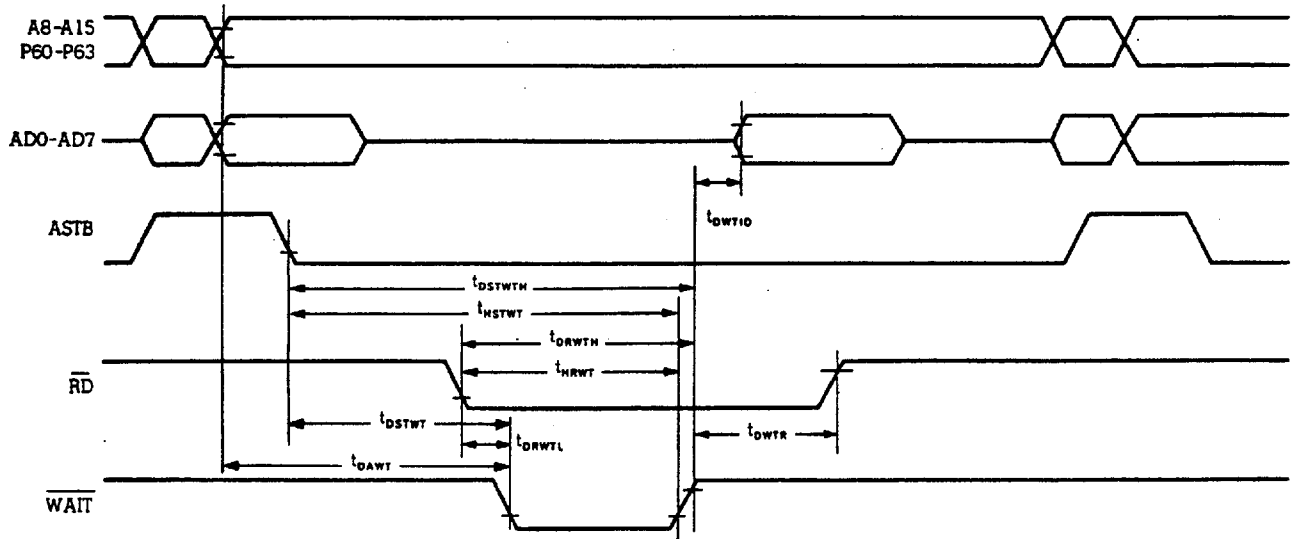
Write operation

Refresh Timing Waveforms

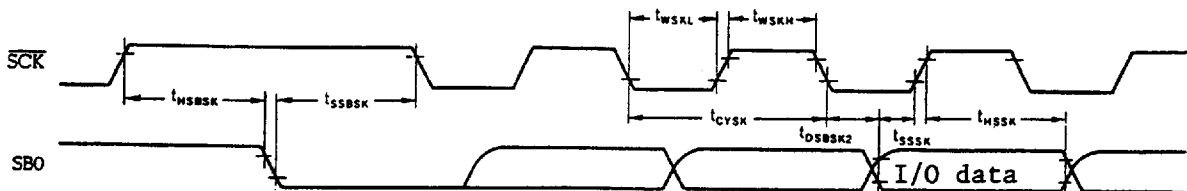### Refresh after read
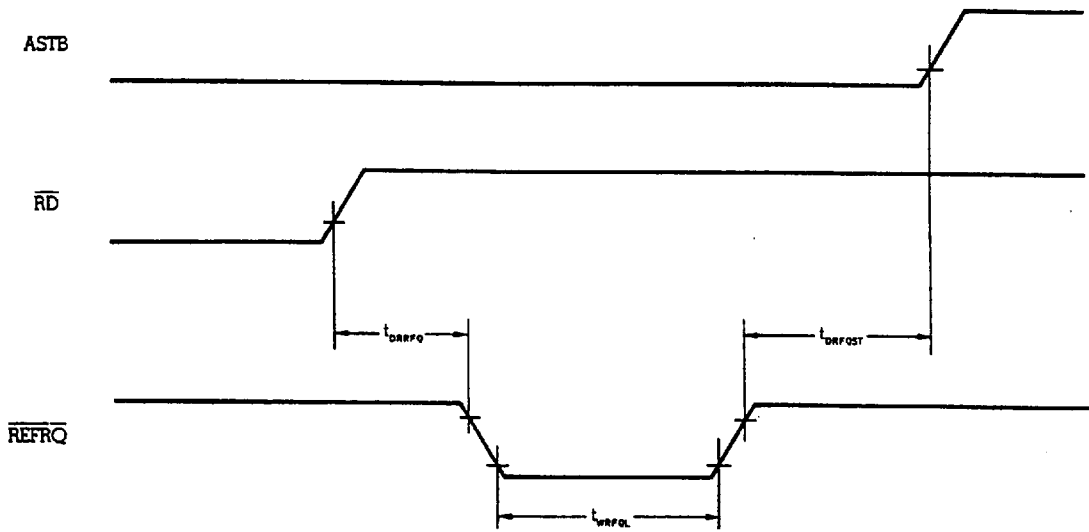
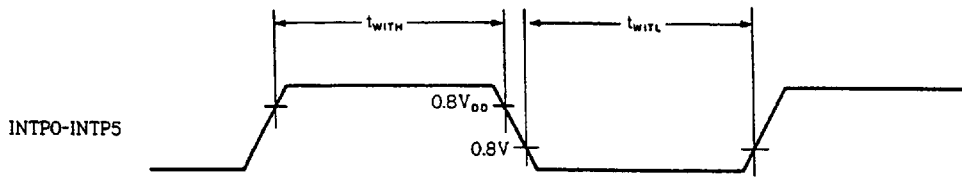### Refresh after write
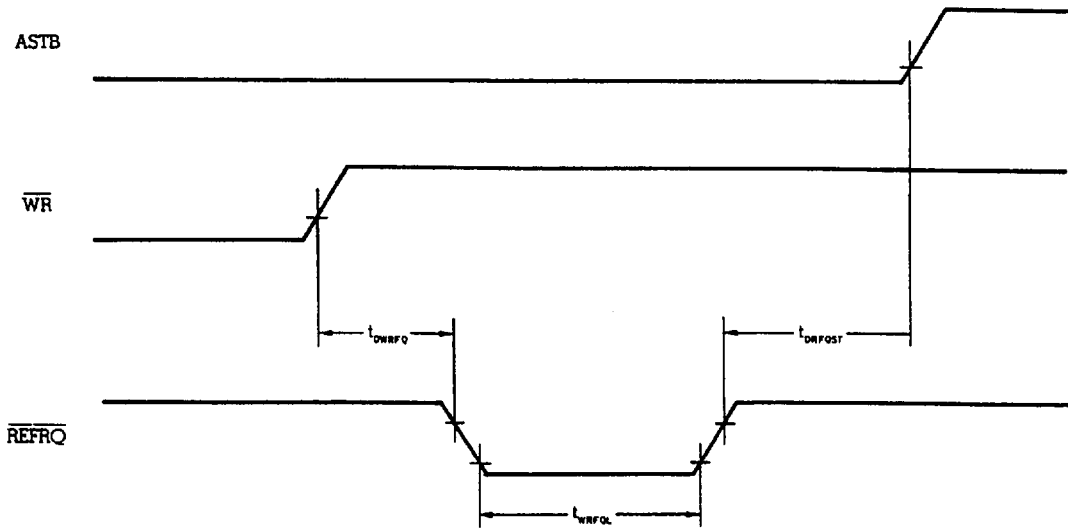
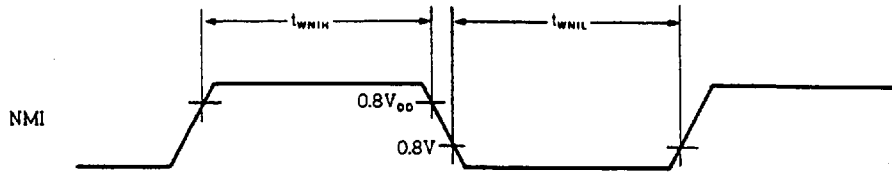## Serial Operation
3-line serial I/O mode
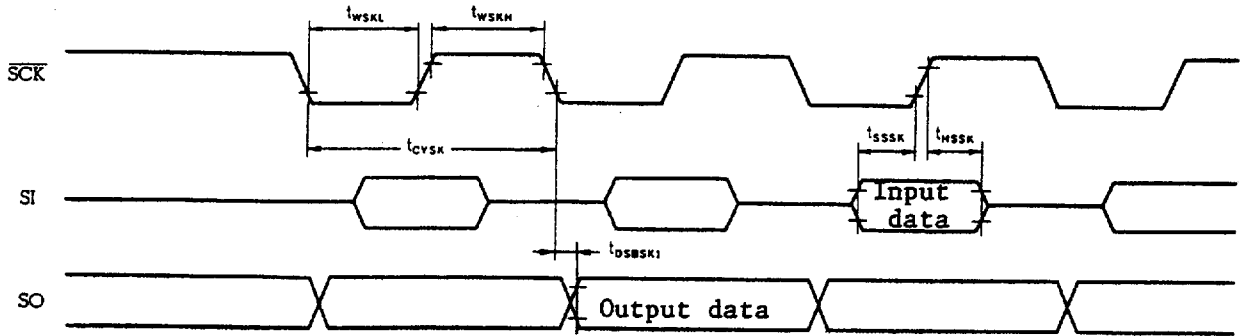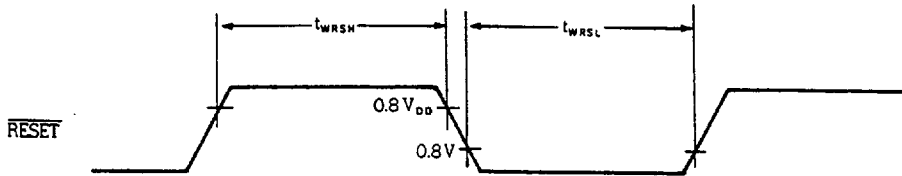

SBI Mode
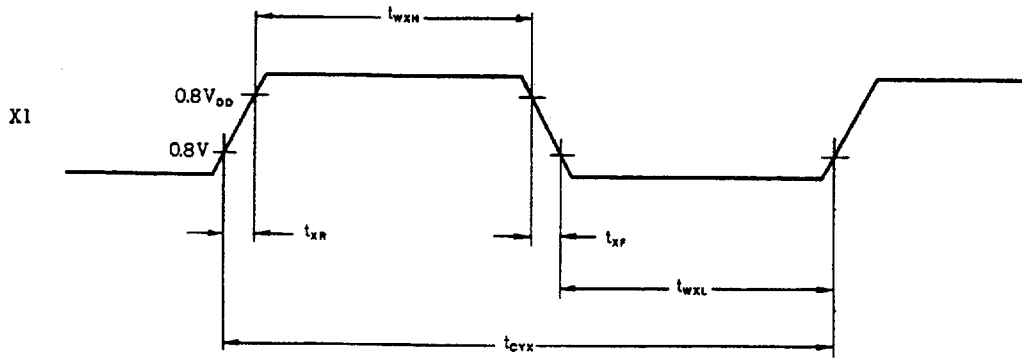## Bus release signal transfer
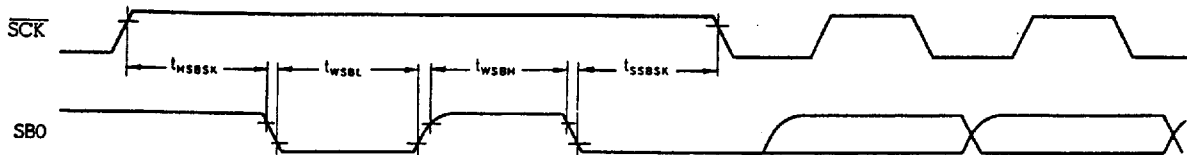
Command signal transfer

Interrupt Input Timing

NMI

t_{WNIH} t_{WNIL}

$0.8V_{DD}$

$0.8V$

INTP0-INTP5

t_{WITH} t_{WITL}

$0.8V_{DD}$

$0.8V$

Reset Input Timing

$\overline{RESET}$

t_{WRSH} t_{WRSL}

$0.8V_{DD}$

$0.8V$

External Clock Timing

Data Retention Characteristics

STOP mode setting

V_{DD}

V_{DDOR}

t_{HVD} t_{FVD} t_{RVD} t_{DREL} t_{WAIT}

RESET

$0.8 V_{DD}$

$0.8 V$

NMI
(Released by falling edge)

$0.8 V_{DD}$

$0.8 V$

NMI
(Released by rising edge)

$0.8 V_{DD}$

$0.8 V$
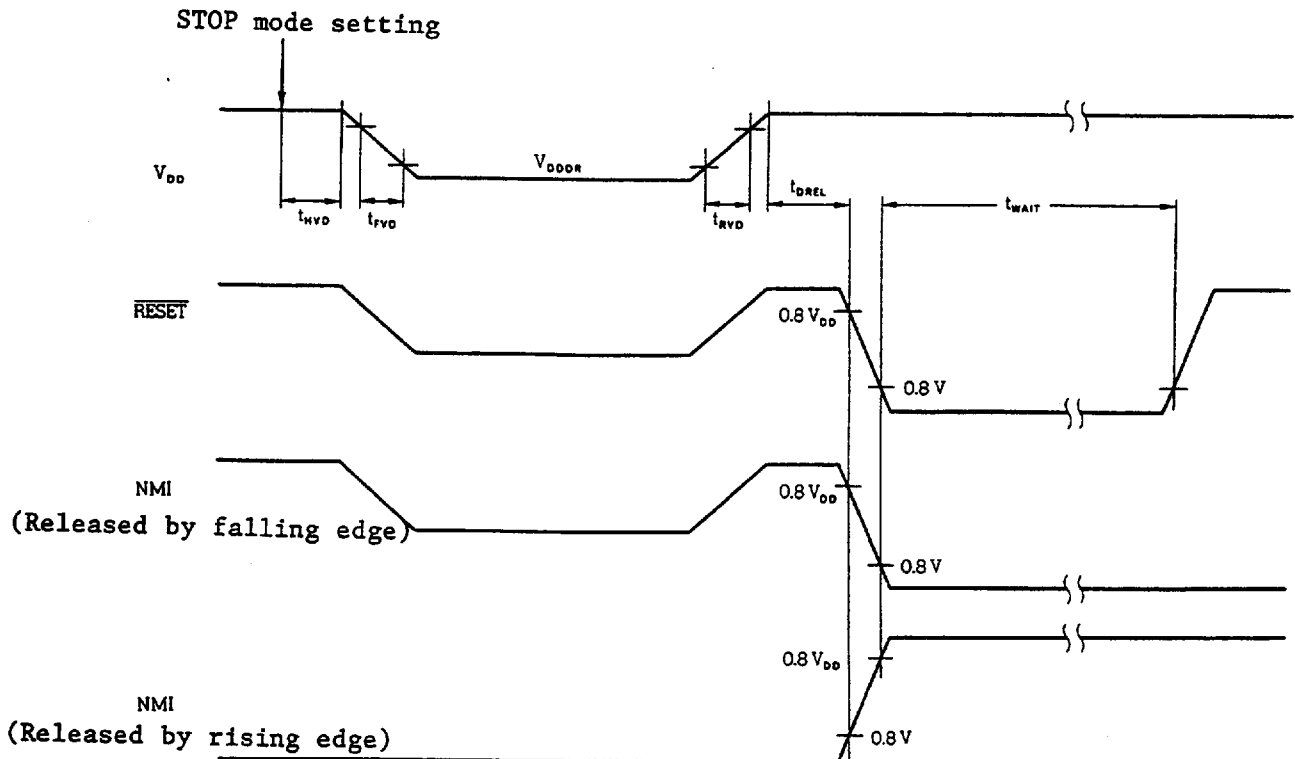
6. PACKAGE INFORMATION
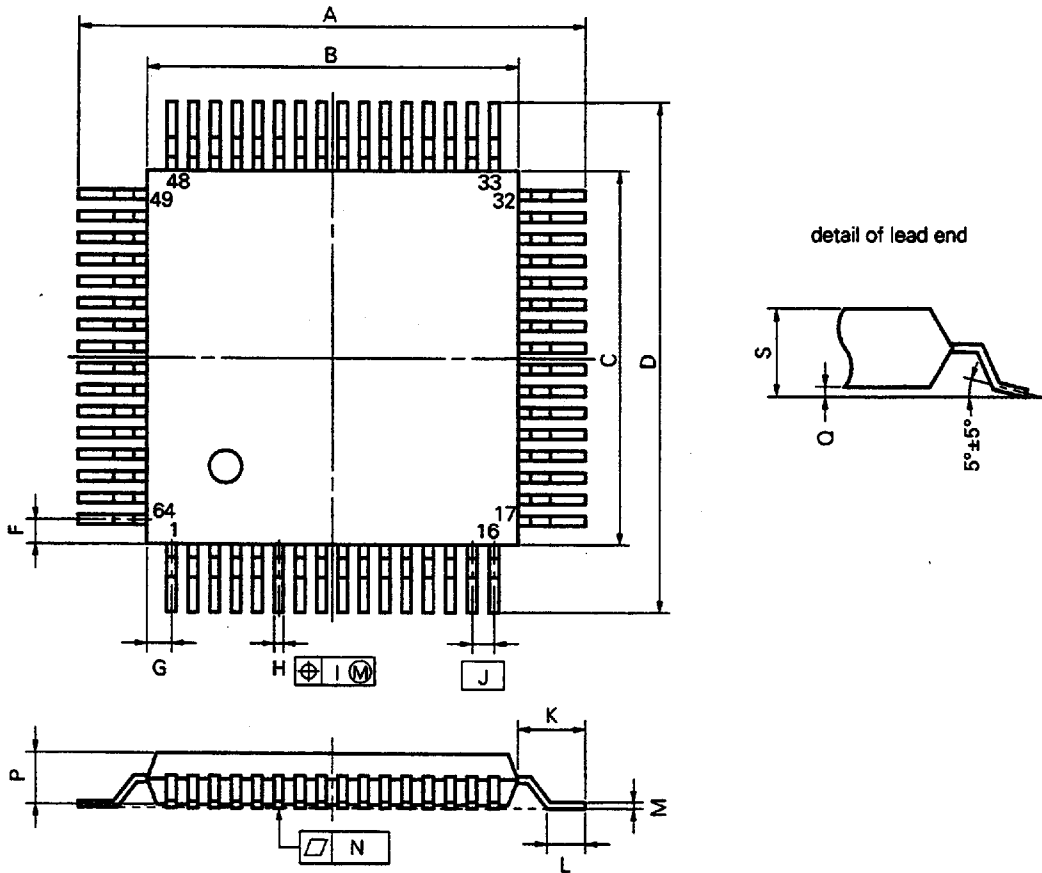
64PIN PLASTIC SHRINK DIP (750 mil)
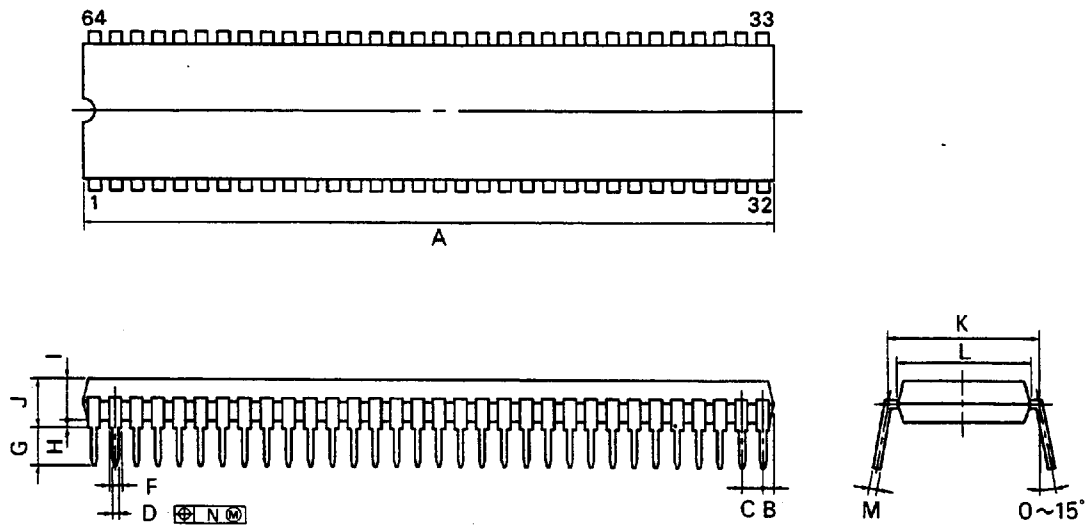
P64C-70-750A,C

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm0.3}$	$0.126^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

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64 PIN PLASTIC QFP (□14)

detail of lead end

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P64GC-80-AB8-3

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

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