The RF Line

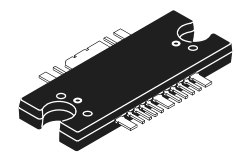
RF LDMOS Integrated Power Amplifiers

MWIC930R1
MWIC930GR1

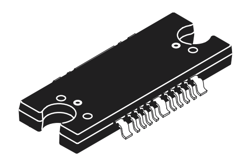
The MWIC930 wideband integrated circuit is designed for CDMA and GSM/GSM EDGE applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On Chip integral matching circuitry makes it usable from 746 to 960 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, N-CDMA and W-CDMA.

- Typical CDMA Performance: 27 Volts, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, 2-Carrier N-CDMA, IS -95, 869-894 MHz, 1.2288 MHz Channel Bandwidth, IM3 Measured in 1.2288 Integrated Bandwidth, ACPR Measured in 30 kHz Integrated Bandwidth, 2.5 MHz Carrier Spacing
  - Output Power — 5 Watts (Avg.)
  - Power Gain — 31 dB
  - Efficiency — 21%
  - Adjacent Channel Power — -52 dBc
  - IRL — -14 dB
- Typical Performance @ P1dB: 921-960 MHz, 26 Volts
  - Output Power — 30 Watts P1dB
  - Power Gain — 30 dB
  - Efficiency — 45%
- On Chip Matching (50 Ohm Input, >4 Ohm Output)
- Integrated Temperature Compensation Capability
- Integrated ESD Protection
- Usable for SCPA and MCPA Architecture
- Capable of Handling 5:1 VSWR, @ 26 Vdc, f = 921 MHz, P_{out} = 30 W CW, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA
- Can Be Bolted or Soldered through a Hole in the Circuit Board for Maximum Thermal Performance
- Also Available in Gull Wing for Surface Mount
- Available in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

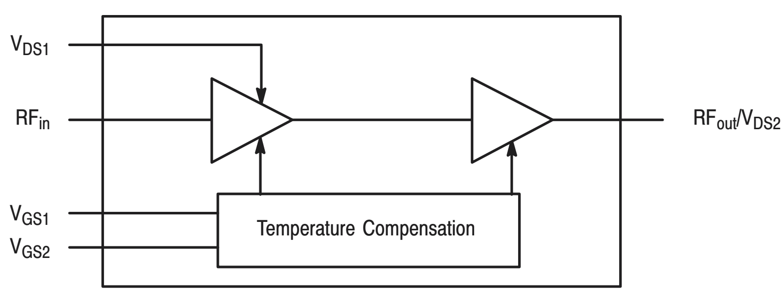
N-CDMA, W-CDMA, GSM/GSM EDGE, 746 - 960 MHz, 30 W, 26-28 V RF LDMOS INTEGRATED POWER AMPLIFIERS



CASE 1329-09
TO-272 WB-16
PLASTIC
MWIC930R1

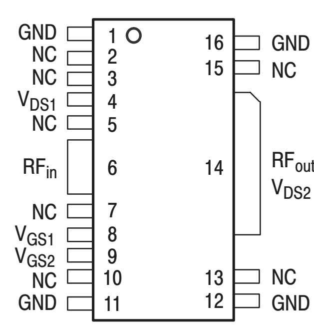


CASE 1329A-03
TO-272 WB-16 GULL
PLASTIC
MWIC930GR1



Functional Block Diagram

PIN CONNECTIONS



(Top View)

MOTOROLA intelligence everywhere™ digital dna™

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
GSM Application (P_{out} = 30 W CW)	Stage 1, 27 Vdc, I_{DQ} = 90 mA Stage 2, 27 Vdc, I_{DQ} = 240 mA		1.22	
GSM EDGE Application (P_{out} = 15 W CW)	Stage 1, 27 Vdc, I_{DQ} = 90 mA Stage 2, 27 Vdc, I_{DQ} = 240 mA		1.39	
CDMA Application (P_{out} = 5 W CW)	Stage 1, 27 Vdc, I_{DQ} = 90 mA Stage 2, 27 Vdc, I_{DQ} = 240 mA		1.50	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

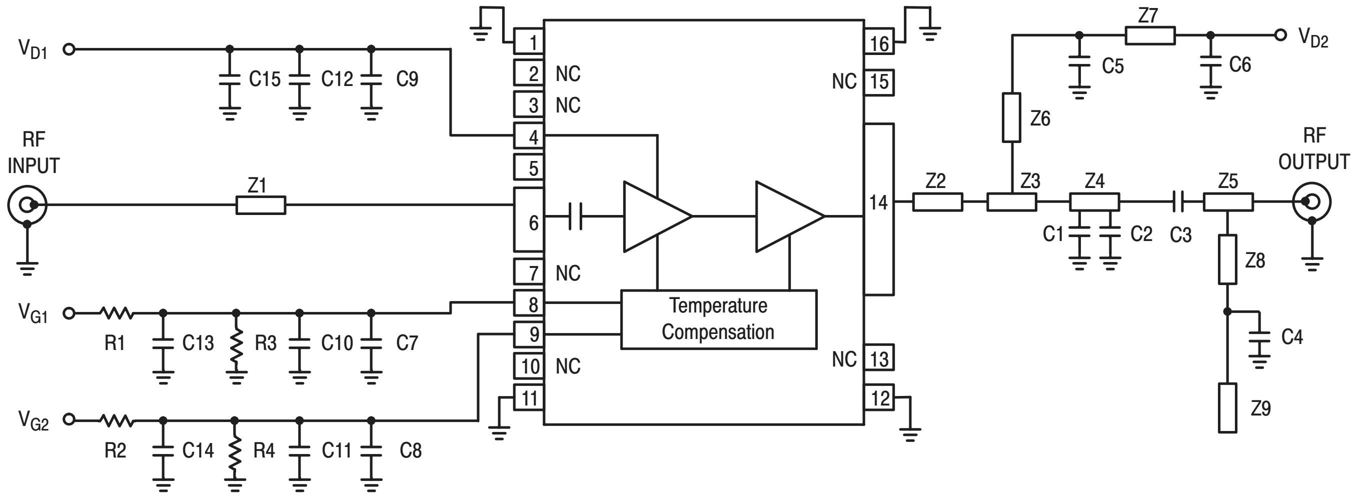
CDMA FUNCTIONAL TESTS (In Motorola CDMA Test Fixture, 50 ohm system) 1-Carrier N-CDMA, 869-894 MHz, IS-95 CDMA Pilot, Sync, Paging, Traffic Codes 8 through 13.

Characteristic	Symbol	Min	Typ	Max	Unit
Common-Source Amplifier Power Gain (V_{DD} = 27 Vdc, P_{out} = 5 W Avg., 1-Carrier N-CDMA, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, f = 869-894 MHz)	G_{ps}	28	31	—	dB
Drain Efficiency (V_{DD} = 27 Vdc, P_{out} = 5 W Avg., 1-Carrier N-CDMA, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, f = 869-894 MHz)	η	18	21	—	%
Adjacent Channel Power Ratio (V_{DD} = 27 Vdc, P_{out} = 5 W Avg., 1-Carrier N-CDMA, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, f = 869-894 MHz)	ACPR	—	-52	-48	dBc
Input Return Loss (V_{DD} = 27 Vdc, P_{out} = 5 W Avg., 1-Carrier N-CDMA, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, f = 880 MHz)	IRL	—	-12	-9	dB

(continued)

ELECTRICAL CHARACTERISTICS - continued (T_C = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PERFORMANCE TESTS (In Motorola Test Fixture) V_{DS} = 26 V, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA					
Quiescent Current Accuracy over Temperature (-10 to 85°C) at Nominal Value	ΔI_{QT}	—	±5	—	%
Gain Flatness in 80 MHz Bandwidth @ P_{out} = 5 W CW (Characterize from 840-920 MHz)	G_F	—	0.3	—	dB
Deviation from Linear Phase in 80 MHz Bandwidth @ P_{out} = 5 W CW (Characterize from 840-920 MHz)	Φ	—	0.6	—	°
Delay @ P_{out} = 5 W CW	Delay	—	3	—	ns
Insertion Phase Window @ P_{out} = 5 W CW	$\Phi\Delta$	—	±15	—	°
GSM/GSM EDGE FUNCTIONAL TESTS (In Motorola GSM Test Fixture) V_{DS} = 27 V, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, 921-960 MHz, CW					
Output Power at 1dB Compression Point	P1dB	—	30	—	Watts
Common-Source Amplifier Power Gain @ P1dB	G_{ps}	—	30	—	dB
Drain Efficiency @ P1dB	η	—	45	—	%
Input Return Loss @ P1dB	IRL	—	-12	—	dB
Third Order Intermodulation Distortion (15 W, 2-Tone 100 kHz Spacing)	IMD3	—	-30	—	dBc
Third Order Intermodulation Distortion (1 W, 2-Tone 100 kHz Tone Spacing)	IMD3 backoff	—	-45	—	dBc
Gain Flatness 921-960 MHz @ P_{out} = 5 W CW	G_F	—	0.3	—	dB
Deviation from Linear Phase 921-960 MHz @ P_{out} = 5 W CW	Φ	—	0.6	—	°



Z1	0.0438″ x 0.970″ 50 Ω Microstrip (not including lead pad)	Z5	0.0438″ x 0.2009″ Microstrip
Z2	0.234″ x 0.1183″ Microstrip (including lead pad)	Z6	0.0504″ x 0.528″ Microstrip
Z3	0.1575″ x 0.0938″ Microstrip	Z7	0.0504″ x 0.150″ Microstrip
Z4	0.08425″ x 0.584″ Microstrip	Z8	0.0254″ x 0.880″ Microstrip
		Z9	0.0254″ x 0.250″ Microstrip
		PCB	Rogers 4350, 0.020″, ε_r = 3.50

Figure 1. 746-960 MHz Test Fixture Schematic

Table 1. 746-960 MHz Test Fixture Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
*C1	15 pF High Q Capacitor	ATC600S150JW	ATC
*C2	6.8 pF High Q Capacitor - GSM Fixture 8.2 pF High Q Capacitor - CDMA Fixture	ATC600S6R8CW ATC600S8R2CW	ATC
*C3	5.6 pF High Q Capacitor	ATC600S5R6CW	ATC
*C4, C5, C7, C8, C9	47 pF High Q Capacitors	ATC600S470JW	ATC
C6, C13, C14, C15	1 μF Chip Capacitors	GRM42-2X7R105K050AL	Murata
C10, C11, C12	10 nF Chip Capacitors	C0603C103J5R	Kemet
R1, R2	1 kΩ, 1/8 W Chip Resistors	RM73B2AT102J	KOA Speer
R3, R4	1 MΩ, 1/4 W Chip Resistors	RM73B2BT105J	KOA Speer

* For output matching and bypass purposes, it is strongly recommended to use these exact capacitors.

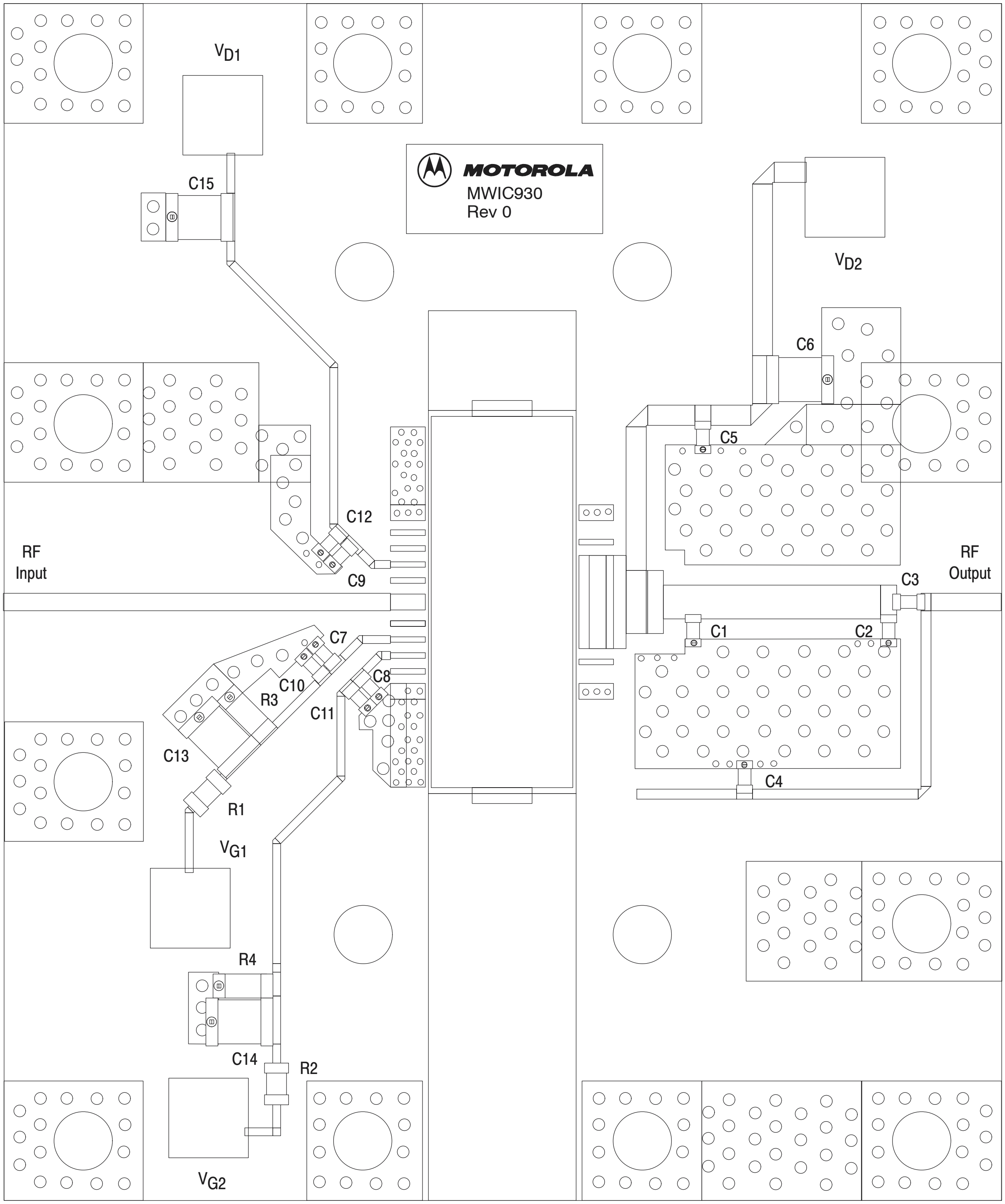


Figure 2. 746-960 MHz Test Circuit Component Layout

TYPICAL CHARACTERISTICS

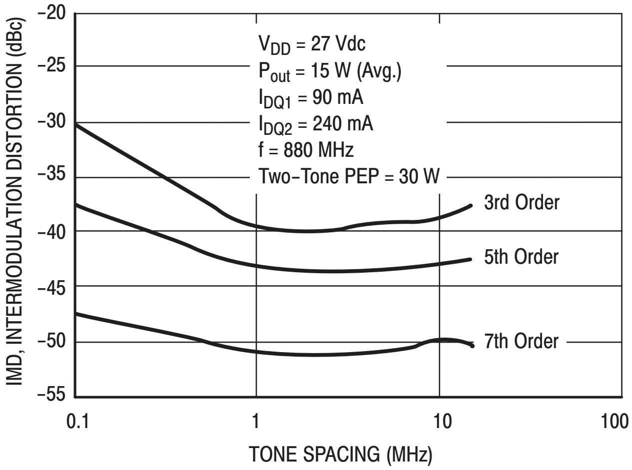


Figure 3. Two-Tone Broadband Performance

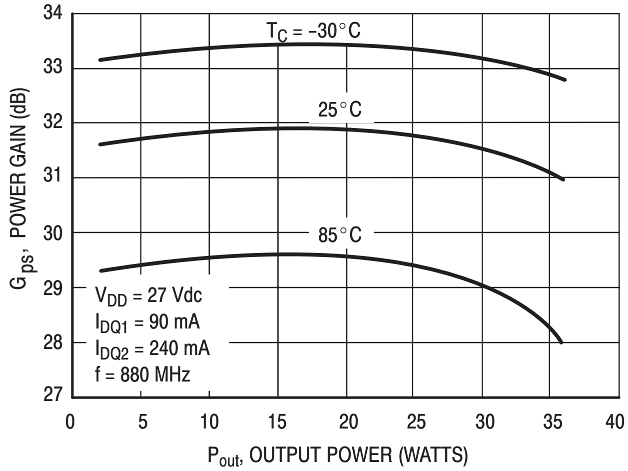


Figure 4. Power Gain versus Output Power

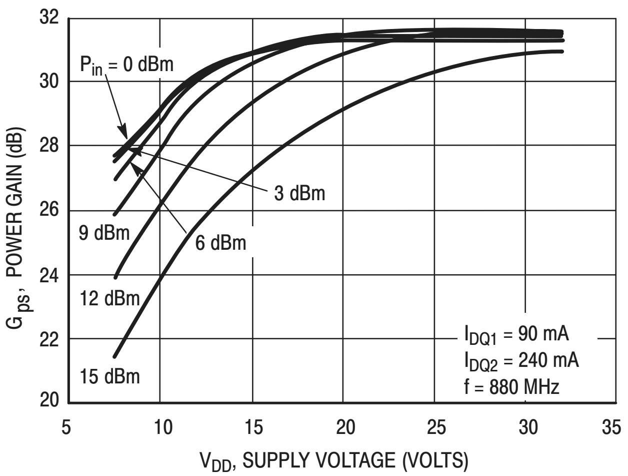


Figure 5. Power Gain versus Supply Voltage

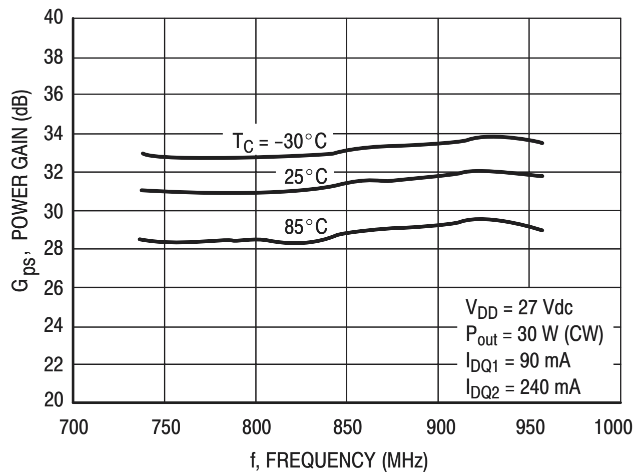


Figure 6. Power Gain versus Frequency

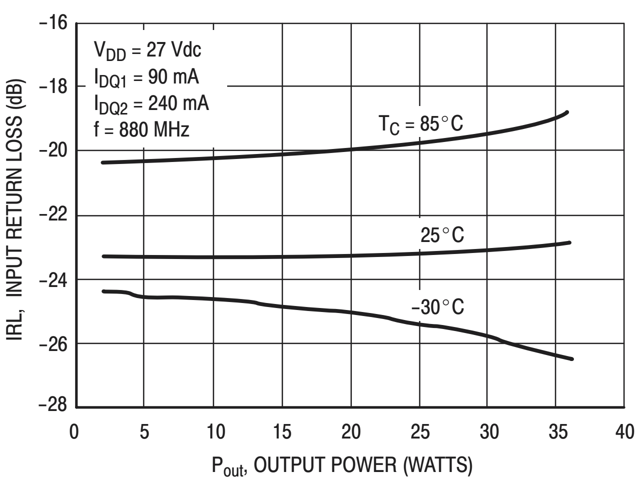


Figure 7. Input Return Loss versus Output Power

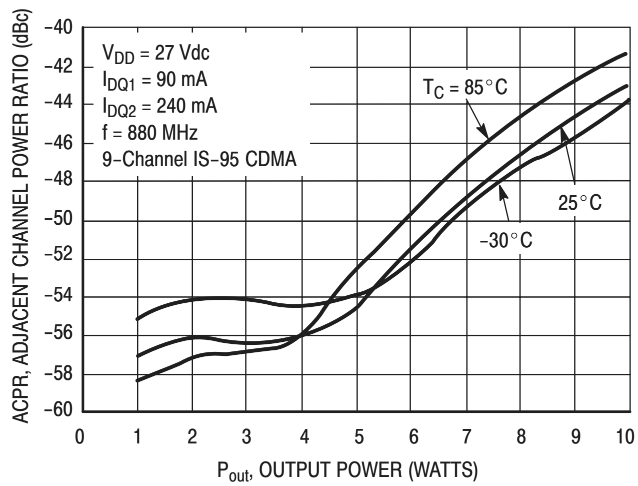


Figure 8. Adjacent Channel Power Ratio versus Output Power

TYPICAL CHARACTERISTICS

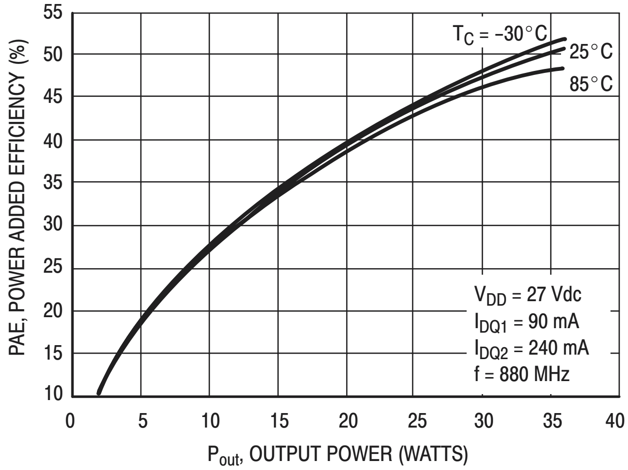


Figure 9. Power Added Efficiency versus Output Power

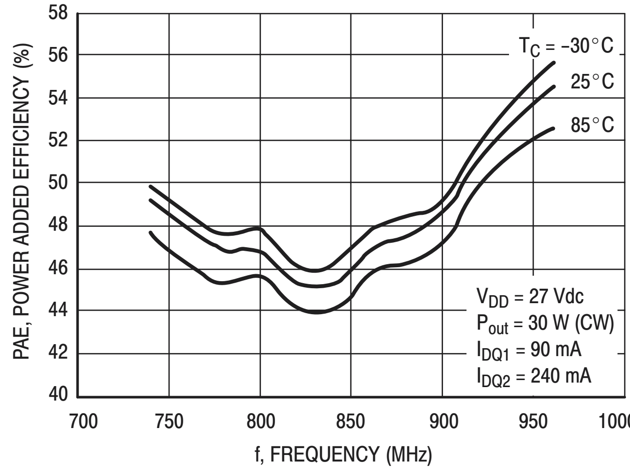
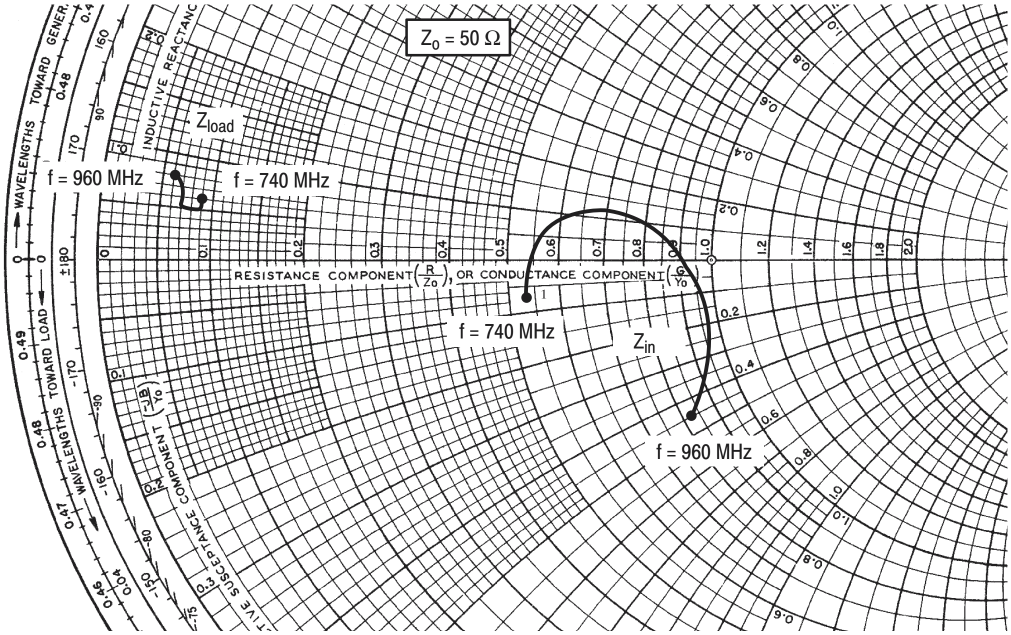


Figure 10. Power Added Efficiency versus Frequency



V_{DD} = 27 Vdc, I_{DQ1} = 90 mA, I_{DQ2} = 240 mA, P_{out} = 5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
740	26.61 - j3.68	4.28 + j2.99
760	26.88 - j0.53	4.37 + j2.91
780	28.22 + j2.21	4.39 + j2.79
800	30.57 + j4.31	4.34 + j2.64
820	33.79 + j5.53	4.21 + j2.54
840	37.83 + j5.30	4.06 + j2.52
860	41.92 + j3.42	3.90 + j2.58
880	45.58 - j0.40	3.73 + j2.70
900	47.77 - j5.84	3.59 + j2.93
920	47.83 - j12.15	3.43 + j3.17
940	45.55 - j18.05	3.28 + j3.44
960	41.58 - j22.64	3.13 + j3.75

Z_{in} = Device input impedance as measured from RF input to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

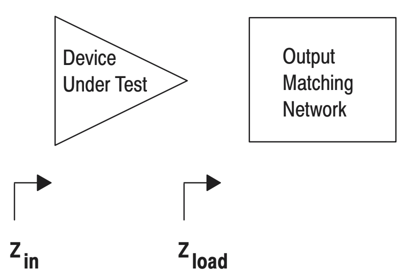
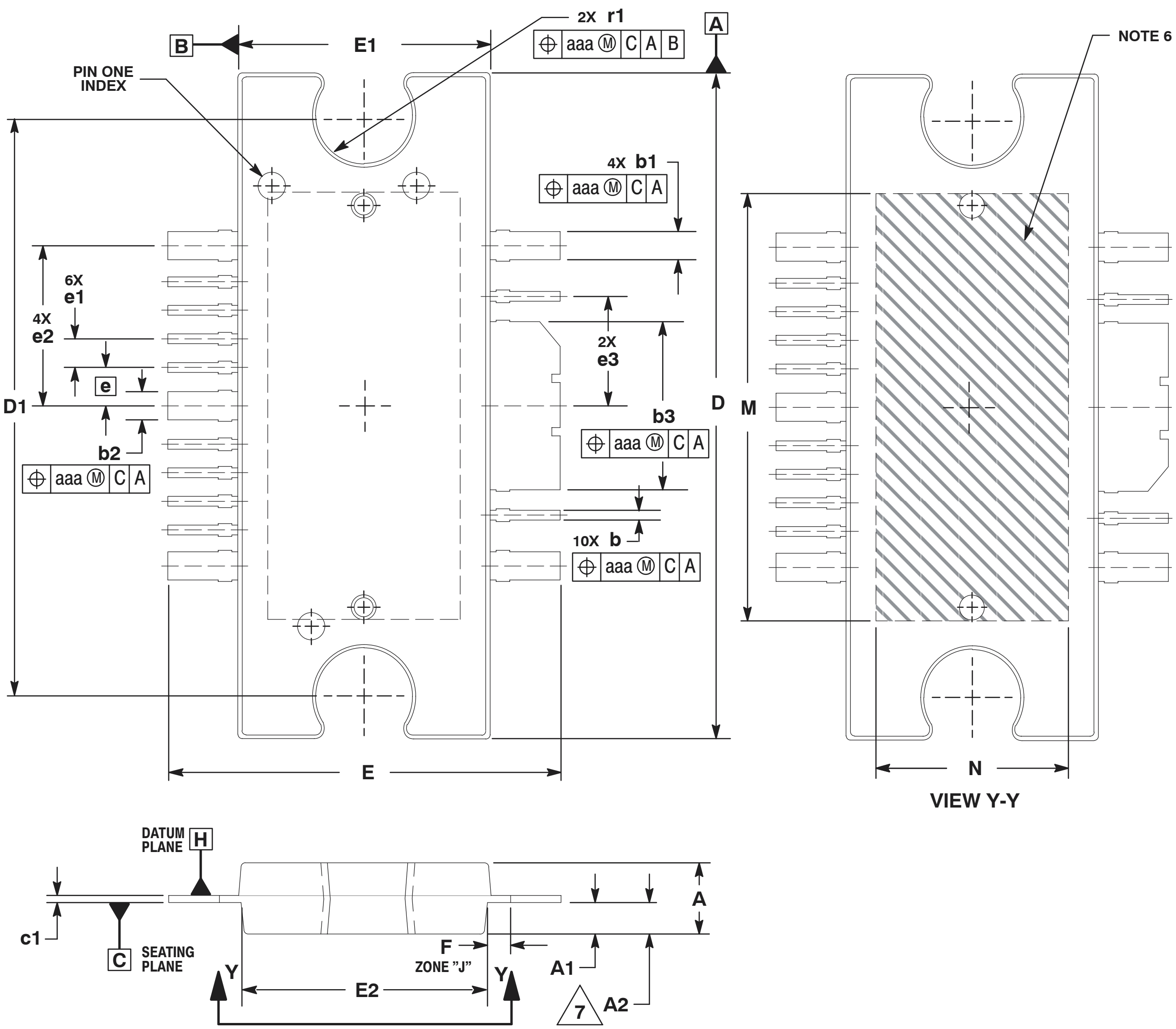


Figure 11. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.551	.559	14.00	14.20
E1	.353	.357	8.97	9.07
E2	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
aaa	.004		.10	

CASE 1329-09
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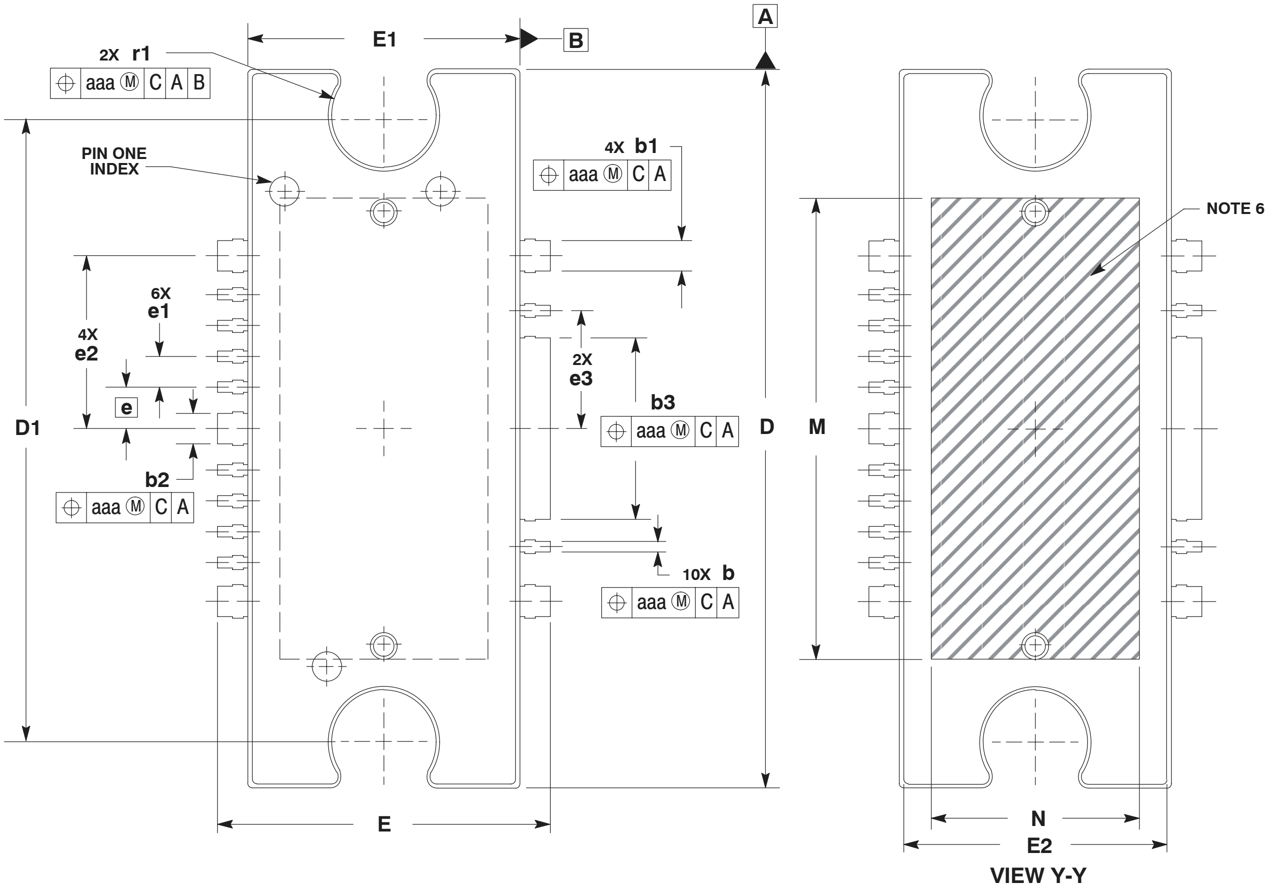
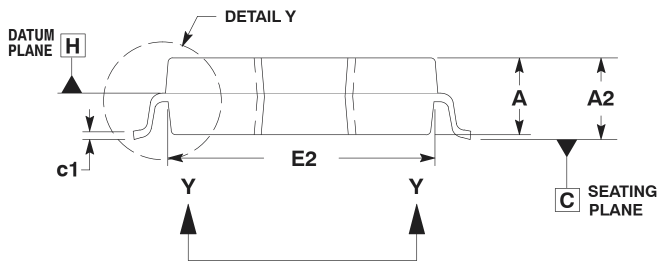
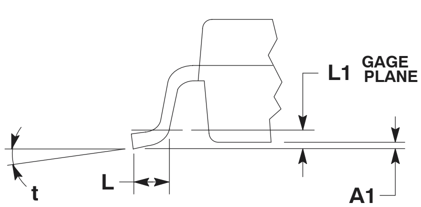
TO-272 WB-16
PLASTIC
MWIC930R1







DETAIL Y

NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DATUM PLANE −H− IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SINK.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.001	.004	0.02	0.10
A2	.099	.110	2.51	2.79
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.429	.437	10.90	11.10
E1	.353	.357	8.97	9.07
E2	.346	.350	8.79	8.89
L	.018	.024	4.90	5.06
L1	.01 BSC		0.25 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
t	2°	8°	2°	8°
aaa	.004		.10	

CASE 1329A-03
ISSUE B
TO-272 WB-16 GULL
PLASTIC
MWIC930GR1

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