

Features

- Mitel ST-BUS compatible
- 4-line x 32-channel inputs
- 4-line x 32-channel outputs
- 128 ports non-blocking switch
- Single power supply (+5 V)
- Low power consumption: 30 mW Typ.
- Microprocessor-control interface
- Three-state serial outputs

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Ord	ering Information	
MT8981DE MT8981DP	40 Pin Plastic DIP 44 PLCC	
-40)°C to +85°C	

Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 128 64 kbit/s channels. Each of the four serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s ST-BUS stream. In addition, the MT8981 provides microprocessor read and write access to individual ST-BUS channels.





Figure 2 - Pin Connections

Pin Description

Pi	Pin #		
40 DIP	44 PLCC	Name	Description
1	2	DTA	Data Acknowledgement (Open Drain Output). This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data. A 909 Ω , 1/4W, resistor is recommended to be used as a pullup.
2-4	3-5	STi0- STi2	ST-BUS Input 0 to 2 (Inputs). These are the inputs for the 2048 kbit/s ST-BUS input streams.
5	7	STi3	ST-BUS Input 3 (Input). These are the inputs for the 2048 kbit/s ST-BUS input streams.
6-9	8-11	IC	Internal Connections. Must be connected to V _{DD} .
10	12	V_{DD}	Power Input. Positive Supply.
11	13	F0i	Framing 0-Type (Input). This is the input for the frame synchronization pulse for the 2048 kbit/s ST-BUS streams. A low on this input causes the internal counter to reset on the next negative transition of $\overline{C4i}$.
12	14	C4i	4.096 MHz Clock (Input). ST-BUS bit cell boundaries lie on the alternate falling edges of this clock.
13- 15	15- 17	A0-A2	Address 0 to 2 (Inputs). These are the inputs for the address lines on the microprocessor interface.
16- 18	19- 21	A3-A5	Address 3 to 5 (Inputs). These are the inputs for the address lines on the microprocessor interface
19	22	DS	Data Strobe (Input). This is the input for the active high data strobe on the microprocessor interface.
20	23	R/W	Read or Write (Input). This is the input for the read/write signal on the microprocessor interface - high for read, low for write.
21	24	CS	Chip Select (Input). This is the input for the active low chip select on the microprocessor interface.

Pin Description (continued)

Pi	n #							
40 DIP	44 PLCC	Name	Description					
22- 24	25- 27	D7-D5	Data 7 to 5 (Three-state I/O Pins). These are the bidirectional data pins on the microprocessor interface.					
25- 29	29- 33	D4-D0	Data 4 to 0 (Three-state I/O Pins). These are the bidirectional data pins on the microprocessor interface.					
30	34	V _{SS}	Power Input. Negative Supply (Ground).					
31- 34	35- 38	IC	Internal Connections. Leave pins disconnected.					
35	39	STo3	ST-BUS Output 3 (Three-state Outputs). These are the pins for the four 2048 kbit/s ST-BUS output streams.					
36- 38	41- 43	STo2- STo0	ST-BUS Output 2 to 0 (Three-state Outputs). These are the pins for the four 2048 kbit/s ST-BUS output streams.					
39	44	ODE	Output Drive Enable (Input). If this input is held high, the STo0-STo3 output drivers function normally. If this input is low, the STo0-STo3 output drivers go into their high impedance state. NB: Even when ODE is high, channels on the STo0-STo3 outputs can go high impedance under software control.					
40	1	IC	Internal Connection. Leave pin disconnected.					

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, MITEL has devised the ST-BUS (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS operate continuously at 2048 kbit/s and are arranged in 125 μ s wide frames which contain 32 8-bit channels. MITEL manufactures a number of devices which interface to the ST-BUS; a key device being the MT8981 chip.

The MT8981 can switch data from channels on ST-BUS inputs to channels on ST-BUS outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS inputs or write to channels on ST-BUS outputs (Message Mode). To the microprocessor, the MT8981 looks like a memory peripheral. The microprocessor can write to the MT8981 to establish switched connections between input ST-BUS channels and output ST-BUS channels, or to transmit messages on output ST-BUS channels. By reading from the MT8981, the microprocessor can receive messages from ST-BUS input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the MT8981 allows systems to use distributed processing and to switch voice or data in an ST-BUS architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the four ST-BUS inputs (STi0 to STi3), and serial data is transmitted at the four ST-BUS outputs (STo0 to STo3). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g., MITEL's MT8964).

This serial input word is converted into parallel data and stored in the 128 X 8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on an ST-BUS output, the data for the channel can either be switched from an ST-BUS input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals \overline{CS} , \overline{DTA} , R/W and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the

A5	A4	A3	A2	A1	A0	HEX ADDRESS	LOCATION
0 1 • • 1	X 0 0 • • 1	X 0 0 • 1	X 0 0 • 1	X 0 0 • • 1	X 0 1 • 1	00 - 1F 20 21 • • 3F	Control Register * Channel 0 [†] Channel 1 [†] • • • Channel 31 [†]
* Writir	ng to the	Control	Registe	r is the a	only fast	transaction.	

† Memory and stream are specified by the contents of the Control Register.

Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of MT8981s to be constructed. It also controls the CSTo pin.

All ST-BUS timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

Software Control

The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory. If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Fig. 3). If A5 is high, then the address lines A4-A0 select the memory location corresponding to channel 0-31 for the memory and stream selected in the Control Register.

The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Fig. 4). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS input or output streams.

Bit 7 of the Control Register allows split memory operation - reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

		Mode (unused) Memory (unused) Stream Control Bits 7 6 5 4 3 2 1 0							
BIT	NAME	DESCRIPTION							
7	Split Memory	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.							
6	Message Mode	When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.							
5	(unused)								
4-3	Memory Select Bits	0-0 - Not to be used 0-1 - Data Memory (read only from the microprocessor port) 1-0 - Connection Memory Low 1-1 - Connection Memory High							
2	(unused)	Must be a 0.							
1-0	Stream Address Bits	The number expressed in binary notation on these bits refers to the input or output ST- BUS stream which corresponds to the subsection of memory made accessible for subsequent operations.							



Figure 5 - Connection Memory High Bits



Figure 6 - Connection Memory Low Bits

If bit 6 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Fig. 5). If bit 2 is 1, the associated ST-BUS output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS input stream and channel where the byte is to be found (see Fig. 6).

If the ODE pin is low, then all serial outputs are highimpedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS output stream and channel. Bit 0=1 enables the driver and bit 0=0 disables it (see Fig. 5).

Applications

Use in a Simple Digital Switching System

Fig. 7 and 8 show how MT8981s can be used with MT8964s to form a simple digital switching system. Fig. 7 shows the interface between the MT8981s and the filter/codecs. Fig. 8 shows the position of these components in an example architecture.

The MT8964 filter/codec in Fig. 7 receives and transmits digitised voice signals on the ST-BUS input D_R , and ST-BUS output D_X , respectively. These signals are routed to the ST-BUS inputs and outputs on the top MT8981, which is used as a digital speech switch.

The MT8964 is controlled by the ST-BUS input D_c originating from the bottom MT8981, which generates the appropriate signals from an output channel in Message Mode. This architecture optimises the messaging capability of the line circuit by building signalling logic, e.g., for on-off hook detection, which communicates on an ST-BUS output. This signalling ST-BUS output is monitored by a microprocessor (not shown) through an ST-BUS input on the bottom MT8981.

Fig. 8 shows how a simple digital switching system may be designed using the ST-BUS architecture. This is a private telephone network with 128 extensions which uses a single MT8981 as a speech switch and a second MT8981 for communication with the line interface circuits.

A larger digital switching system may be designed by cascading a number of MT8981s. Fig. 9 shows how four MT8981s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS inputs to any channel on the ST-BUS outputs.





Application Circuit with 6802 Processor

Fig. 10 shows an example of a complete circuit which may be used to evaluate the chip.

For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both are within the limits of the chip's specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the \overline{FP} signal, but the values used may have to be changed if faster 393 counters become available.

The chip is shown as memory mapped into the MEK6802D3 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The MEK6802D3 board uses a $10K\Omega$ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.



Figure 9 - Four 8981s Arranged in a Non-Blocking 8 x 8 Configuration



Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	V _{DD} - V _{SS}		-0.3	7	V
2	Voltage on Digital Inputs	VI	V _{SS} -0.3	V _{DD} +0.3	V
3	Voltage on Digital Outputs	Vo	V _{SS} -0.3	V _{DD} +0.3	V
4	Current at Digital Outputs	Ι _ο		40	mA
5	Storage Temperature	Τs	-65	+150	°C
6	Package Power Dissipation	P _D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Min	Тур [‡]	Max	Units	Test Conditions
1	Operating Temperature	T _{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	4.75		5.25	V	
3	Input Voltage	VI	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Тур‡	Max	Units	Test Conditions
1		Supply Current	I _{DD}		6	10	mA	Outputs unloaded
2	Ň	Input High Voltage	V _{IH}	2.0			V	
3	P U	Input Low Voltage	V _{IL}			0.8	V	
4	T	Input Leakage	I			5	μΑ	$V_{\rm I}$ between $V_{\rm SS}$ and $V_{\rm DD}$
5	S	Input Pin Capacitance	Cı		8		pF	
6		Output High Voltage	V _{OH}	2.4			V	I _{OH} = 10 mA
7	U	Output High Current	I _{ОН}	10	15		mA	Sourcing. V _{OH} =2.4V
8	T	Output Low Voltage	V _{OL}			0.4	V	I _{OL} = 5 mA
9		Output Low Current	I _{OL}	5	10		mA	Sinking. $V_{OL} = 0.4V$
10	T	High Impedance Leakage	I _{oz}			5	μΑ	$V_{\rm O}$ between $V_{\rm SS}$ and $V_{\rm DD}$
11		Output Pin Capacitance	Co		8		pF	

[‡] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



Figure 11 - Output Test Load

		Characteristics	Sym	Min	Тур [‡]	Max	Units	Test Conditions
1		Clock Period*	t _{CLK}	220	244	300	ns	
2	1	Clock Width High	t _{CH}	95	122	150	ns	
3	N	Clock Width Low	t _{CL}	110	122	150	ns	
4	P	Clock Transition Time	t _{CTT}		20		ns	
5	T	Frame Pulse SetupTime	t _{FPS}	20		200	ns	
6	S	Frame Pulse Hold Time	t _{FPH}	0.020		50	μs	
7		Frame Pulse Width	t _{FPW}		244		ns	

AC Electrical Characteristics[†] - Clock Timing (Figures 12 and 13)

† Timing is over recommended temperature & power supply voltages
 ‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
 * Contents of Connection Memory are not lost if the clock stops, however, ST-BUS outputs go into the high impedance state.

NB: Frame Pulse is repeated every 512 cycles of $\overline{C4i}$.



Figure 12 - Frame Alignment



		Characteristics	Sym	Min	Тур‡	Max	Units	Test Conditions
1		STo0/3 Delay - Active to High Z	t _{SAZ}	20	50	80	ns	R_L =1 K Ω^* , C_L =150 pF
2	0	STo0/3 Delay - High Z to Active	t _{SZA}	25	60	125	ns	C _L =150 pF
3	U T	STo0/3 Delay - Active to Active	t _{SAA}	30	65	125	ns	C _L =150 pF
4	P	STo0/3 Hold Time	t _{SOH}	25	45		ns	C _L =150 pF
5	U T	Output Driver Enable Delay	t _{OED}		45	125	ns	$R_L=1 \text{ K}\Omega^*, C_L=150 \text{ pF}$
6	S	External Control Hold Time	t _{xCH}	0	50		ns	C _L =150 pF
7		External Control Delay	t _{XCD}		75	110	ns	C _L =150 pF
8	I	Serial Input Setup Time	t _{sis}		-40	-20	ns	
9	N	Serial Input Hold Time	t _{SIH}	90			ns	

AC Electrical Characteristics[†] - Serial Streams (Figures 11, 14, 15 and 16)

† Timing is over recommended temperature & power supply voltages

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.



Figure 14 - Serial Outputs and External Control



Figure 15 - Output Driver Enable



Figure 16 - Serial Inputs

	Characteristics	Sym	Min	Тур [‡]	Max	Units	Test Conditions
1	Chip Select Setup Time	t _{CSS}	20	0		ns	
2	Read/Write Setup Time	t _{RWS}	25	5		ns	
3	Address Setup Time	t _{ADS}	25	5		ns	
4	Acknowledgement Delay Fast	t _{AKD}		40	100	ns	C _L =150 pF
	Slow	t _{AKD}	2.7		7.2	cycles	C4i cycles ^①
5	Fast Write Data Setup Time	t _{FWS}	20			ns	
6	Slow Write Data Delay	t _{SWD}		2.0	1.7	cycles	C4i cycles ^①
7	Read Data Setup Time	t _{RDS}			0.5	cycles	$\overline{C4i} \text{ cycles}^{\textcircled{1}}, \text{ C}_{L} = 150 \text{ pF}$
8	Data Hold Time Read	t _{DHT}	20			ns	$R_L=1 K\Omega^*$, $C_L=150 pF$
	Write	t _{DHT}	20	10		ns	
9	Read Data To High Impedance	t _{RDZ}		50	90	ns	$R_L=1 K\Omega^*$, $C_L=150 pF$
10	Chip Select Hold Time	t _{CSH}	0			ns	
11	Read/Write Hold Time	t _{RWH}	0			ns	
12	Address Hold Time	t _{ADH}	0			ns	
13	Acknowledgement Hold Time	t _{AKH}	10	60	80	ns	$R_L=1 \text{ K}\Omega^*, C_L=150 \text{ pF}$

AC Electrical Characteristics[†] - Processor Bus (Figures 11 and 17)

† Timing is over recommended temperature & power supply voltages.

* High Impedance is measured by pulling to the appropriate rail with R_L , with timing corrected to cancel time taken to discharge C_L . ① Processor accesses are dependent on the C4i clock, and so some timings are expressed as multiples of the C4i clock period.



Figure 17 - Processor Bus

Notes:

Package Outlines





1) Not to scale 2) Dimensions in inches

a) (Dimensions in millimeters)
b) For D & E add for allowable Mold Protrusion 0.010"

Dim	20-	Pin	28-	Pin	44-	Pin	68-	Pin	84-	Pin
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Α	0.165	0.180	0.165	0.180	0.165	0.180	0.165	0.200	0.165	0.200
	(4.20)	(4.57)	(4.20)	(4.57)	(4.20)	(4.57)	(4.20)	(5.08)	(4.20)	(5.08)
A ₁	0.090	0.120	0.090	0.120	0.090	0.120	0.090	0.130	0.090	0.130
	(2.29)	(3.04)	(2.29)	(3.04)	(2.29)	(3.04)	(2.29)	(3.30)	(2.29)	(3.30)
D/E	0.385	0.395	0.485	0.495	0.685	0.695	0.985	0.995	1.185	1.195
	(9.78)	(10.03)	(12.32)	(12.57)	(17.40)	(17.65)	(25.02)	(25.27)	(30.10)	(30.35)
D ₁ /E ₁	0.350	0.356	0.450	0.456	0.650	0.656	0.950	0.958	1.150	1.158
	(8.890)	(9.042)	(11.430)	(11.582)	(16.510)	(16.662)	(24.130)	(24.333)	(29.210)	(29.413)
D ₂ /E ₂	0.290	0.330	0.390	0.430	0.590	0.630	0.890	0.930	1.090	1.130
	(7.37)	(8.38)	(9.91)	(10.92)	(14.99)	(16.00)	(22.61)	(23.62)	(27.69)	(28.70)
е	0	0.004	0	0.004	0	0.004	0	0.004	0	0.004
F	0.026	0.032	0.026	0.032	0.026	0.032	0.026	0.032	0.026	0.032
	(0.661)	(0.812)	(0.661)	(0.812)	(0.661)	(0.812)	(0.661)	(0.812)	(0.661)	(0.812)
G	0.013	0.021	0.013	0.021	0.013	0.021	0.013	0.021	0.013	0.021
	(0.331)	(0.533)	(0.331)	(0.533)	(0.331)	(0.533)	(0.331)	(0.533)	(0.331)	(0.533)
Н	0.050 BSC 0.050 BSC		0.050	0.050 BSC		0.050 BSC		0.050 BSC		
	(1.27 BSC) (1.27 BSC)		(1.27	(1.27 BSC)		(1.27 BSC)		(1.27 BSC)		
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
	•	•	•	•	•	•		•	•	

Package Outlines





	8-Pin Plastic		16-Pin Plastic		18-Pin Plastic		20-Pin Plastic	
DIM								
	Min	Max	Min	Max	Min	Max	Min	Мах
Α		0.210 (5.33)		0.210 (5.33)		0.210 (5.33)		0.210 (5.33)
A ₂	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)	0.115 (2.92)	0.195 (4.95)
b	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)
b ₂	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)	0.045 (1.14)	0.070 (1.77)
С	0.008 (0.203)	0.014 (0.356)	0.008 (0.203)	0.014(0.356)	0.008 (0.203)	0.014 (0.356)	0.008 (0.203)	0.014 (0.356)
D	0.355 (9.02)	0.400 (10.16)	0.780 (19.81)	0.800 (20.32)	0.880 (22.35)	0.920 (23.37)	0.980 (24.89)	1.060 (26.9)
D ₁	0.005 (0.13)		0.005 (0.13)		0.005 (0.13)		0.005 (0.13)	
E	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)	0.300 (7.62)	0.325 (8.26)
E ₁	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)	0.240 (6.10)	0.280 (7.11)
е	0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)		0.100 BSC (2.54)	
e _A	0.300 BSC (7.62)		0.300 BSC (7.62)		0.300 BSC (7.62)		0.300 BSC (7.62)	
L	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)	0.115 (2.92)	0.150 (3.81)
e _B		0.430 (10.92)		0.430 (10.92)		0.430 (10.92)		0.430 (10.92)
e _C	0	0.060 (1.52)	0	0.060 (1.52)	0	0.060 (1.52)	0	0.060 (1.52)

NOTE: Controlling dimensions in parenthesis () are in millimeters.



Plastic Dual-In-Line Packages (PDIP) - E Suffix

	22-Pin		24-Pin		28-Pin		40-Pin	
DIM	Plastic		Plastic		Plastic		Plastic	
	Min	Max	Min	Max	Min	Max	Min	Max
Α		0.210 (5.33)		0.250 (6.35)		0.250 (6.35)		0.250 (6.35)
A ₂	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)	0.125 (3.18)	0.195 (4.95)
b	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)	0.014 (0.356)	0.022 (0.558)
b ₂	0.045 (1.15)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)	0.030 (0.77)	0.070 (1.77)
С	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.015 (0.381)
D	1.050 (26.67)	1.120 (28.44)	1.150 (29.3)	1.290 (32.7)	1.380 (35.1)	1.565 (39.7)	1.980 (50.3)	2.095 (53.2)
D ₁	0.005 (0.13)		0.005 (0.13)		0.005 (0.13)		0.005 (0.13)	
E	0.390 (9.91)	0.430 (10.92)	0.600 (15.24)	0.670 (17.02)	0.600 (15.24)	0.670 (17.02)	0.600 (15.24)	0.670 (17.02)
E			0.290 (7.37)	.330 (8.38)				
E ₁	0.330 (8.39)	0.380 (9.65)	0.485 (12.32)	0.580 (14.73)	0.485 (12.32)	0.580 (14.73)	0.485 (12.32)	0.580 (14.73)
E ₁			0.246 (6.25)	0.254 (6.45)				
е	0.100 BSC (2.54)							
e _A	0.400 BSC (10.16)		0.600 BSC (15.24)		0.600 BSC (15.24)		0.600 BSC (15.24)	
e _A			0.300 BSC (7.62)					
e _B				0.430 (10.92)				
L	0.115 (2.93)	0.160 (4.06)	0.115 (2.93)	0.200 (5.08)	0.115 (2.93)	0.200 (5.08)	0.115 (2.93)	0.200 (5.08)
α		15°		15°		15°		15°



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