

# Spread Spectrum Clock Generator

## MB88161

### DESCRIPTION

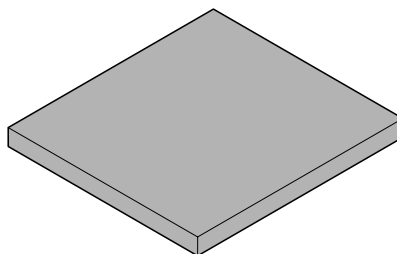
MB88161 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator.

### FEATURES

- Input frequency : 20 MHz to 28 MHz (Multiplied by 1), 14 MHz to 40 MHz (Multiplied by 2)
- Multiplication rate : 1, 2
- Output frequency : 20 MHz to 28 MHz (Multiplied by 1), 28 MHz to 80 MHz (Multiplied by 2)
- Modulation rate : no modulation,  $\pm 0.5\%$ ,  $\pm 1.0\%$ ,  $\pm 2.0\%$ ,  $-1.0\%$ ,  $-2.0\%$ ,  $-4.0\%$  (The terminal can be selected.)
- Equipped with oscillation circuit : Range of oscillation 10 MHz to 40 MHz
- Built-in oscillation stabilization capacitance : 4pF (Typ)
- Modulation clock output Duty : 40% to 60%
- Modulation clock Cycle-Cycle Jitter : Less than 100 ps
- Low current consumption by CMOS process : 7.0 mA (24 MHz : no load, Typ-sample, Typ-condition)
- Power supply voltage : 2.7 V to 3.6 V
- Operating temperature :  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Package : BCC 18-pin

### PACKAGE

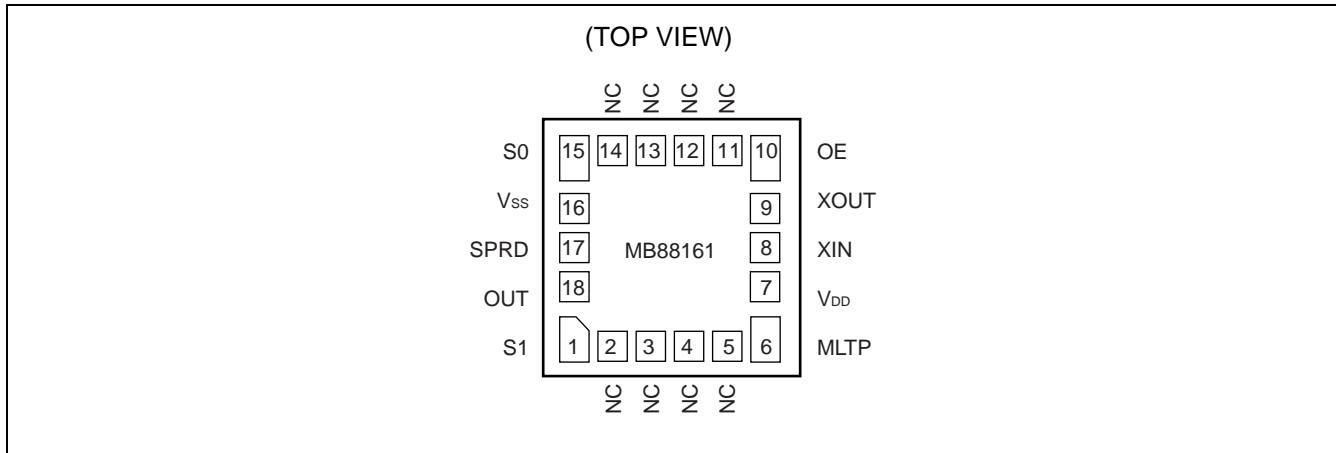
18-pin plastic BCC



(LCC-18P-M05)

# MB88161

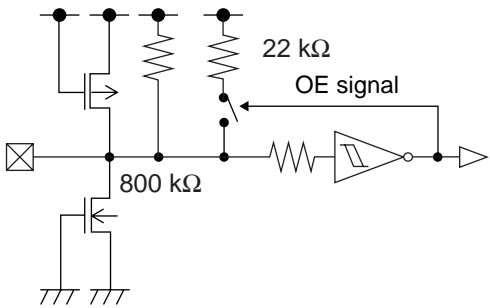
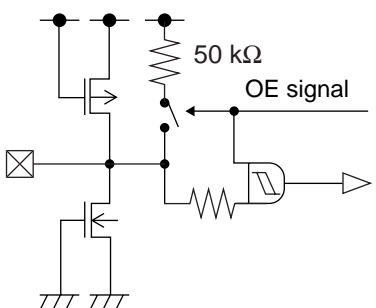
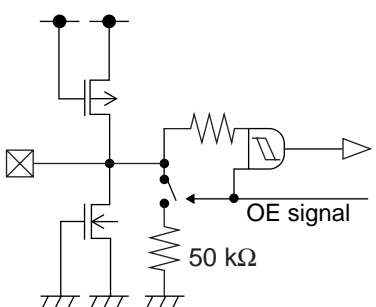
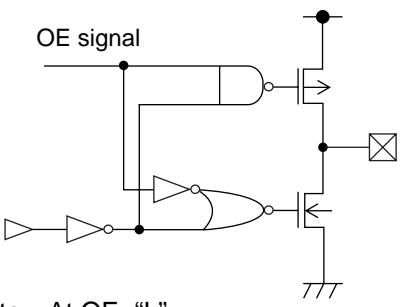
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Pin no.	Pin name	I/O	Description
1	S1	I	Modulation rate setting pin (with pull-up resistance)
2	NC	—	Non-connection pin (do not connect anything)
3	NC	—	Non-connection pin (do not connect anything)
4	NC	—	Non-connection pin (do not connect anything)
5	NC	—	Non-connection pin (do not connect anything)
6	MLTP	I	Multiplication rate setting pin (with pull-down resistance)
7	V <sub>DD</sub>	—	Power supply voltage pin
8	XIN	I	Resonator connection pin/clock input pin
9	XOUT	O	Resonator connection pin
10	OE	I	Clock output enable pin (with pull-up resistance)
11	NC	—	Non-connection pin (do not connect anything)
12	NC	—	Non-connection pin (do not connect anything)
13	NC	—	Non-connection pin (do not connect anything)
14	NC	—	Non-connection pin (do not connect anything)
15	S0	I	Modulation rate setting pin (with pull-up resistance)
16	V <sub>SS</sub>	—	GND pin
17	SPRD	I	Modulation type setting pin (with pull-up resistance)
18	OUT	O	Modulation clock output pin (OE= "L" Hi-Z output)

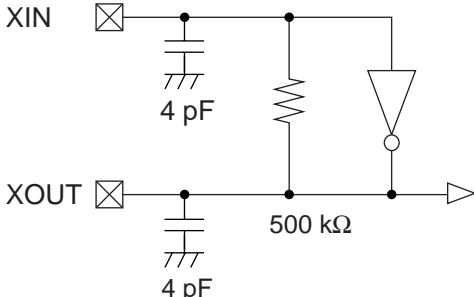
## ■ I/O CIRCUIT TYPE

Pin	Circuit type	Remarks
OE	 <p>Note : At OE="L" 22kΩ Pull Up cut</p>	<ul style="list-style-type: none"> <li>• With pull-up resistor The value of pull-up resistor is switched by the input level of OE signal. 800 kΩ at OE="L" (Typ) 22 kΩ at OE="H" (Typ)</li> <li>• CMOS hysteresis input</li> </ul>
S0, S1, SPRD	 <p>Note : At OE="L" Pull Up cut</p>	<ul style="list-style-type: none"> <li>• With pull-up resistor 50 kΩ (Typ)</li> <li>• CMOS hysteresis input</li> <li>• Pull-up resistor is disconnected at OE="L", and internal signal is fixed to "L".</li> </ul>
MLTP	 <p>Note : At OE="L" Pull Down cut</p>	<ul style="list-style-type: none"> <li>• With pull-down resistor 50 kΩ (Typ)</li> <li>• CMOS hysteresis input</li> <li>• Pull-down resistor is disconnected at OE="L", and internal signal is fixed to "L".</li> </ul>
OUT	 <p>Note : At OE="L" Hi-Z output</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• <math>I_{OL} = 8.0 \text{ mA}</math></li> <li>• Hi-Z output at OE="L"</li> </ul>

(Continued)

# MB88161

(Continued)

Pin	Circuit type	Remarks
XIN, XOUT	 <p>The diagram shows the internal circuit for the XIN and XOUT pins. The XIN pin is connected to an input terminal through a 4 pF capacitor. The XOUT pin is connected to an output terminal through a 4 pF capacitor. A 500 kΩ resistor is connected between the XIN and XOUT nodes. A buffer circuit is connected to the XOUT node, consisting of an inverter followed by a buffer stage.</p>	<ul style="list-style-type: none"><li>• Oscillation circuit</li><li>• Built-in feedback resistance : 500 kΩ (Typ)</li><li>• Built-in oscillation stabilization capacitance : 4 pF (Typ)</li></ul>

## ■ HANDLING DEVICES

### Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply and GND. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

### Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

### Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

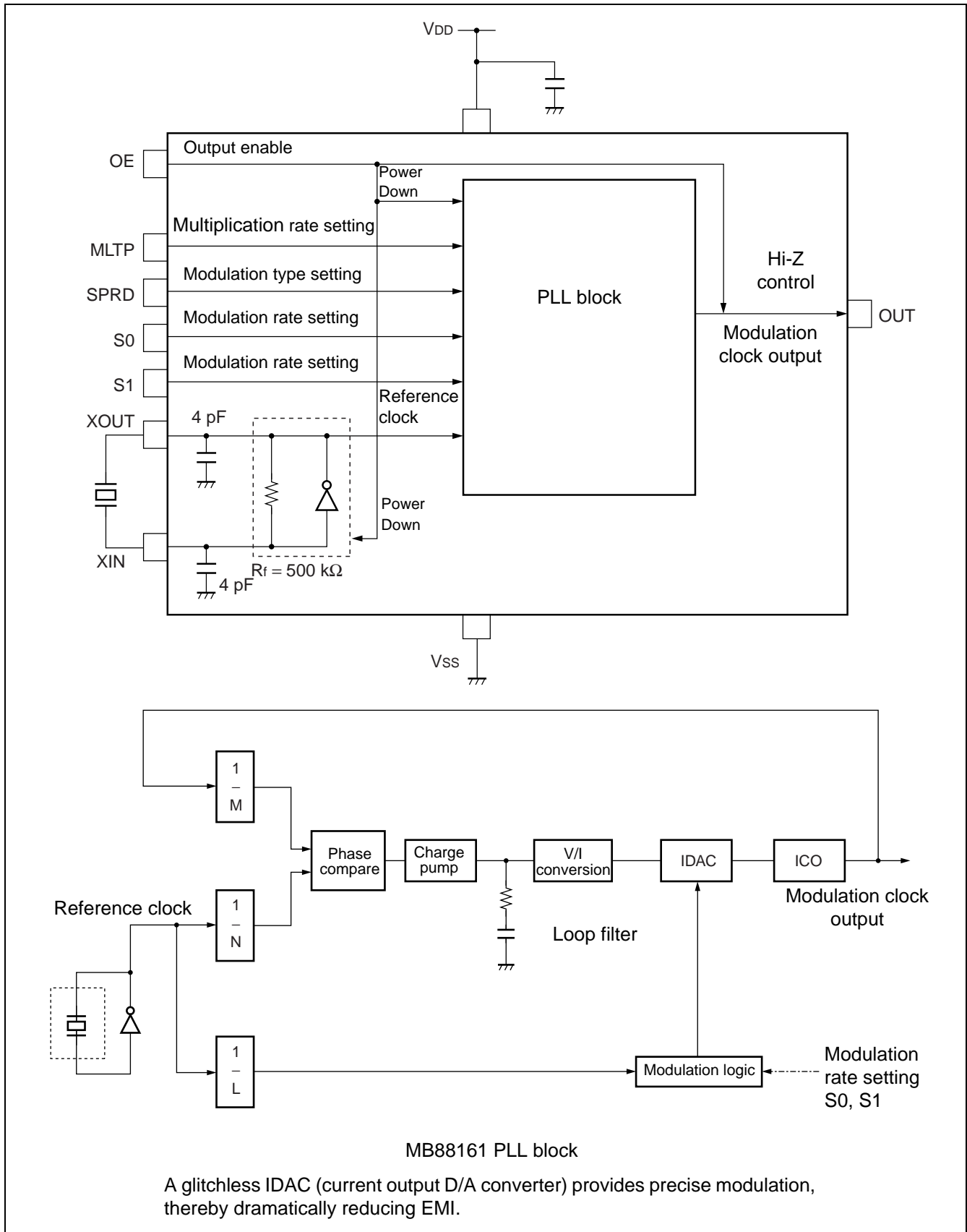
We recommend connecting electrolytic capacitor (about 10  $\mu\text{F}$ ) and the ceramic capacitor (about 0.01  $\mu\text{F}$ ) in parallel between power supply and GND near the device, as a bypass capacitor.

### Oscillation circuit

Noise near the XIN pin and XOUT pin may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN pin or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN pin and XOUT pin with ground.

## ■ BLOCK DIAGRAM



## ■ PIN SETTING

After the pin setting is changed, the stabilization wait time of the modulation clock is required. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time in “• AC Characteristics” in

### ■ ELECTRICAL CHARACTERISTICS.

Each setting pin contains the pull-up resistor or pull-down resistor. Therefore, these pins is set to default state for input opened.

### MLTP multiplication setting

MLTP	Multiplication rate	Input Frequency	Output Frequency	Remarks
L	Multiplied by 1	20 MHz to 28 MHz	20 MHz to 28 MHz	Default
H	Multiplied by 2	14 MHz to 40 MHz	28 MHz to 80 MHz	—

Note : Set MLTP pin to “L” for input opened because MLTP pin has the pull-down resistor.

### OE clock output enable

OE	Status	Remarks
L	Modulation clock output (OUT pin) Hi-Z/Power down status	—
H	Operation status	Default

Note : When OE pin is set to “L”, all oscillation circuits/PLL stop and enter power down mode, low-power consumption mode. Modulation clock output (OUT pin) becomes Hi-Z state during the power down. Set OE pin to “H” for input opened because OE pin has the pull-up resistor.

### SPRD modulation type setting

SPRD	Modulation type	Remarks
L	Down spread	—
H	Center spread	Default

Note : Set SPRD pin to “H” for input opened because SPRD pin has the pull-up resistor.

### S0/S1 modulation rate setting

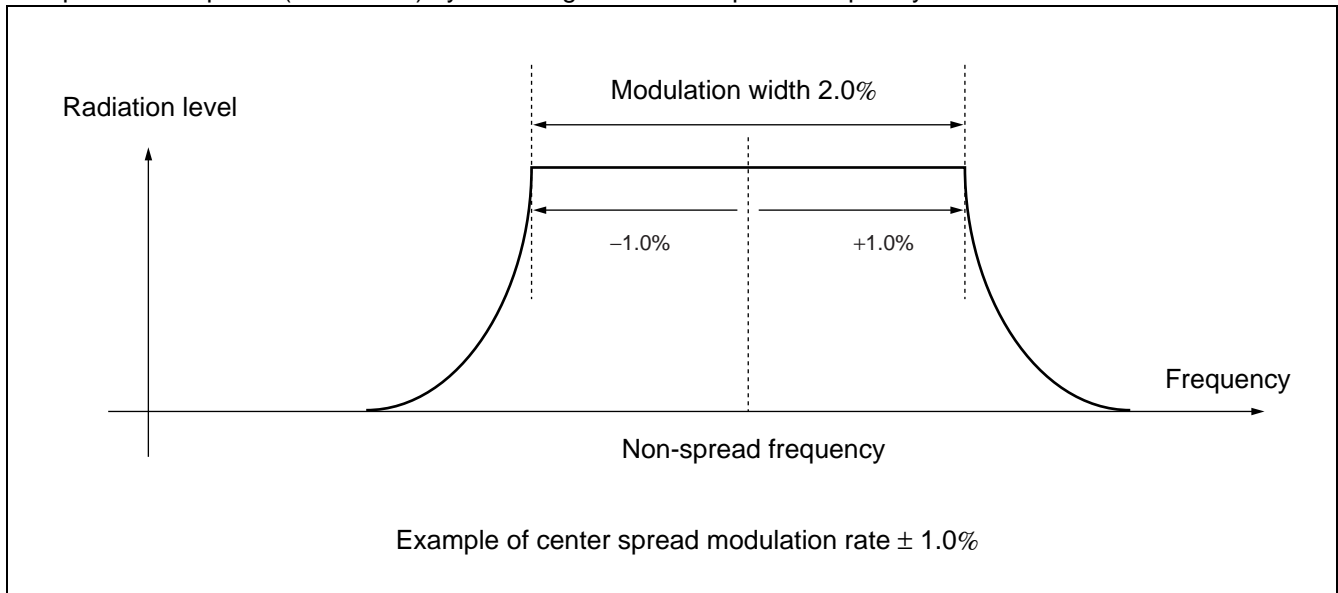
S1	S0	Modulation rate		Remarks
		At down spread	At center spread	
L	L	No modulation	No modulation	—
L	H	– 1.0%	± 0.5%	—
H	L	– 4.0%	± 2.0%	—
H	H	– 2.0%	± 1.0%	Default

Note : Set S1 pin and S0 pin to “H” for input opened because S1 pin and S0 pin have the pull-up resistor.

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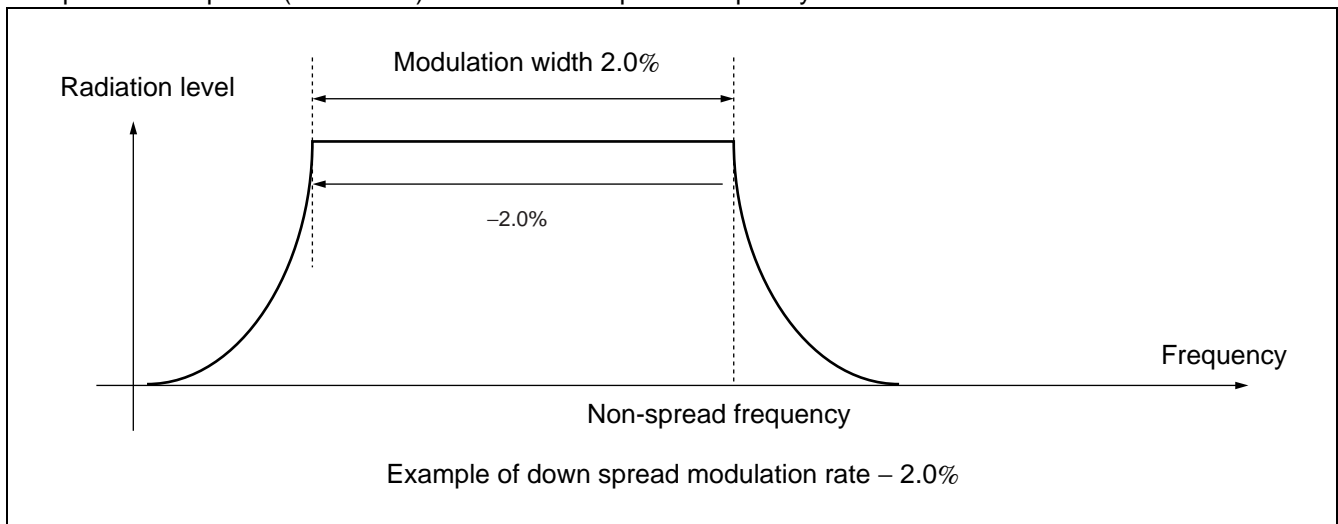
- Center spread

Spectrum is spread (modulated) by centering on the non-spread frequency.



- Down spread

Spectrum is spread (modulated) below the non-spread frequency.





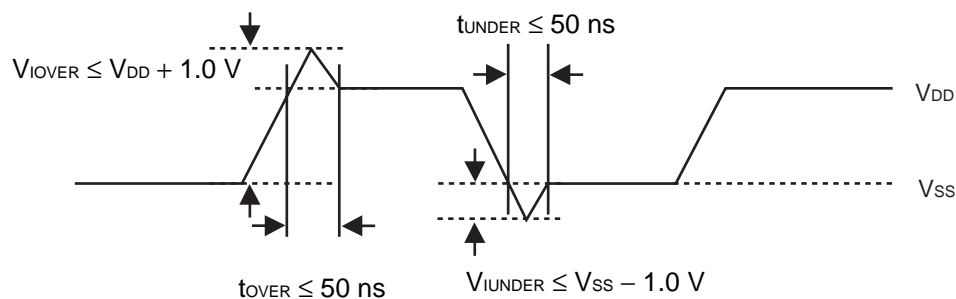
## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	$V_{DD}$	- 0.5	+ 4.0	V
Input voltage*	$V_I$	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Output voltage*	$V_O$	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Storage temperature	$T_{ST}$	- 55	+ 125	°C
Operation junction temperature	$T_J$	- 40	+ 125	°C
Output current	$I_O$	- 14	+ 14	mA
Overshoot	$V_{IOVER}$	—	$V_{DD} + 1.0$ ( $t_{OVER} \leq 50$ ns)	V
Undershoot	$V_{IUNDER}$	$V_{SS} - 1.0$ ( $t_{UNDER} \leq 50$ ns)	—	V

\* : The parameter is based on  $V_{SS} = 0.0$  V.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

### Overshoot/Undershoot



## RECOMMENDED OPERATING CONDITIONS

( $V_{SS} = 0.0\text{ V}$ )

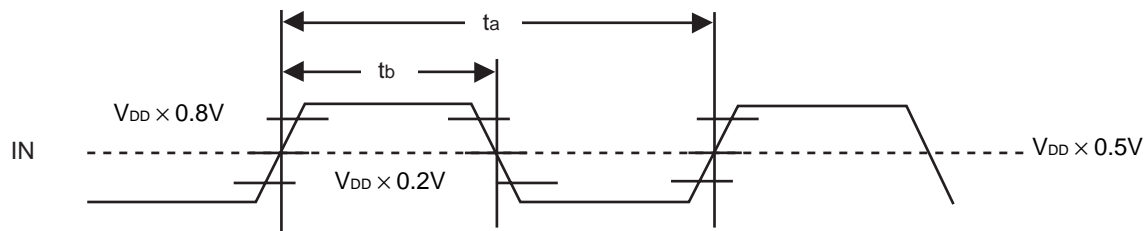
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	$V_{DD}$	$V_{DD}$	—	2.7	3.3	3.6	V
“H” level input voltage	$V_{IH}$	XIN, MLTP, OE, SPRD, S1, S0	—	$V_{DD} \times 0.80$	—	$V_{DD} + 0.3$	V
“L” level input voltage	$V_{IL}$		—	$V_{SS}$	—	$V_{DD} \times 0.20$	V
Input clock duty cycle	$t_{DCI}$	XIN	Input frequency 14 MHz to 40 MHz	40	50	60	%
Operating temperature	$T_a$	—	—	- 40	—	+ 85	°C

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Input clock duty cycle ( $t_{DCI} = t_b/t_a$ )



## ■ ELECTRICAL CHARACTERISTICS

### • DC Characteristics

( $T_a = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	$I_{CC}$	$V_{DD}$	24 MHz output no load capacitance	—	7.0	11.0	mA
Power down current	$I_{PD}$	$V_{DD}$	At power down (At OE="L")	—	5	20	$\mu\text{A}$
Output voltage	$V_{OH}$	OUT	"H" level output, $I_{OH} = -8\text{ mA}$	$0.8 \times V_{DD}$	—	$V_{DD}$	V
	$V_{OL}$		"L" level output, $I_{OL} = 8\text{ mA}$	$V_{SS}$	—	$0.2 \times V_{DD}$	V
Output impedance	$Z_{OC}$	OUT	20 MHz to 80 MHz	—	30	—	$\Omega$
Load capacitance	$C_L$	OUT	20 MHz to 80 MHz	—	—	15	pF
Built-in oscillation stabilization capacitance	$C_{OSC}$	XIN, XOUT	—	—	4	—	pF
Input pull-up resistance	$R_{PUOEH}$	OE	$V_{IH} = 0.8 \times V_{DD}$	10	25	100	$\text{k}\Omega$
	$R_{PUOEL}$	OE	$V_{IL} = 0.0\text{ V}$	500	800	1200	$\text{k}\Omega$
	$R_{PU}$	OE, SPRD, S1, S0	$V_{IL} = 0.0\text{ V}$	25	50	200	$\text{k}\Omega$
Input pull-down resistance	$R_{PD}$	MLTP	$V_{IH} = V_{DD}$	25	50	200	$\text{k}\Omega$

Note : When OE pin is set to "L", the pull-up resistor connected to SPRD pin, S1 pin, and S0 pin and the pull-down resistor connected to MLTP pin are disconnected, and internal signal is fixed to "L".  
See "■ I/O CIRCUIT TYPE" for details.

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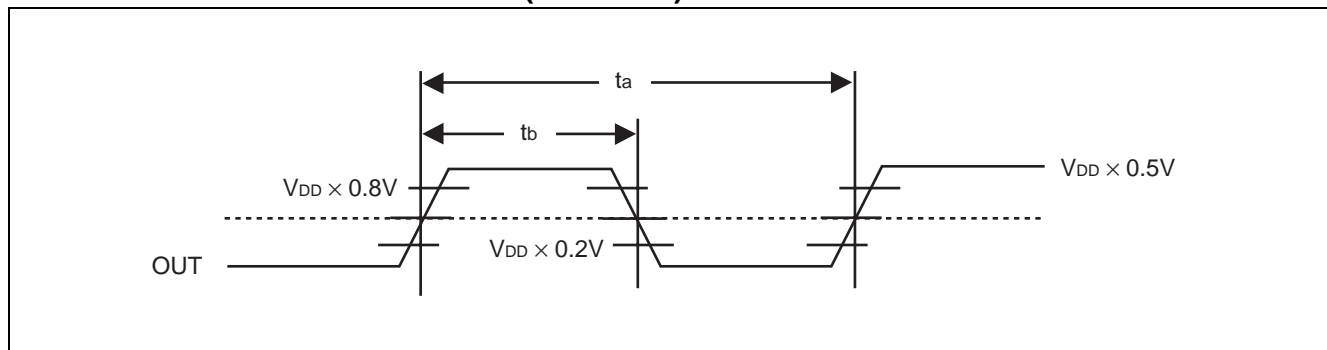
- AC Characteristics

(Ta = -40 °C to +85 °C, V<sub>DD</sub> = 2.7 V to 3.6 V, V<sub>SS</sub> = 0.0 V)

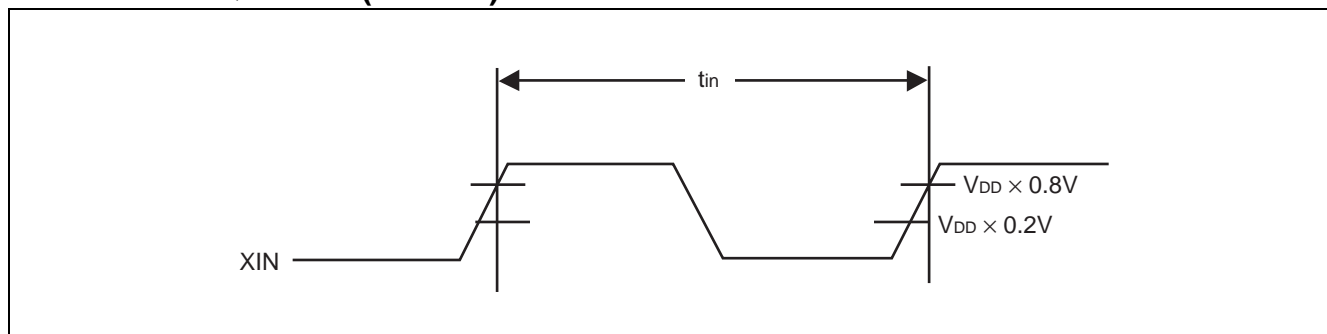
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f <sub>in</sub>	XIN	MLTP= "L" Crystal oscillation input	20	—	28	MHz
			MLTP= "H" Crystal oscillation input	14	—	40	
Crystal oscillation frequency	f <sub>x</sub>	XIN, XOUT	MLTP= "L" Fundamental oscillation	20	—	28	MHz
			MLTP= "H" Fundamental oscillation	14	—	40	
Output frequency	f <sub>OUT</sub>	OUT	MLTP= "L"	20	—	28	MHz
			MLTP= "H"	28	—	80	
Output clock rise time	t <sub>r</sub>	OUT	0.2 × V <sub>DD</sub> to 0.8 × V <sub>DD</sub> Load capacitance 15pF	0.4	—	4.0	ns
Output clock fall time	t <sub>f</sub>	OUT	0.2 × V <sub>DD</sub> to 0.8 × V <sub>DD</sub> Load capacitance 15 pF	0.4	—	4.0	ns
Output clock duty cycle	t <sub>DCC</sub>	OUT	0.5 × V <sub>DD</sub>	40	—	60	%
Modulation frequency	f <sub>MOD</sub>	OUT	Input frequency at 24MHz Multiplied by 1	—	32.0	—	kHz
			Input frequency at 24MHz Multiplied by 2	—	21.3	—	
Lock-Up time	t <sub>LK</sub>	OUT	—	—	4	10	ms
Cycle-Cycle jitter	t <sub>JC</sub>	OUT	Ta= +25°C, V <sub>DD</sub> =3.3V, No load capacitance, Standard deviation σ	—	—	100	ps
Output enable "L" width	t <sub>OELW</sub>	OE	—	1	—	—	μs
Power supply rise time	t <sub>VDR</sub>	V <sub>DD</sub>	0.0V to 2.7V	100	—	—	μs
Output Hi-Z start time after power down entry	t <sub>PEZ</sub>	OUT	Rise time or fall time of "OE" at 5 ns	—	—	10	ns
Output Hi-Z release time after power down exit	t <sub>PIZ</sub>	OUT	Rise time or fall time of "OE" at 5 ns	0	—	—	ns
Output start time after power down exit	t <sub>PIO</sub>	OUT	Rise time or fall time of "OE" at 5 ns Load capacitance 15 pF	—	—	10	ns

Note : The stabilization wait time of the modulation clock is required after the power is turned on or when the clock output enable setting (OE pin), multiplication setting (MLTP pin) or modulation rate setting (S1pin and S0 pin) is changed. The stabilization wait time of the modulation clock takes the maximum value of Lock-Up time.

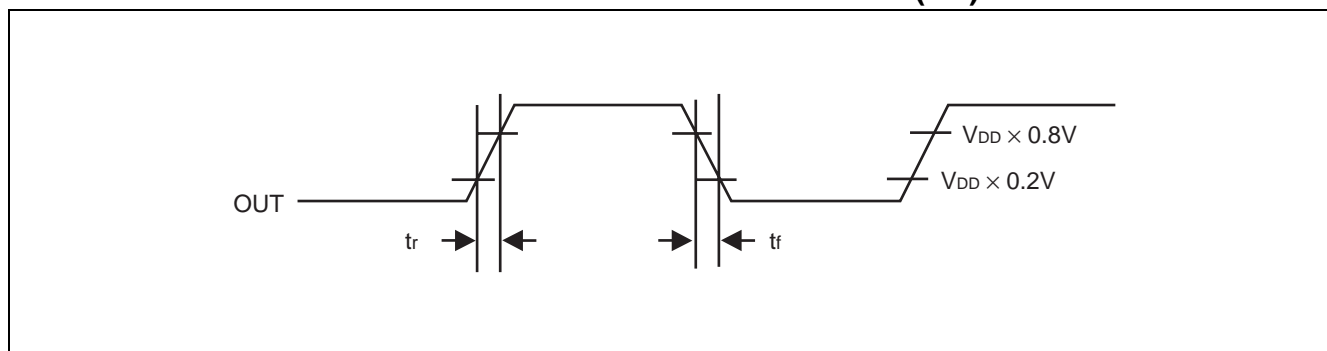
## ■ OUTPUT CLOCK DUTY CYCLE ( $t_{DCC} = t_b/t_a$ )



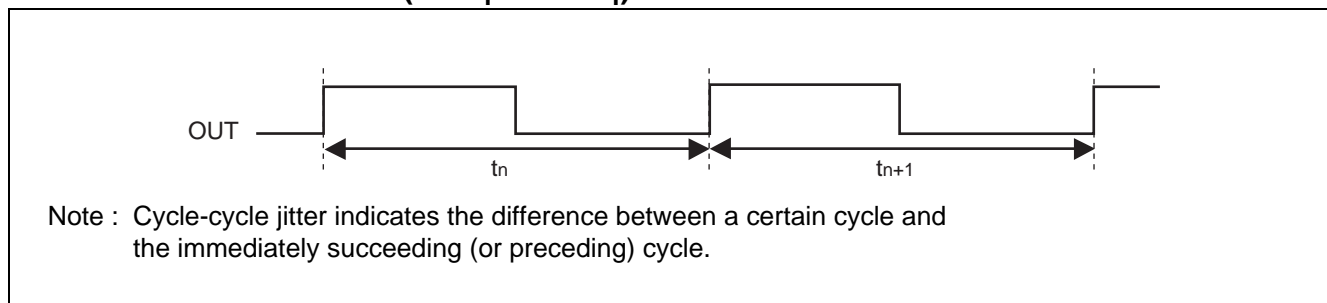
## ■ INPUT FREQUENCY ( $f_{in} = 1/t_{in}$ )



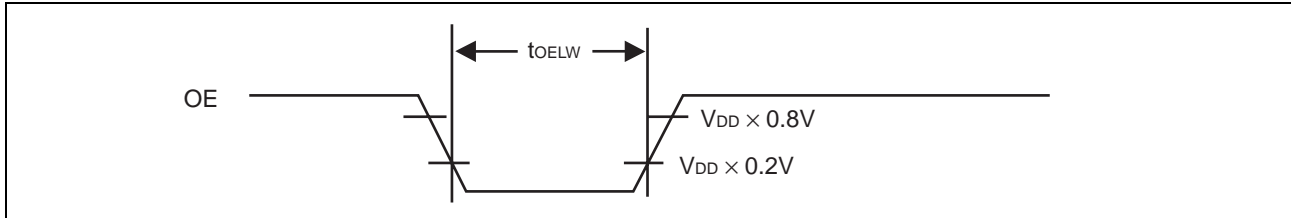
## ■ OUTPUT CLOCK RISE TIME/OUTPUT CLOCK FALL TIME ( $t_r/t_f$ )



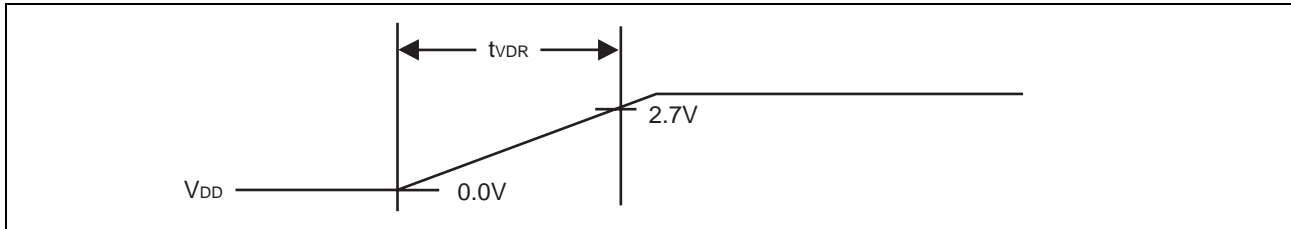
## ■ CYCLE-CYCLE JITTER ( $t_{JC} = |t_n - t_{n+1}|$ )



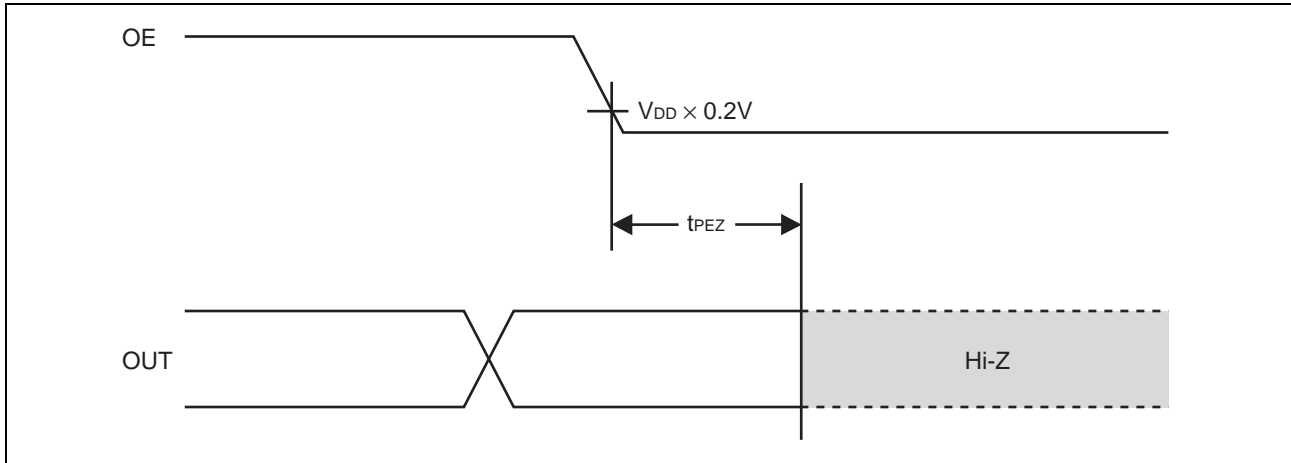
## ■ OUTPUT ENABLE "L" WIDTH ( $t_{OELW}$ )



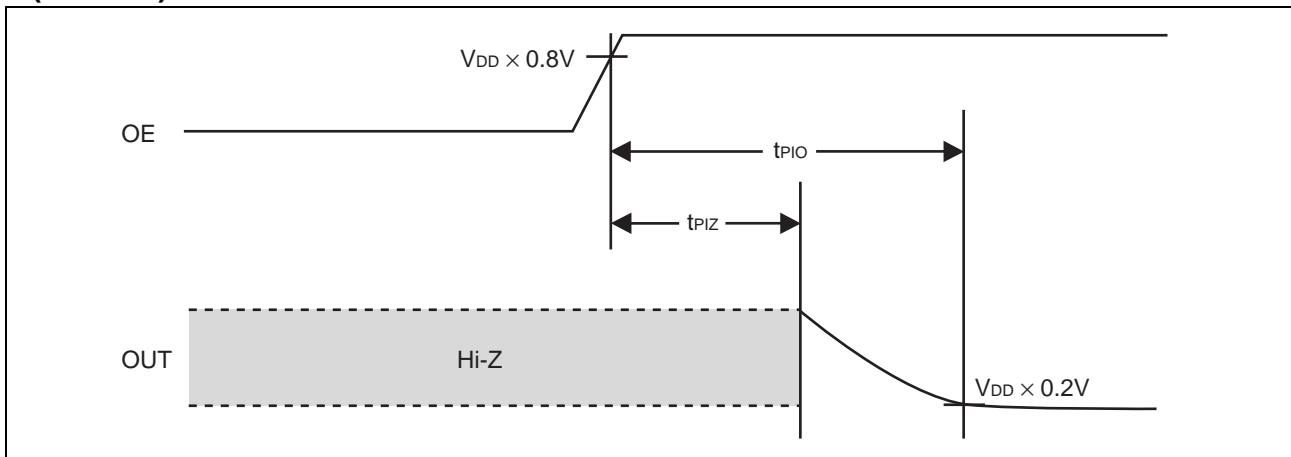
## ■ POWER SUPPLY RISE TIME ( $t_{VDR}$ )



## ■ OUTPUT Hi-Z START TIME AFTER POWER DOWN ENTRY ( $t_{PEZ}$ )

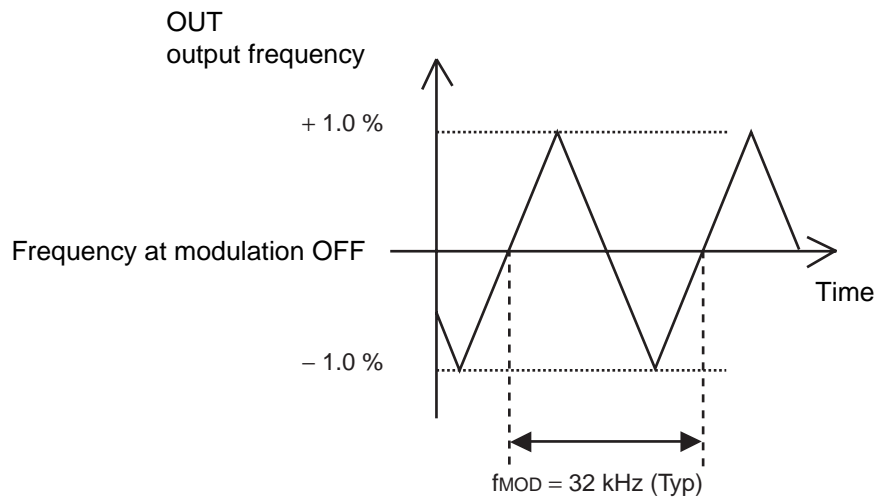


## ■ OUTPUT Hi-Z RELEASE TIME • OUTPUT START TIME AFTER POWER DOWN EXIT ( $t_{PIZ} \bullet t_{PIO}$ )

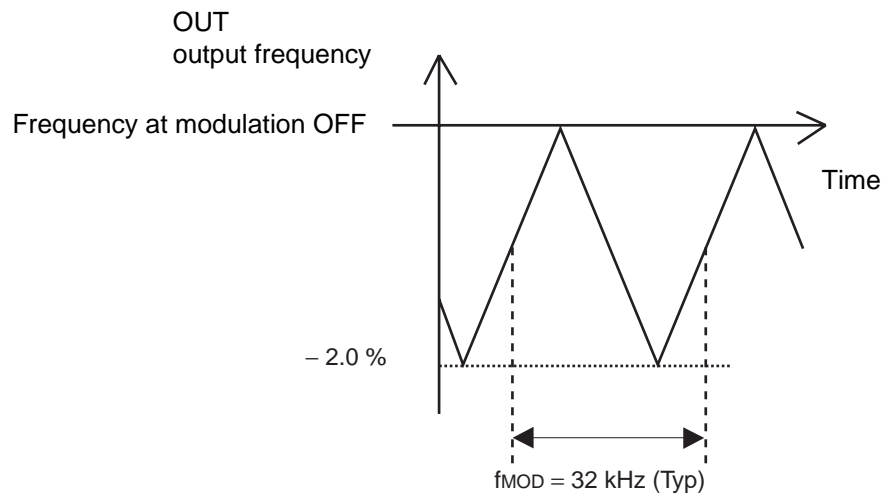


## ■ MODULATION WAVEFORM

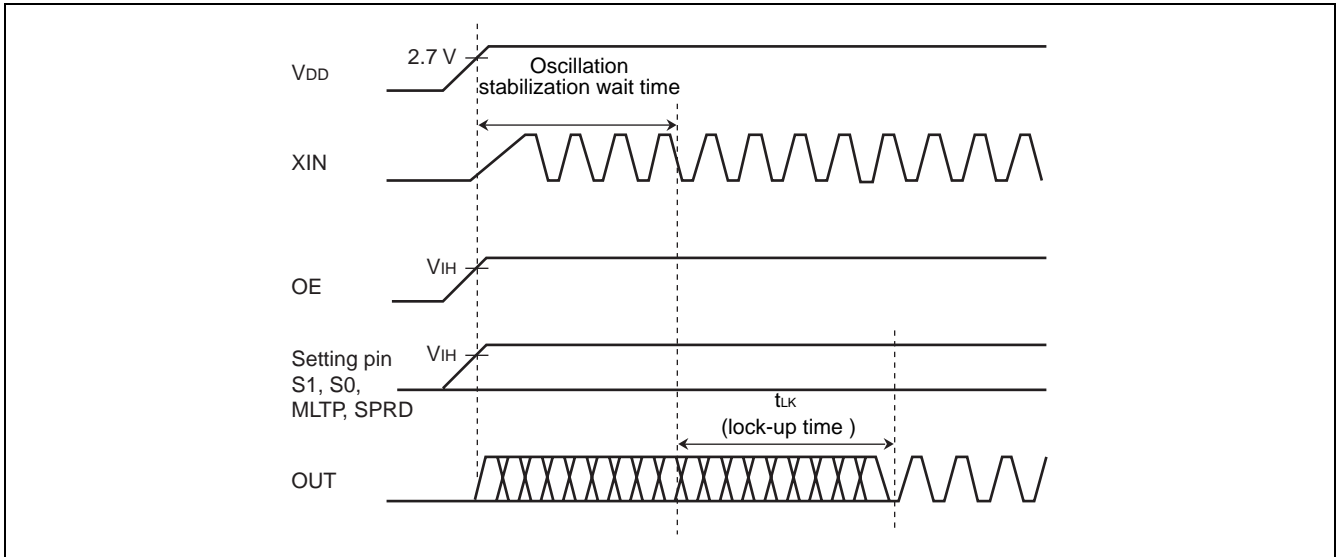
- Modulation rate  $\pm 1.0\%$ , example of center spread



- Modulation rate  $-2.0\%$ , example of down spread



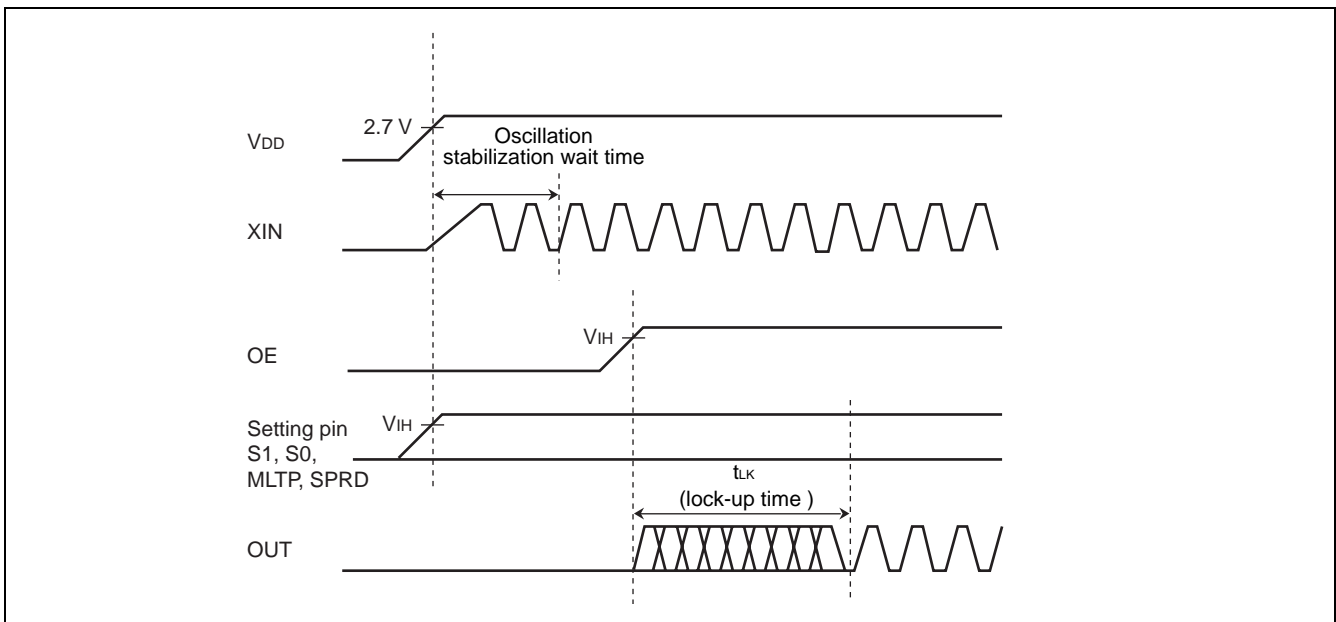
## LOCK-UP TIME



The clock stabilization wait time is required when the power is turned on.

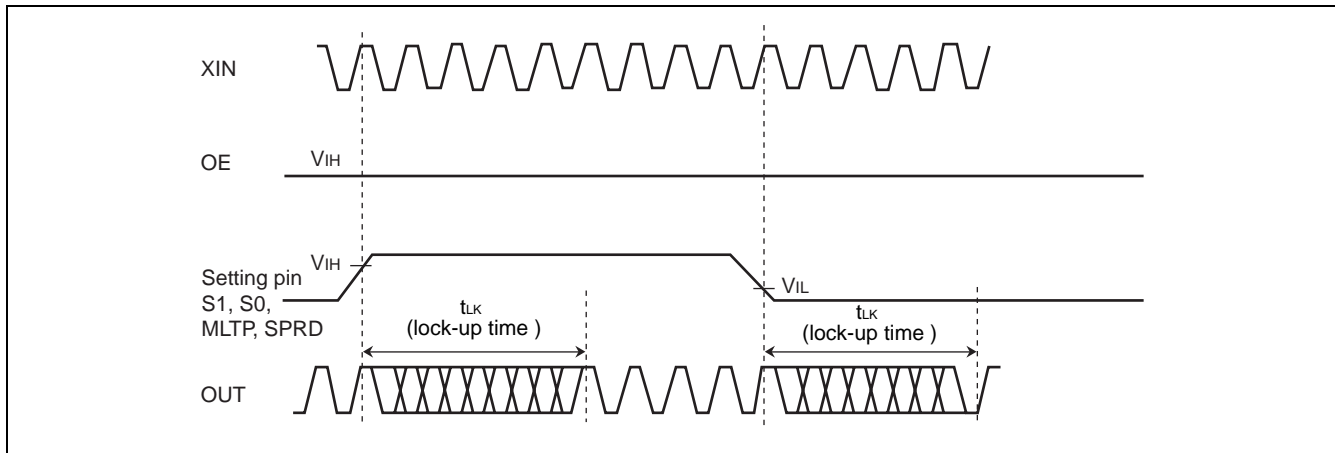
If the OE pin is fixed at "H" level, the maximum time after the power is turned on until the required clock is obtained is (the stabilization wait time of input clock to XIN pin) + (the lock-up time "t<sub>LK</sub>").

For the stabilization wait time of input clock to the XIN pin, check the characteristics of the resonator or oscillator used.



If the OE pin is used for power down control, the required clock is obtained at most the lock-up time "t<sub>LK</sub>" after the OE pin goes "H" level.





If the setting pin (S1, S0, MLTP, or SPRD) is used for control during normal operation, the required clock is obtained at most the lock-up time " $t_{LK}$ " after the level at the pin is determined.

Note : The wait time for the clock signal output from the OUT pin to become stable is required after the IC is released from power-down mode by the OE pin or after another pin's setting is changed. During the period until the output clock signal becomes stable, the output frequency, output clock duty cycle, modulation period, and Cycle-Cycle jitter characteristic cannot be guaranteed. It is therefore advisable to perform processing such as cancelling a reset of the device at the succeeding stage after the lock-up time.



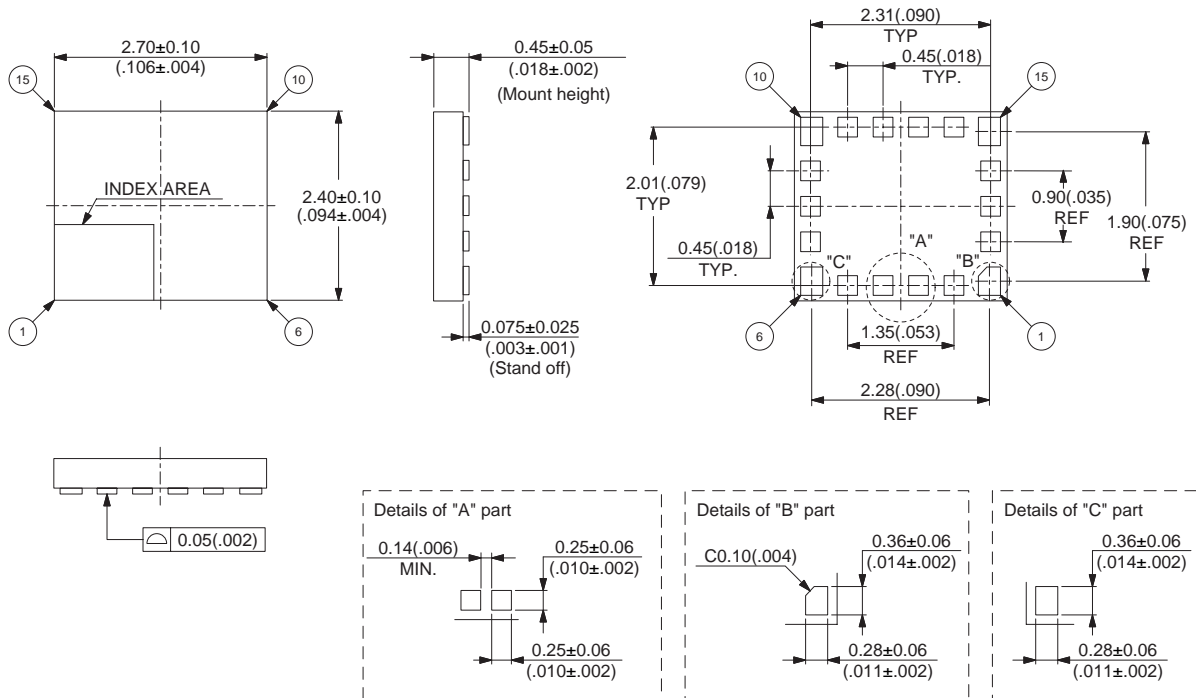
## ■ ORDERING INFORMATION

Part no.	Package	Emboss taping
MB88161PVB-G-EFE1	18-pin plastic BCC (LCC-18P-M05)	EF type
MB88161PVB-G-ERE1		ER type

# MB88161

## PACKAGE DIMENSION

18-pin plastic BCC  
(LCC-18P-M05)



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Dimensions in mm (inches)

Note: The values in parentheses are reference values.

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