



## 2913 AND 2914 COMBINED SINGLE-CHIP PCM CODEC AND FILTER

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| <ul style="list-style-type: none"> <li>■ 2913 Synchronous Clocks Only, 300 Mill Package</li> <li>■ 2914 Asynchronous Clocks, 8th Bit Signaling, Loop Back Test Capability</li> <li>■ AT&amp;T D3/D4 and CCITT Compatible for Synchronous Operation</li> <li>■ Pin Selectable <math>\mu</math>-Law or A-Law Operation</li> <li>■ Two Timing Modes:             <ul style="list-style-type: none"> <li>— Fixed Data Rate Mode<br/>1.536, 1.544, or 2.048 MHz</li> <li>— Variable Data Rate Mode<br/>64 KHz 2.048 MHz</li> </ul> </li> </ul> | <ul style="list-style-type: none"> <li>■ Exceptional Analog Performance</li> <li>■ 28-Pin Plastic Leaded Chip Carrier (PLCC) for Higher Integration</li> <li>■ Low Power HMOS-E Technology:             <ul style="list-style-type: none"> <li>— 5 mW Typical Power Down</li> <li>— 140 mW Typical Operating</li> </ul> </li> <li>■ Fully Differential Architecture Enhances Noise Immunity</li> <li>■ On-Chip Auto Zero, Sample and Hold, and Precision Voltage References</li> <li>■ Direct Interface with Transformer or Electronic Hybrids</li> </ul> |
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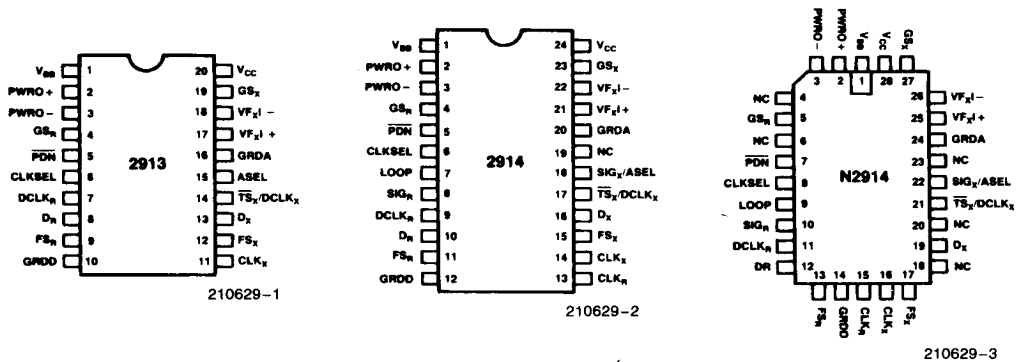
The Intel 2913 and 2914 are fully integrated PCM codecs with transmit/receive filters fabricated in a highly reliable and proven N-channel HMOS silicon gate technology (HMOS-E). These devices provide the functions that were formerly provided by two complex chips (2910A or 2911A and 2912A). Besides the higher level of integration, the performance of the 2913 and 2914 is superior to that of the separate devices.

The primary applications for the 2913 and 2914 are in telephone systems:

- Switching—Digital PBX's and Central Office Switching Systems
- Transmission—D3/D4 Type Channel Banks and Subscriber Carrier Systems
- Subscriber Instruments—Digital Handsets and Office Workstations

The wide dynamic range of the 2913 and 2914 (78 dB) and the minimal conversion time make them ideal products for other applications such as:

- |                                                                                                                |                                                                                                                       |
|----------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Voice Store and Forward</li> <li>• Digital Echo Cancellers</li> </ul> | <ul style="list-style-type: none"> <li>• Secure Communications Systems</li> <li>• Satellite Earth Stations</li> </ul> |
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**Figure 1. Pin Configurations**

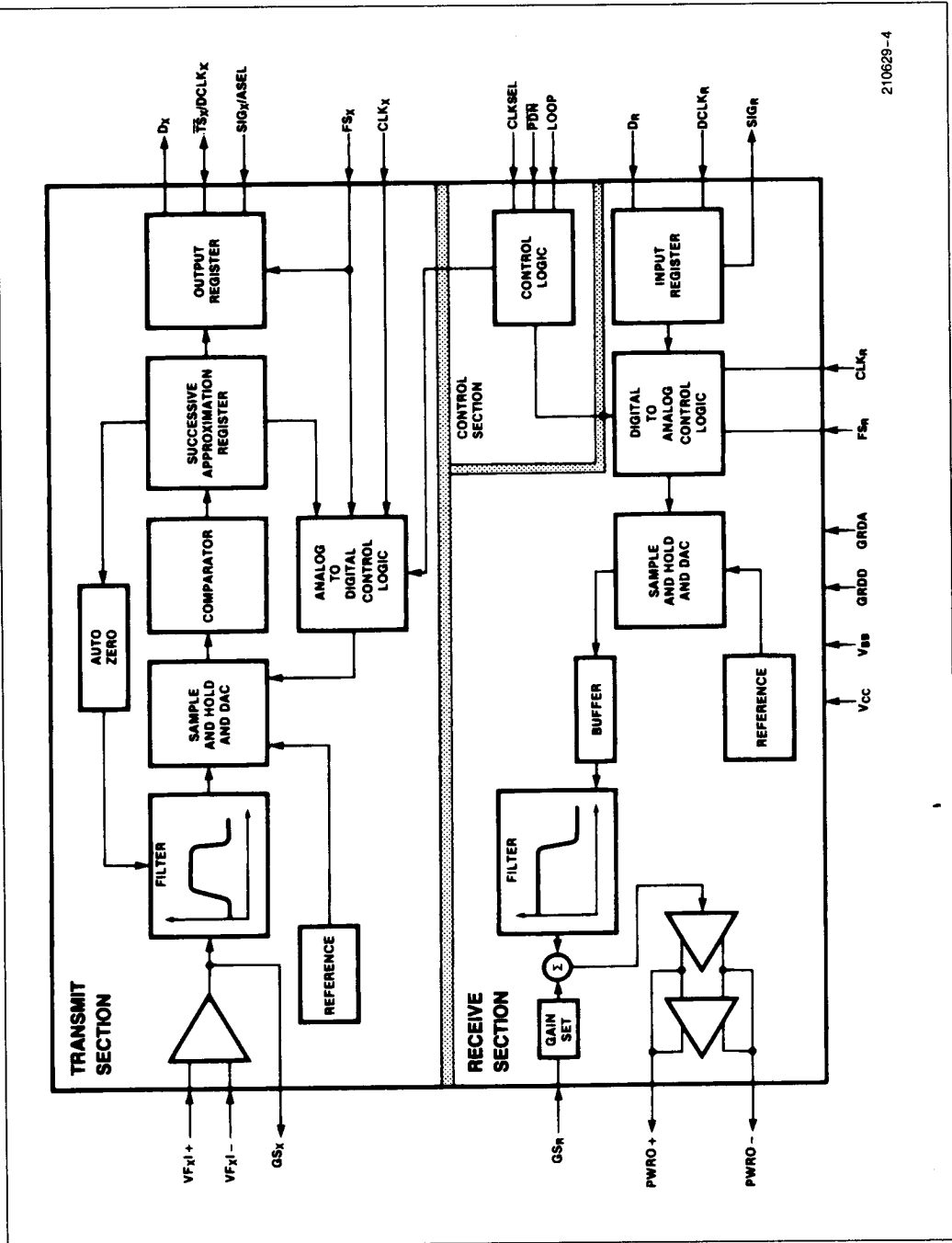


Figure 2. Block Diagram

Table 1. Pin Names

Name	Description	Name	Description
V <sub>BB</sub>	Power (-5V)	GS <sub>X</sub>	Transmit Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VF <sub>XI-</sub> , VF <sub>XI+</sub>	Analog Inputs
GS <sub>R</sub>	Receive Gain Control	GRDA	Analog Ground
PDN	Power Down Select	NC	No Connect
CLKSEL	Master Clock Frequency Select	SIG <sub>X</sub>	Transmit Signaling Input
LOOP	Analog Loop Back	ASEL	μ- or A-Law Select
SIG <sub>R</sub>	Receive Signaling Output	TS <sub>X</sub>	Timeslot Strobe/Buffer Enable
DCLK <sub>R</sub>	Receive Variable Data Clock	DCLK <sub>X</sub>	Transmit Variable Data Clock
D <sub>R</sub>	Receive PCM Input	D <sub>X</sub>	Transmit PCM Output
FS <sub>R</sub>	Receive Frame Synchronization Clock	FS <sub>X</sub>	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK <sub>X</sub>	Transmit Master Clock
V <sub>CC</sub>	Power (+5V)	CLK <sub>R</sub>	Receive Master Clock (2914 Only, Internally Connected to CLK <sub>X</sub> on 2913)

Table 2. Pin Description

Symbol	Function
V <sub>BB</sub>	Most negative supply; input voltage is -5V ± 5%.
PWRO+	Non-inverting output of power amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO-	Inverting output of power amplifier. Functionally identical and complementary to PWRO+.
GS <sub>R</sub>	Input to the gain setting network on the output power amplifier. Transmission level can be adjusted over a 12 dB range depending on the voltage at GS <sub>R</sub> .
PDN	Power down select. When PDN is TTL high, the device is active. When low, the device is powered down.
CLKSEL	Input which must be pinstrapped to reflect the master clock frequency at CLK <sub>X</sub> , CLK <sub>R</sub> . CLKSEL = V <sub>BB</sub> ..... 2.048 MHz CLKSEL = GRDD ..... 1.544 MHz CLKSEL = V <sub>CC</sub> ..... 1.536 MHz
LOOP	Analog loopback. When this pin is TTL high, the analog output (PWRO+) is internally connected to the analog input (VF <sub>XI+</sub> ). GS <sub>R</sub> is internally connected to PWRO-, and VF <sub>XI-</sub> is internally connected to GS <sub>X</sub> . A 0 dBm0 digital signal input at D <sub>R</sub> is returned as a +3 dBm0 digital signal output at D <sub>X</sub> .
SIG <sub>R</sub>	Signaling bit output, receive channel. In fixed data rate mode, SIG <sub>R</sub> outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
DCLK <sub>R</sub>	Selects the fixed or variable data rate mode. When DCLK <sub>R</sub> is connected to V <sub>BB</sub> , the fixed data rate mode is selected. When DCLK <sub>R</sub> is not connected to V <sub>BB</sub> , the device operates in the variable data rate mode. In this mode DCLK <sub>R</sub> becomes the receive data clock which operates at TTL levels from 64 Kb to 2.048 Mb data rates.

Table 2. Pin Description (Continued)

Symbol	Function
D <sub>R</sub>	Receive PCM input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock; CLK <sub>R</sub> in the fixed data rate mode and DCLK <sub>R</sub> in variable data rate mode.
FS <sub>R</sub>	8 KHz frame synchronization clock input/timeslot enable, receive channel. A multi-function input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FS <sub>R</sub> is TTL low for 300 milliseconds.
GRDD	Digital ground for all internal logic circuits. Not internally tied to GRDA.
CLK <sub>R</sub>	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK <sub>X</sub>	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS <sub>X</sub>	8 KHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FS <sub>R</sub> . The transmit channel enters the standby state whenever FS <sub>X</sub> is TTL low for 300 milliseconds.
D <sub>X</sub>	Transmit PCM output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock: CLK <sub>X</sub> in fixed data rate mode and DCLK <sub>X</sub> in variable data rate mode.
$\overline{\text{TS}}_X/\text{DCLK}_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin is an open drain output designed to be used as an enable signal for a three-state buffer. In variable data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64 Kb to 2.048 Mb data rates.
SIG <sub>X</sub> /ASEL	A dual purpose pin. When connected to V <sub>BB</sub> , A-law operation is selected. When it is not connected to V <sub>BB</sub> this pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D <sub>X</sub> lead. If not used as an input pin, ASEL should be strapped to either V <sub>CC</sub> or GRDD.
NC	No connect.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF <sub>XI</sub> +	Non-inverting analog input to uncommitted transmit operational amplifier.
VF <sub>XI</sub> -	Inverting analog input to uncommitted transmit operational amplifier.
GS <sub>X</sub>	Output terminal of transmit channel input op amp. Internally, this is the voice signal input to the transmit filter.
V <sub>CC</sub>	Most positive supply; input voltage is +5V ± 5%.

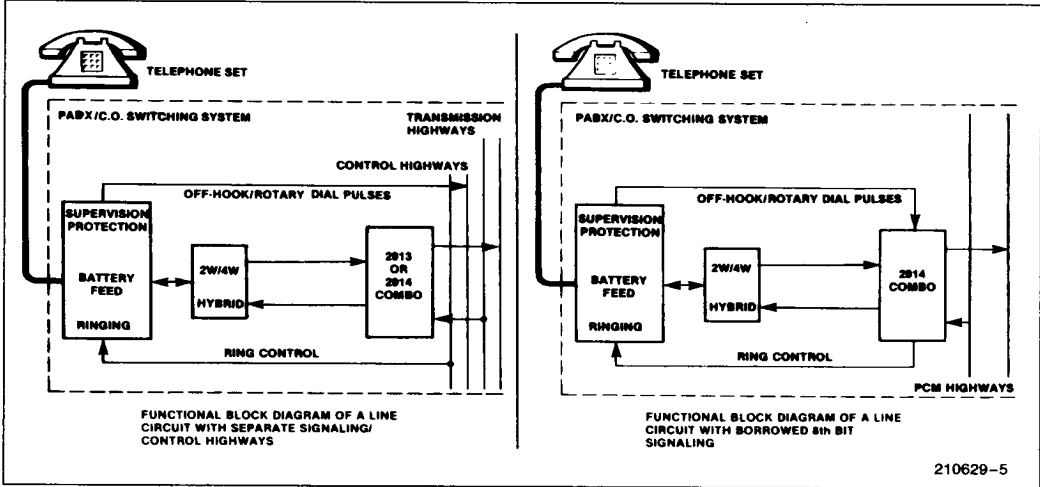
### FUNCTIONAL DESCRIPTION

The 2913 and 2914 provide the analog-to-digital and the digital-to-analog conversions and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system. They are intended to be used at the analog termination of a PCM line or trunk.

The following major functions are provided:

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

### SWITCHING



### CHANNEL BANKS

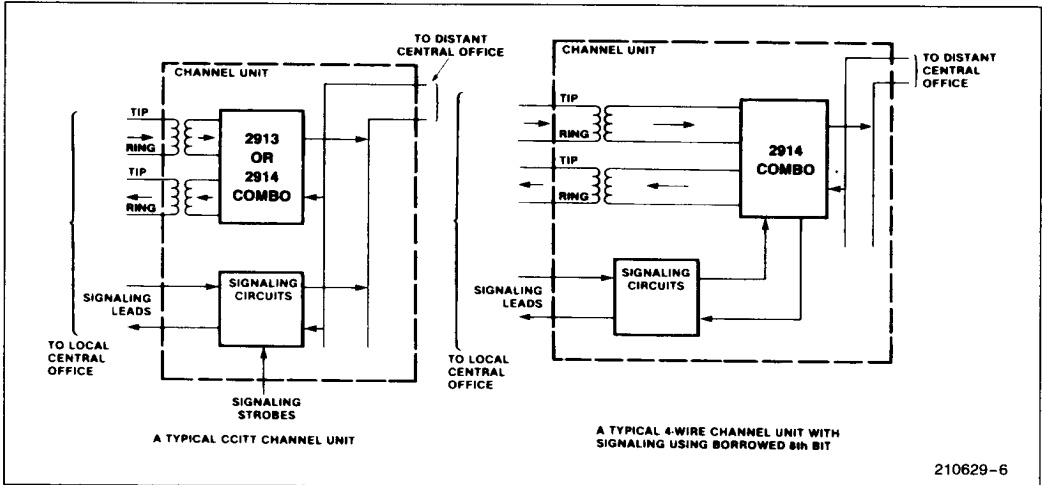


Figure 3. Typical Line Terminations

## GENERAL OPERATION

### System Reliability Features

The combochip can be powered up by pulsing  $FS_X$  and/or  $FS_R$  while a TTL high voltage is applied to  $\overline{PDN}$ , provided that all clocks and supplies are connected. The 2913 and 2914 have internal resets on power up (or when  $V_{BB}$  or  $V_{CC}$  are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs  $D_X$  and  $\overline{TS}_X$  are held in a high impedance state for approximately four frames (500  $\mu s$ ) after power up or application of  $V_{BB}$  or  $V_{CC}$ . After this delay,  $D_X$ ,  $\overline{TS}_X$ , and signaling will be functional and will occur in the proper time-slot. The analog circuits on the transmit side require approximately 60 milliseconds to reach their equilibrium value due to the autozero circuit settling time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output  $SIG_R$  is also held low for a maximum of four frames after power up or application of  $V_{BB}$  or  $V_{CC}$ .  $SIG_R$  will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability,  $\overline{TS}_X$  and  $D_X$  will be placed in a high impedance state approximately 30  $\mu s$  after an interruption of  $CLK_X$ . Similarly,  $SIG_R$  will be held low approximately 30  $\mu s$  after an interruption of  $CLK_R$ . These interruptions could possibly occur with some kind of fault condition.

## Power Down and Standby Modes

To minimize power consumption, two power down modes are provided in which most 2913/2914 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in Table 3, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the  $\overline{PDN}$  pin. In this mode, power consumption is reduced to the value shown in Table 3. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the  $\overline{PDN}$  pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire device down by selectively removing  $FS_X$  and/or  $FS_R$ . With both channels in the standby state, power consumption is reduced to the value shown in Table 3. If transmit only operation is desired,  $FS_X$  should be applied to the device while  $FS_R$  is held low. Similarly, if receive only operation is desired,  $FS_R$  should be applied while  $FS_X$  is held low.

## Fixed Data Rate Mode

Fixed data rate timing, which is 2910A and 2911A compatible, is selected by connecting  $DCLK_R$  to  $V_{BB}$ . It employs master clocks  $CLK_X$  and  $CLK_R$ , frame synchronization clocks  $FS_X$  and  $FS_R$ , and output  $\overline{TS}_X$ .

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Table 3. Power-Down Methods

Device Status	Power-Down Method	Typical Power Consumption	Digital Output Status
Power Down Mode	$\overline{PDN} = \text{TTL Low}$	5 mW	$\overline{TS}_X$ and $D_X$ are placed in a high impedance state and $SIG_R$ is placed in a TTL low state within 10 $\mu s$ .
Standby Mode	$FS_X$ and $FS_R$ are TTL Low	12 mW	$\overline{TS}_X$ and $D_X$ are placed in a high impedance state and $SIG_R$ is placed in a TTL low state 300 milliseconds after $FS_X$ and $FS_R$ are removed.
Only Transmit Is on Standby	$FS_X$ is TTL Low	70 mW	$\overline{TS}_X$ and $D_X$ are placed in a high impedance state within 300 milliseconds.
Only Receive Is on Standby	$FS_R$ is TTL Low	110 mW	$SIG_R$ is placed in a TTL low state within 300 milliseconds.

CLK<sub>X</sub> and CLK<sub>R</sub> serve both as master clocks to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS<sub>X</sub> and FS<sub>R</sub> are 8 KHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by their pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables the signaling function. TS<sub>X</sub> is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D<sub>X</sub> on the first eight positive transitions of CLK<sub>X</sub> following the rising edge of FS<sub>X</sub>. Similarly, on the receive side, data is received on the first eight falling edges of CLK<sub>R</sub>. The frequency of CLK<sub>X</sub> and CLK<sub>R</sub> is selected by the CLKSEL pin to be either 1.536, 1.544, or 2.048 MHz. No other frequency of operation is allowed in the fixed data rate mode.

### Variable Data Rate Mode

Variable data rate timing is selected by connecting DCLK<sub>R</sub> to the bit clock for the receive PCM highway rather than to V<sub>BB</sub>. It employs master clocks CLK<sub>X</sub> and CLK<sub>R</sub>, bit clocks DCLK<sub>R</sub> and DCLK<sub>X</sub>, and frame synchronization clocks FS<sub>R</sub> and FS<sub>X</sub>.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, which can be asynchronous in the case of the 2914 or synchronous in the case of the 2913, from 64 KHz to 2.048 MHz. Master clock's inputs are still restricted to 1.536, 1.544, or 2.048 MHz.

In this mode, DCLK<sub>R</sub> and DCLK<sub>X</sub> become the data clocks for the receive and transmit PCM highways. While FS<sub>X</sub> is high, PCM data from D<sub>X</sub> is transmitted onto the highway on the next eight consecutive positive transitions of DCLK<sub>X</sub>. Similarly, while FS<sub>R</sub> is high, each PCM bit from the highway is received by D<sub>R</sub> on the next eight consecutive negative transitions of DCLK<sub>R</sub>.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125 μs frame as long as DCLK<sub>X</sub> is pulsed and FS<sub>X</sub> is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

### Signaling

Signaling can only be performed with the 24-pin device in the fixed data rate timing mode (DCLK<sub>R</sub> = V<sub>BB</sub>). Signaling frames on the transmit and receive sides are independent of one another and are selected by a double-width frame sync pulse on the appropriate channel. During a transmit signaling frame, the codec will encode the incoming analog signal and substitute the signal present on SIG<sub>X</sub> for the least significant bit of the encoded PCM word. Similarly, in a receive signaling frame, the codec will decode the seven most significant bits according to CCITT recommendation G.733 and output the logical state of the LSB on the SIG<sub>R</sub> lead until it is updated in the next signaling frame. Timing relationships for signaling operation are shown in Figure 4.

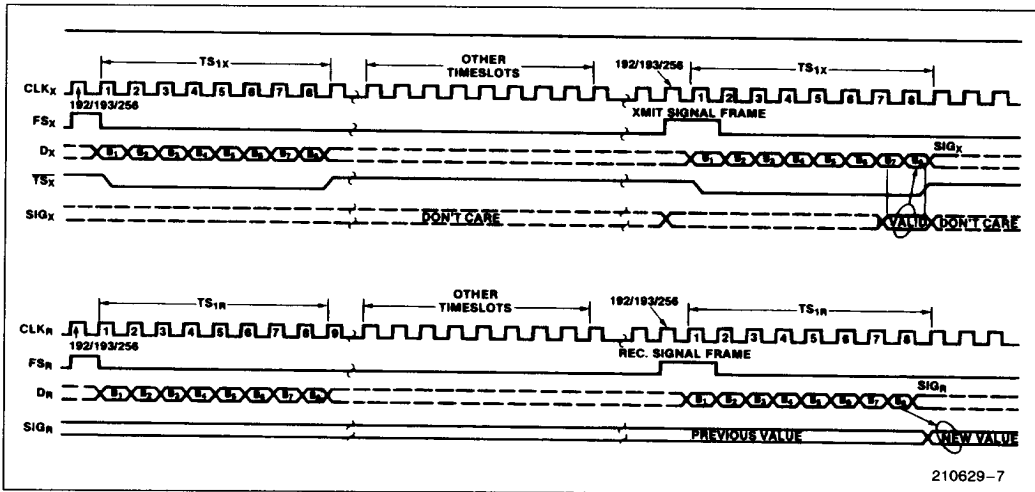


Figure 4. Signaling Timing (Used Only with Fixed Data Rate Mode)

### Asynchronous Operation

The 2914 can be operated with asynchronous clocks in either the fixed or variable data rate modes. In order to avoid crosstalk problems associated with special interrupt circuitry, the design of the Intel 2913/2914 combochip includes separate digital-to-analog converters and voltage references on the transmit and receive sides to allow independent operation of the two channels.

In either timing mode, the master clock, data clock, and timeslot strobe must be synchronized at the beginning of each frame.  $CLK_X$  and  $DCLK_X$  are synchronized once per frame but may be of different frequencies. The receive channel operates in a similar manner and is completely independent of the transmit timing (refer to Variable Data Rate Timing Diagrams). This approach requires the provision of two separate master clocks, even in variable data rate mode, but avoids the use of a synchronizer which can cause intermittent data conversion errors.

### Analog Loopback

A distinctive feature of the 2914 is its analog loopback capability. This feature allows the user to send a control signal which internally connects the analog input and output ports. As shown in Figure 5, when LOOP is TTL high the analog output ( $PWRO+$ ) is internally connected to the analog input ( $VF_X|+$ ),  $GS_R$  is internally connected to  $PWRO-$ , and  $VF_X|-$  is internally connected to  $GS_X$ .

With this feature, the user can test the line circuit remotely by comparing the digital codes sent into the receive channel ( $D_R$ ) with those generated on the transmit channel ( $D_X$ ). Due to the difference in transmission levels between the transmit and receive sides, a 0 dBm0 code sent into  $D_R$  will

emerge from  $D_X$  as a +3 dBm0 code, an implicit gain of 3 dB. Thus, the maximum signal input level which can be tested using analog loopback is 0 dBm0.

### Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique uses a difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections and each is trimmed independently during the manufacturing process. The reference value is then further trimmed in the gain setting op-amps to a final precision value. With this method the combochip can achieve the extremely accurate Digital Milliwatt Responses specified in the transmission parameters, providing the user a significant margin for error in other board components.

### Conversion Laws

The 2913 and 2914 are designed to operate in both  $\mu$ -law and A-law systems. The user can select either conversion law according to the voltage present on the  $SIG_X/ASEL$  pin. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for  $\mu$ -law and A-law conversion. If A-law operation is desired,  $SIG_X$  should be tied to  $V_{BB}$ . Thus, signaling is not allowed during A-law operation. If  $\mu = 255$ -law operation is selected, then  $SIG_X$  is a TTL level input which modifies the LSB of the PCM output in signaling frames.

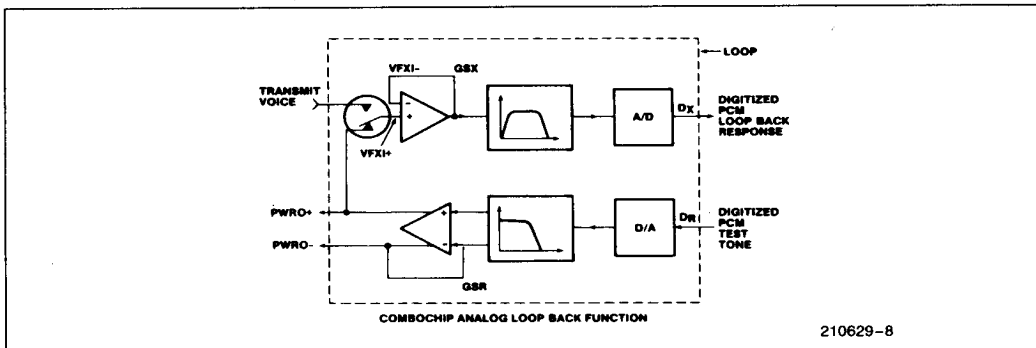


Figure 5. Simplified Block Diagram of 2914 Combochip in the Analog Loopback Configuration



## TRANSMIT OPERATION

### Transmit Filter

The input section provides gain adjustment in the passband by means of an on-chip operational amplifier. This operational amplifier has a common mode range of  $\pm 2.17$  volts, a DC offset of 25 mV, an open loop voltage gain of 5000, and a unity gain bandwidth of typically 1 MHz. Gain of up to 20 dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output ( $GS_X$ ) must be greater than 10 K $\Omega$  in parallel with less than 50 pF. The input signal on lead  $VF_{X1+}$  can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see Figure 6).

A low pass anti-aliasing section is included on-chip. This section typically provides 35 dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.714. The 2913 and 2914 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 8.

A high pass section configuration was chosen to reject low frequency noise from 50 Hz and 60 Hz power lines, 17 Hz European electric railroads, ringing

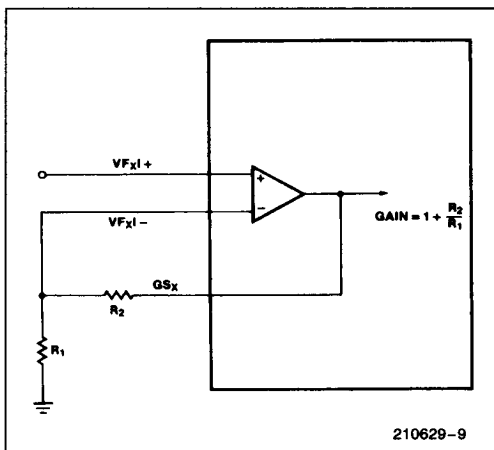


Figure 6. Transmit Filter Gain Adjustment

frequencies and their harmonics, and other low frequency noise. Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200 Hz. This feature allows the use of low-cost transformer hybrids without external components.

### Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique; the sign bit from the encoder output is long term averaged and subtracted from the input to the encoder. In this way, all DC offset is removed from the encoder input waveform.

## RECEIVE OPERATION

### Decoding

The PCM word at the  $D_I$  lead is serially fetched on the first eight data clock bits of the frame. A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

### Receive Filter

The receive filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.714. The filter contains the required compensation for the  $(\sin x)/x$  response of such decoders. The receive filter characteristics and specifications are shown in Figure 9.

### Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended or 600 ohms differentially.

Table 4. Zero Transmission Level Points

Symbol	Parameter	Value	Units	Test Conditions
OTLP1 <sub>X</sub>	Zero Transmission Level Point Transmit Channel (0 dBm0) $\mu$ -Law	+ 276 + 1.00	dBm dBm	Referenced to 600 $\Omega$ Referenced to 900 $\Omega$
OTLP2 <sub>X</sub>	Zero Transmission Level Point Transmit Channel (0 dBm0) A-Law	+ 2.79 + 1.03	dBm dBm	Referenced to 600 $\Omega$ Referenced to 900 $\Omega$
OTLP1 <sub>R</sub>	Zero Transmission Level Point Receive Channel (0 dBm0) $\mu$ -Law	+ 5.76 + 4.00	dBm dBm	Referenced to 600 $\Omega$ Referenced to 900 $\Omega$
OTLP2 <sub>R</sub>	Zero Transmission Level Point Receive Channel (0 dBm0) A-Law	+ 5.79 + 4.03	dBm dBm	Referenced to 600 $\Omega$ Referenced to 900 $\Omega$

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS<sub>R</sub> input. GS<sub>R</sub> is internally connected to an analog gain setting network. When GS<sub>R</sub> is strapped to PWRO<sup>-</sup>, the receive level is maximized; when it is tied to PWRO<sup>+</sup>, the level is minimized. The output transmission level interpolates between 0 dB and -12 dB as GS<sub>R</sub> is interpolated (with a potentiometer) between PWRO<sup>+</sup> and PWRO<sup>-</sup>. The use of the output gain set is illustrated in Figure 7.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D<sub>R</sub> is the eight-code sequence specified in CCITT recommendation G.711.

**OUTPUT GAIN SET: DESIGN CONSIDERATIONS**

(Refer to Figure 7)

PWRO<sup>+</sup> and PWRO<sup>-</sup> are low impedance complementary outputs. The voltages at the nodes are:

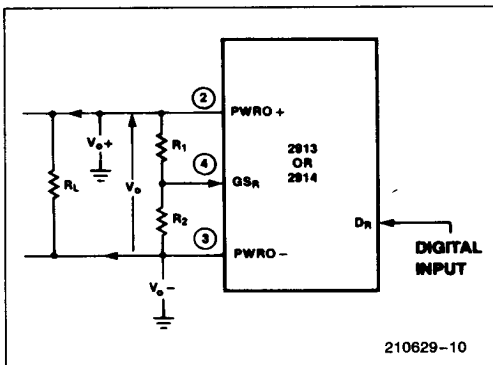


Figure 7. Gain Setting Configuration

V<sub>O</sub><sup>+</sup> at PWRO<sup>+</sup>

V<sub>O</sub><sup>-</sup> at PWRO<sup>-</sup>

$$V_O = (V_{O+}) - (V_{O-}) \text{ (total differential response)}$$

R<sub>1</sub> and R<sub>2</sub> are a gain setting resistor network with the center tap connected to the GS<sub>R</sub> input.

A value greater than 10K ohms for R<sub>1</sub> + R<sub>2</sub> and less than 100K ohms for R<sub>1</sub> in parallel with R<sub>2</sub> is recommended because:

- (a) The parallel combination of R<sub>1</sub> + R<sub>2</sub> and R<sub>L</sub> sets the total loading.
- (b) The total capacitance at the GS<sub>R</sub> input and the parallel combination of R<sub>1</sub> and R<sub>2</sub> define a time constant which has to be minimized to avoid inaccuracies.

A is the gain of the power amplifiers, where

$$A = \frac{1 + (R_1/R_2)}{4 + (R_1/R_2)}$$

For design purposes, a useful form is R<sub>1</sub>/R<sub>2</sub> as a function of A.

$$R_1/R_2 = \frac{4A - 1}{1 - A}$$

(Allowable values for A are those which make R<sub>1</sub>/R<sub>2</sub> positive.)

Examples are:

If A = 1 (maximum output), then

$$R_1/R_2 = \infty \text{ or } V(GS_R) = V_{O-};$$

i.e., GS<sub>R</sub> is tied to PWRO<sup>-</sup>

If A = 1/2, then

$$R_1/R_2 = 2$$

If A = 1/4, (minimum output) then

$$R_1/R_2 = 0 \text{ or } V(GS_R) = V_{O+};$$

i.e., GS<sub>R</sub> is tied to PWRO<sup>+</sup>.

**ABSOLUTE MAXIMUM RATINGS**

Temperature under Bias ..... -10°C to +80°C  
 Storage Temperature ..... -65°C to +150°C  
 V<sub>CC</sub> and GRDD  
   with Respect to V<sub>BB</sub> ..... -0.3V to +15V  
 All Input and Output Voltages  
   with Respect to V<sub>BB</sub> ..... -0.3V to +15V  
 Power Dissipation ..... 1.35W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**D.C. CHARACTERISTICS**

T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = +5V ±5%, V<sub>BB</sub> = -5V ±5%, GRDA = 0V, GRDD = 0V, unless otherwise specified

Typical values are for T<sub>A</sub> = 25°C and nominal power supply values

**DIGITAL INTERFACE**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I <sub>IL</sub>	Low Level Input Current			10	μA	GRDD ≤ V <sub>IN</sub> ≤ V <sub>IL</sub> (1)
I <sub>IH</sub>	High Level Input Current			10	μA	V <sub>IH</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
V <sub>IL</sub>	Input Low Voltage, except CLKSEL			0.8	V	
V <sub>IH</sub>	Input High Voltage, except CLKSEL	2.0			V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 3.2 mA at D <sub>X</sub> , $\overline{TS}_X$ and SIG <sub>R</sub>
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = 9.6 mA at D <sub>X</sub> I <sub>OH</sub> = 1.2 mA at SIG <sub>R</sub>
V <sub>ILO</sub>	Input Low Voltage, CLKSEL(2)	V <sub>BB</sub>		V <sub>BB</sub> + 0.5	V	
V <sub>IIO</sub>	Input Intermediate Voltage, CLKSEL	GRDD - 0.5		0.5	V	
V <sub>IHO</sub>	Input High Voltage, CLKSEL	V <sub>CC</sub> - 0.5		V <sub>CC</sub>	V	
C <sub>OX</sub>	Digital Output Capacitance(3)		5		pF	
C <sub>IN</sub>	Digital Input Capacitance		5	10	pF	

**D.C. CHARACTERISTICS**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ ,  $V_{BB} = -5\text{V} \pm 5\%$ ,  $GRDA = 0\text{V}$ ,  $GRDD = 0\text{V}$ , unless otherwise specified

Typical values are for  $T_A = 25^\circ\text{C}$  and nominal power supply values (Continued)

**POWER DISSIPATION** All measurements made at  $f_{DCLK} = 2.048\text{ MHz}$ , outputs unloaded

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$I_{CC1}$	$V_{CC}$ Operating Current <sup>(5)</sup>		14	19	mA	
$I_{BB1}$	$V_{BB}$ Operating Current		-18	-24	mA	
$I_{CC0}$	$V_{CC}$ Power Down Current		0.5	1.0	mA	$\overline{PDN} \leq V_{IL}$ ; after 10 $\mu\text{s}$
$I_{BB0}$	$V_{BB}$ Power Down Current		-0.5	-1.0	mA	$\overline{PDN} \leq V_{IL}$ ; after 10 $\mu\text{s}$
$I_{CCS}$	$V_{CC}$ Standby Current		1.2	2.4	mA	$FS_X, FS_R \leq V_{IL}$ ; after 300 ms
$I_{BBS}$	$V_{BB}$ Standby Current		-1.2	-2.4	mA	$FS_X, FS_R \leq V_{IL}$ ; after 300 ms
$P_{D1}$	Operating Power Dissipation <sup>(4)</sup>		140	200	mW	
$P_{D0}$	Power Down Dissipation <sup>(4)</sup>		5	10	mW	$\overline{PDN} \leq V_{IL}$ ; after 10 $\mu\text{s}$
$P_{ST}$	Standby Power Dissipation <sup>(4)</sup>		12	25	mW	$FS_X, FS_R \leq V_{IL}$

**NOTES:**

- $V_{IN}$  is the voltage on any digital pin.
- $SIG_X$  and  $DCLK_R$  are TTL level inputs between  $GRDD$  and  $V_{CC}$ ; they are also pin straps for mode selection when tied to  $V_{BB}$ . Under these conditions  $V_{ILO}$  is the input low voltage requirement.
- Timing parameters are guaranteed based on a 100 pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60 pF.
- With nominal power supply values.
- $V_{CC}$  applied last or simultaneously with  $V_{BB}$ .

**ANALOG INTERFACE, TRANSMIT CHANNEL INPUT STAGE**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$I_{BXI}$	Input Leakage Current, $V_{FXI+}$ , $V_{FXI-}$			100	nA	$-2.17\text{V} \leq V_{IN} \leq 2.17\text{V}$
$R_{IXI}$	Input Resistance, $V_{FXI+}$ , $V_{FXI-}$	10			M $\Omega$	
$V_{OSXI}$	Input Offset Voltage, $V_{FXI+}$ , $V_{FXI-}$			25	mV	
CMRR	Common Mode Rejection, $V_{FXI+}$ , $V_{FXI-}$	55			dB	$-2.17\text{V} \leq V_{IN} \leq 2.17\text{V}$
$A_{VOL}$	DC Open Loop Voltage Gain, $GS_X$	5000				
$f_c$	Open Loop Unity Gain Bandwidth, $GS_X$		1		MHz	
$C_{LXI}$	Load Capacitance, $GS_X$			50	pF	
$R_{LXI}$	Minimum Load Resistance, $GS_X$	10			K $\Omega$	

**ANALOG INTERFACE, RECEIVE CHANNEL DRIVER AMPLIFIER STAGE**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$R_{ORA}$	Output Resistance, $PWRO+$ , $PWRO-$		1		$\Omega$	
$V_{OSRA}$	Single-Ended Output DC Offset, $PWRO+$ , $PWRO-$		75	$\pm 150$	mV	Relative to $GRDA$
$C_{LRA}$	Load Capacitance, $PWRO+$ , $PWRO-$			100	pF	

### A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS

Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave.<sup>(1)</sup> Input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration.<sup>(2)</sup> All output levels are (sin x)/x corrected. Specifications are for synchronous operation. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal power supply values. ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5\text{V} \pm 5\%$ ;  $V_{BB} = -5\text{V} \pm 5\%$ ;  $GRDA = 0\text{V}$ ;  $GRDD = 0\text{V}$ ; unless otherwise specified).

#### GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
EmW	Encoder Milliwatt Response Tolerance	-0.18	$\pm 0.04$	+0.18	dBm0	Signal input of 1.064 Vrms $\mu$ -law Signal input of 1.068 Vrms A-law $T_A = 25^\circ\text{C}$ , $V_{BB} = -5\text{V}$ , $V_{CC} = +5\text{V}$
EmW <sub>TS</sub>	EmW Variation with Temperature and Supplies	-0.07	$\pm 0.02$	+0.07	dB	$\pm 5\%$ supplies, 0 to $70^\circ\text{C}$ Relative to nominal conditions
DmW	Digital Milliwatt Response Tolerance	-0.18	$\pm 0.04$	+0.18	dBm0	Measure relative to 0TLPR. Signal input per CCITT Recommendation G.711. Output signal of 1000 Hz, $R_L = \infty$ ; $T_A = 25^\circ\text{C}$ ; $V_{BB} = -5\text{V}$ , $V_{CC} = +5\text{V}$ .
DmW <sub>TS</sub>	DmW Variation with Temperature and Supplies	-0.07	+0.02	+0.07	dB	$\pm 5\%$ supplies, 0 to $70^\circ\text{C}$

#### NOTES:

1. 0 dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 Vrms or an output of 1.503 Vrms for  $\mu$ -law. See Table 4.

2. Unity gain input amplifier: GS<sub>X</sub> is connected to VF<sub>X|</sub>-, Signal input VF<sub>X|</sub>+, Maximum gain output amplifier; GS<sub>R</sub> is connected to PWRO-, output to PWRO+.

#### GAIN TRACKING Reference Level = -10 dBm0

Symbol	Parameter	2913-1, 2914-1		2913, 2914		Unit	Test Conditions
		Min	Max	Min	Max		
GT1 <sub>X</sub>	Transmit Gain Tracking Error Sinusoidal Input; $\mu$ -Law		$\pm 0.2$		$\pm 0.25$	dB	+3 to -40 dBm0
			$\pm 0.3$		$\pm 0.5$	dB	-40 to -50 dBm0
			$\pm 0.65$		$\pm 1.2$	dB	-50 to -55 dBm0
GT2 <sub>X</sub>	Transmit Gain Tracking Error Sinusoidal Input; A-Law		$\pm 0.2$		$\pm 0.25$	dB	+3 to -40 dBm0
			$\pm 0.3$		$\pm 0.5$	dB	-40 to -50 dBm0
			$\pm 0.65$		$\pm 1.2$	dB	-50 to -55 dBm0
GT1 <sub>R</sub>	Receive Gain Tracking Error Sinusoidal Input; $\mu$ -Law		$\pm 0.2$		$\pm 0.25$	dB	+3 to -40 dBm0
			$\pm 0.3$		$\pm 0.5$	dB	-40 to -50 dBm0
			$\pm 0.65$		$\pm 1.2$	dB	-50 to -55 dBm0 Measured at PWRO+, $R_L = 300\Omega$
GT2 <sub>R</sub>	Receive Gain Tracking Error Sinusoidal Input; A-Law		$\pm 0.2$		$\pm 0.25$	dB	+3 to -40 dBm0
			$\pm 0.3$		$\pm 0.5$	dB	-40 to -50 dBm0
			$\pm 0.65$		$\pm 1.2$	dB	-50 to -55 dBm0 Measured at PWRO+, $R_L = 300\Omega$

**A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS** (Continued)

**NOISE** All receive channel measurements are single ended

Symbol	Parameter	2913-1, 2914-1			2913, 2914			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
N <sub>XC1</sub>	Transmit Noise, C-Message Weighted			13			15	dBrnc0	V <sub>F<sub>X</sub>l+</sub> = GRDA, V <sub>F<sub>X</sub>l-</sub> = GS <sub>X</sub>
N <sub>XC2</sub>	Transmit Noise, C-Message Weighted with Eighth Bit Signaling			16			18	dBrnc0	V <sub>F<sub>X</sub>l+</sub> = GRDA, V <sub>F<sub>X</sub>l-</sub> = GS <sub>X</sub> ; 6th Frame Signaling
N <sub>XP</sub>	Transmit Noise, Psophometrically Weighted			-77			-75	dBm0p	V <sub>F<sub>X</sub>l+</sub> = GRDA, V <sub>F<sub>X</sub>l-</sub> = GS <sub>X</sub>
N <sub>RC1</sub>	Receive Noise, C-Message Weighted: Quiet Code			8			11	dBrnc0	D <sub>R</sub> = 11111111
N <sub>RC2</sub>	Receive Noise, C-Message Weighted: Sign Bit Toggle			9			12	dBrnc0	Input to D <sub>R</sub> is zero code with sign bit toggle at 1 KHz rate
N <sub>RP</sub>	Receive Noise, Psophometrically Weighted			-82			-79	dBm0p	D <sub>R</sub> = lowest positive decode level
N <sub>SF</sub>	Single Frequency Noise End to End Measurement			-50			-50	dBm0	CCITT G.712.4.2, measure at PWRO+
PSRR <sub>1</sub>	V <sub>CC</sub> Power Supply Rejection, Transmit Channel		-30			-30		dB	Idle channel; 200 mV P-P signal on supply; 0 to 50 KHz, measure at D <sub>X</sub>
PSRR <sub>2</sub>	V <sub>BB</sub> Power Supply Rejection, Transmit Channel		-30			-30		dB	Idle channel; 200 mV P-P signal on supply; 0 to 50 KHz, measure at D <sub>X</sub>
PSRR <sub>3</sub>	V <sub>CC</sub> Power Supply Rejection, Receive Channel		-25			-25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+, 0 to 50 KHz
PSRR <sub>4</sub>	V <sub>BB</sub> Power Supply Rejection, Receive Channel		-25			-25		dB	Idle channel; 200 mV P-P signal on supply; measure narrow band at PWRO+, 0 to 50 KHz
CT <sub>TR</sub>	Crosstalk, Transmit to Receive			-80			-71	dB	V <sub>F<sub>X</sub>l+</sub> = 0 dBm0, 1.02 KHz, D <sub>R</sub> = lowest positive decode level, measure at PWRO+
CT <sub>RT</sub>	Crosstalk, Receive to Transmit			-80			-71	dB	D <sub>R</sub> = 0 dBm0, 1.02 KHz V <sub>F<sub>X</sub>l+</sub> = GRDA, measure at D <sub>X</sub>

**A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS** (Continued)

**DISTORTION**

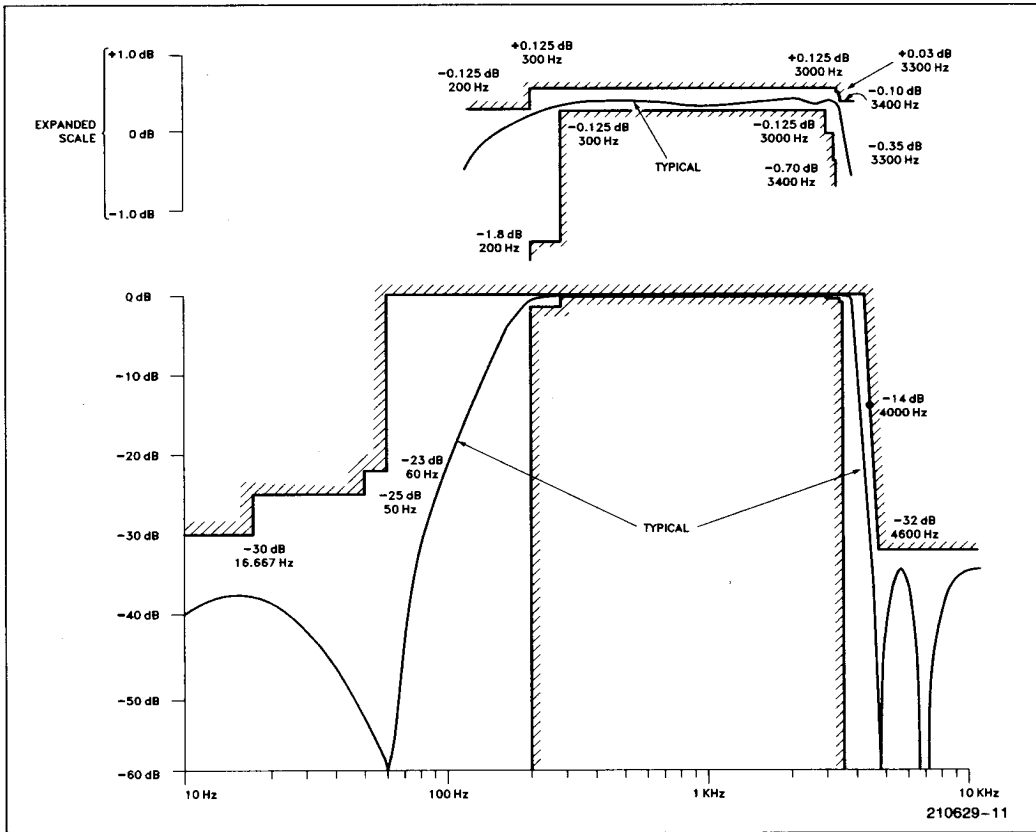
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SD1 <sub>X</sub>	Transmit Signal to Distortion, $\mu$ -Law Sinusoidal Input; CCITT G.714-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD2 <sub>X</sub>	Transmit Signal to Distortion, A-Law Sinusoidal Input; CCITT G.714-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD1 <sub>R</sub>	Receive Signal to Distortion, $\mu$ -Law Sinusoidal Input; CCITT G.714-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
SD2 <sub>R</sub>	Receive Signal to Distortion, A-Law Sinusoidal Input; CCITT G.714-Method 2	36			dB	0 to -30 dBm0
		30			dB	-30 to -40 dBm0
		25			dB	-40 to -45 dBm0
DP <sub>X</sub>	Transmit Single Frequency Distortion Products			-46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
DP <sub>R</sub>	Receive Single Frequency Distortion Products			-46	dBm0	AT&T Advisory #64 (3.8) 0 dBm0 Input Signal
IMD <sub>1</sub>	Intermodulation Distortion, End to End Measurement			-35	dB	CCITT G.712 (7.1)
IMD <sub>2</sub>	Intermodulation Distortion, End to End Measurement			-49	dBm0	CCITT G.712 (7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			-25	dBm0	CCITT G.712 (6.1)
SIS	Spurious in Band Signals, End to End Measurement			-40	dBm0	CCITT G.712 (9)
D <sub>AX</sub>	Transmit Absolute Delay		245		$\mu$ s	Fixed Data Rate. CLK <sub>X</sub> = 2.048 MHz 0 dBm0, 1.02 KHz signal at VF <sub>XI</sub> + Measure at D <sub>X</sub> .
D <sub>DX</sub>	Transmit Differential Envelope Delay Relative to D <sub>AX</sub>	170			$\mu$ s	f = 500 - 600 Hz
		95			$\mu$ s	f = 600 - 1000 Hz
		45			$\mu$ s	f = 1000 - 2600 Hz
		105			$\mu$ s	f = 2600 - 2800 Hz
D <sub>AR</sub>	Receive Absolute Delay		190		$\mu$ s	Fixed Data Rate, CLK <sub>R</sub> = 2.048 MHz; Digital input is DMW codes. Measure at PWRO + .
D <sub>DR</sub>	Receive Differential Envelope Delay Relative to D <sub>AR</sub>	45			$\mu$ s	f = 500 - 600 Hz
		35			$\mu$ s	f = 600 - 1000 Hz
		85			$\mu$ s	f = 1000 - 2600 Hz
		110			$\mu$ s	f = 2600 - 2800 Hz

**A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS** (Continued)

**TRANSMIT CHANNEL TRANSFER CHARACTERISTICS**

Input amplifier is set for unity gain; noninverting; maximum gain output.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G <sub>RX</sub>	Gain Relative to Gain at 1.02 KHz					0 dBm0 Signal input at VF <sub>XI</sub> +
	16.67 Hz			-30	dB	
	50 Hz			-25	dB	
	60 Hz			-23	dB	
	200 Hz	-1.8		-0.125	dB	
	300 to 3000 Hz	-0.125		+0.125	dB	
	3300 Hz	-0.35		+0.03	dB	
	3400 Hz	-0.7		-0.10	dB	
	4000 Hz			-14	dB	
	4600 Hz and Above			-32	dB	



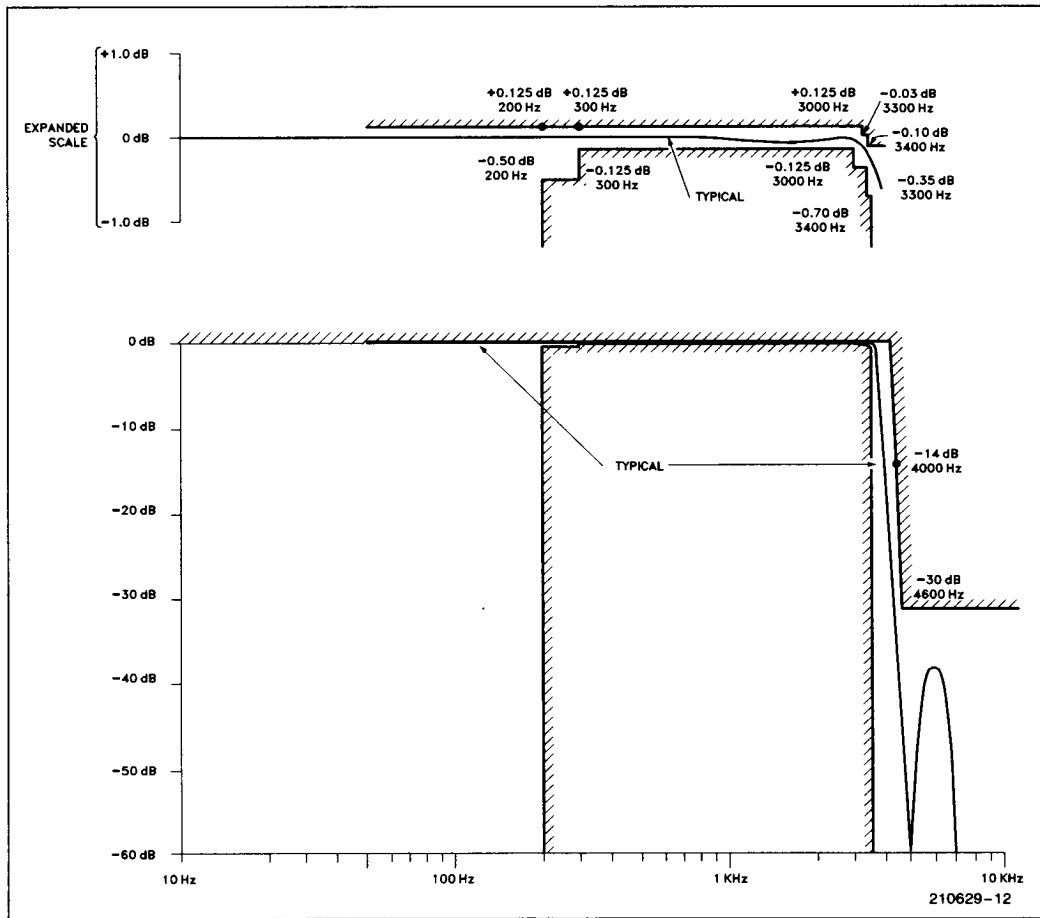
**Figure 8. Transmit Channel**  
5-61



**A.C. CHARACTERISTICS—TRANSMISSION PARAMETERS** (Continued)

**RECEIVE CHANNEL TRANSFER CHARACTERISTICS**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G <sub>RR</sub>	Gain Relative to Gain at 1.02 KHz					0 dBm <sub>0</sub> Signal input at D <sub>R</sub>
	Below 200 Hz			+ 0.125	dB	
	200 Hz	- 0.5		+ 0.125	dB	
	300 to 3000 Hz	- 0.125		+ 0.125	dB	
	3300 Hz	- 0.35		+ 0.03	dB	
	3400 Hz	- 0.7		- 0.1	dB	
	4000 Hz			- 14	dB	
	4600 Hz and Above			- 30	dB	



**Figure 9. Receive Channel**

## A.C. CHARACTERISTICS—TIMING PARAMETERS

## CLOCK SECTION

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{CY}$	Clock Period, CLK <sub>X</sub> , CLK <sub>R</sub>	488			ns	$f_{CLKX} = f_{CLKR} = 2.048 \text{ MHz}$
$t_{CLK}$	Clock Pulse Width, CLK <sub>X</sub> , CLK <sub>R</sub>	220			ns	
$t_{DCLK}$	Data Clock Pulse Width	220			ns	$64 \text{ KHz} \leq f_{DCLK} \leq 2.048 \text{ MHz}$
$t_{CDC}$	Clock Duty Cycle, CLK <sub>X</sub> , CLK <sub>R</sub>	45	50	55	%	
$t_r, t_f$	Clock Rise and Fall Time	5		30	ns	

TRANSMIT SECTION, FIXED DATA RATE MODE<sup>(1)</sup>

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{DZX}$	Data Enabled on TS Entry	0		145	ns	$0 < C_{LOAD} < 100 \text{ pF}$
$t_{DDX}$	Data Delay from CLK <sub>X</sub>	0		145	ns	$0 < C_{LOAD} < 100 \text{ pF}$
$t_{HZX}$	Data Float on TS Exit	60		215	ns	$C_{LOAD} = 0$
$t_{SON}$	Timeslot X to Enable	0		145	ns	$0 < C_{LOAD} < 100 \text{ pF}$
$t_{SOFF}$	Timeslot X to Disable	60		215	ns	$C_{LOAD} = 0$
$t_{FSD}$	Frame Sync Delay	100		$t_{CLK}$	ns	
$t_{SS}$	Signal Setup Time	0			ns	
$t_{SH}$	Signal Hold Time	0			ns	

## RECEIVE SECTION, FIXED DATA RATE MODE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{DSR}$	Receive Data Setup	10			ns	
$t_{DHR}$	Receive Data Hold	60			ns	
$t_{FSD}$	Frame Sync Delay	100		$t_{CLK}$	ns	
$t_{SIGR}$	SIG <sub>R</sub> Update	0		2	$\mu\text{s}$	

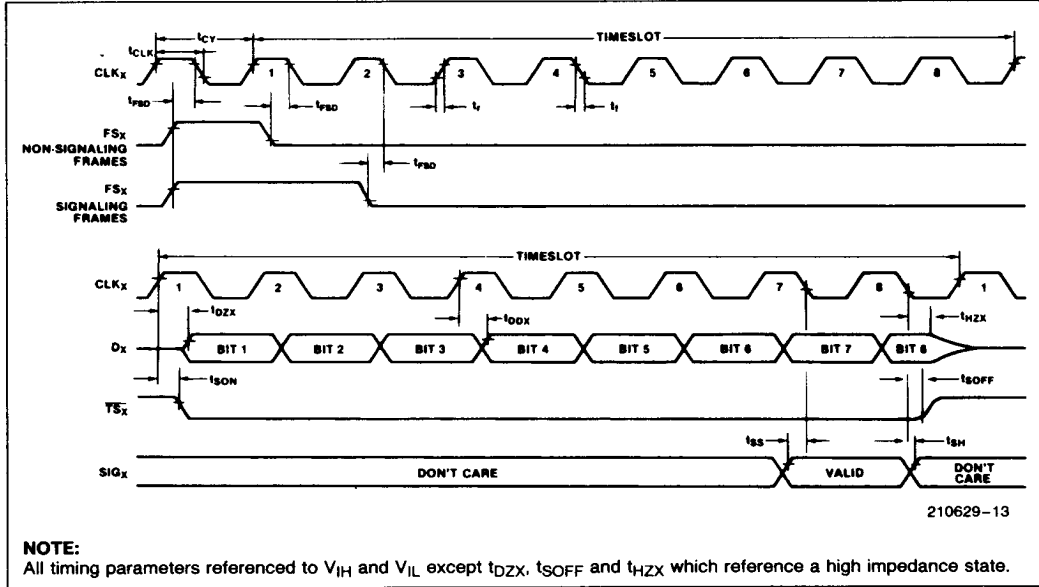
## NOTE:

1. Timing parameters  $t_{DZX}$ ,  $t_{HZX}$ , and  $t_{SOFF}$  are referenced to a high impedance state.

WAVEFORMS

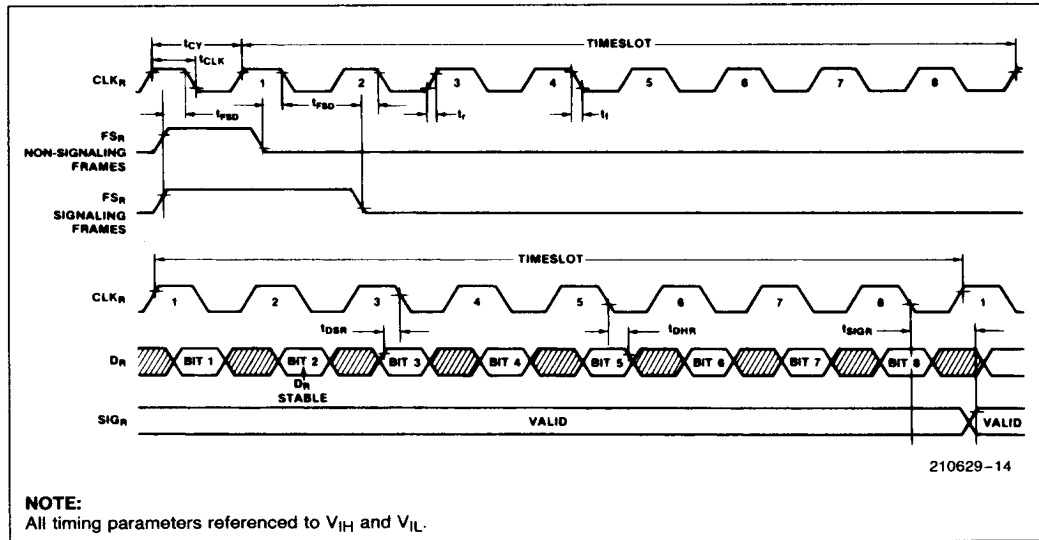
Fixed Data Rate Timing

TRANSMIT TIMING



210629-13

RECEIVE TIMING



210629-14

**WAVEFORMS** (Continued)

**TRANSMIT SECTION, VARIABLE DATA RATE MODE<sup>(1)</sup>**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t <sub>SDX</sub>	Timeslot Delay from DCLK <sub>X</sub> <sup>(2)</sup>	140		t <sub>DX</sub> - 140	ns	
t <sub>FSD</sub>	Frame Sync Delay	100		t <sub>CY</sub> - 100	ns	
t <sub>DDX</sub>	Data Delay from DCLK <sub>X</sub>	0		100	ns	0 < C <sub>LOAD</sub> < 100 pF
t <sub>DON</sub>	Timeslot to D <sub>X</sub> Active	0		50	ns	0 < C <sub>LOAD</sub> < 100 pF
t <sub>DOFF</sub>	Timeslot to D <sub>X</sub> Inactive	0		80	ns	0 < C <sub>LOAD</sub> < 100 pF
t <sub>DX</sub>	Data Clock Period	488		15620	ns	
t <sub>DFSX</sub>	Data Delay from FS <sub>X</sub>	0		140	ns	

**RECEIVE SECTION, VARIABLE DATA RATE MODE**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t <sub>SDR</sub>	Timeslot Delay from DCLK <sub>R</sub> <sup>(3)</sup>	140		t <sub>DR</sub> - 140	ns	
t <sub>FSD</sub>	Frame Sync Delay	100		t <sub>CY</sub> - 100	ns	
t <sub>DSR</sub>	Data Setup Time	10			ns	
t <sub>DHR</sub>	Data Hold Time	60			ns	
t <sub>DR</sub>	Data Clock Period	488		15620	ns	
t <sub>SER</sub>	Timeslot End Receive Time	60			ns	

**64 KB OPERATION, VARIABLE DATA RATE MODE**

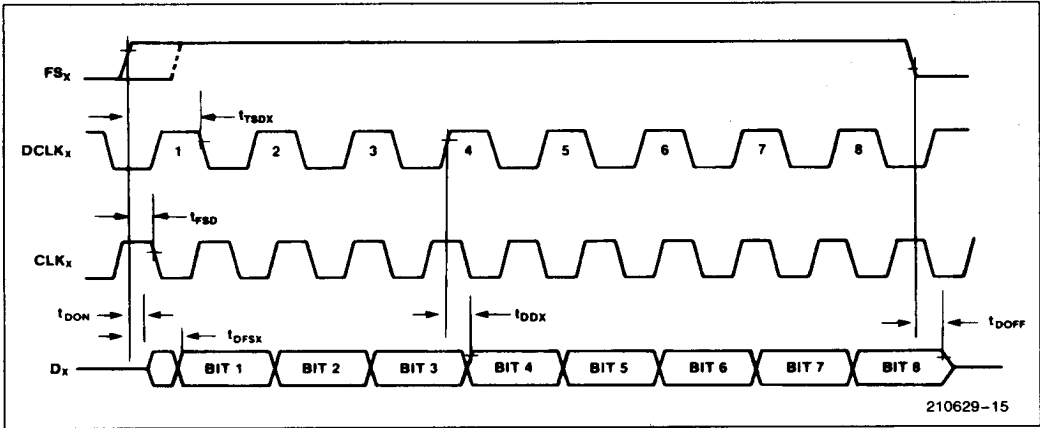
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t <sub>FSLX</sub>	Transmit Frame Sync Minimum Downtime	488			ns	FS <sub>X</sub> is TTL high for remainder of frame
t <sub>FSLR</sub>	Receive Frame Sync Minimum Downtime	1952			ns	FS <sub>R</sub> is TTL high for remainder of frame
t <sub>DCLK</sub>	Data Clock Pulse Width			10	μs	

**NOTES:**

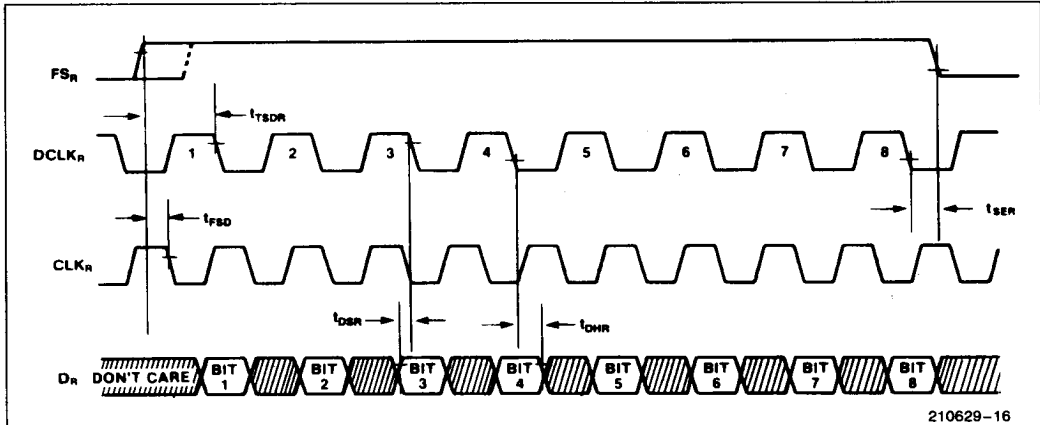
1. Timing parameters for t<sub>DON</sub> and t<sub>DOFF</sub> are referenced to a high impedance state.
2. t<sub>FSLX</sub> minimum requirements override t<sub>SDX</sub> maximum spec for 64 KHz operation.
3. t<sub>FSLR</sub> minimum requirements override t<sub>SDR</sub> maximum spec for 64 KHz operation.

VARIABLE DATA RATE TIMING

TRANSMIT TIMING



RECEIVE TIMING



**NOTE:**  
All timing parameters referenced to  $V_{IH}$  and  $V_{IL}$  except  $t_{DON}$  and  $t_{DOFF}$  which reference a high impedance state.

A.C. TESTING INPUT, OUTPUT WAVEFORM

