ON Semiconductor®

ASM3P2180A

Peak Reducing EMI Solution

Features

- Generates a 1x EMI optimized clock output.
- Input frequency: 6MHz - 10MHz
  18MHz - 30MHz
- Output frequency: 6MHz - 10MHz
  18MHz - 30MHz
- Two selectable down spread options.
- Selectable frequency range.
- Integrated loop filter components.
- Operates with a 3.3V supply.
- CMOS design.
- 8-pin SOIC packages.

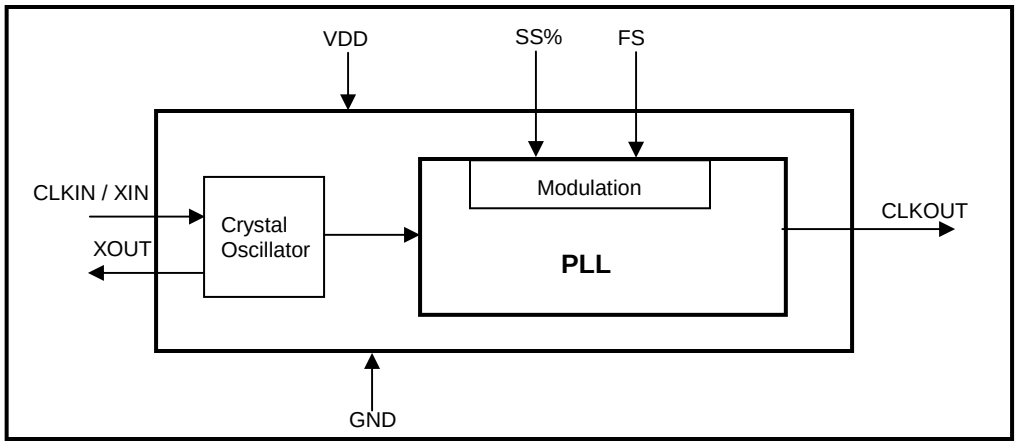
Product Description

The ASM3P2180A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. ASM3P2180A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. ASM3P2180A allows significant system cost savings by reducing the number of circuit board layers, and shielding that are traditionally required to pass EMI regulations. ASM3P2180A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation. ASM3P2180A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all-digital method.

Applications

The ASM3P2180A is targeted towards notebook LCD displays, other displays using an LVDS interface, PC peripheral devices and embedded systems.

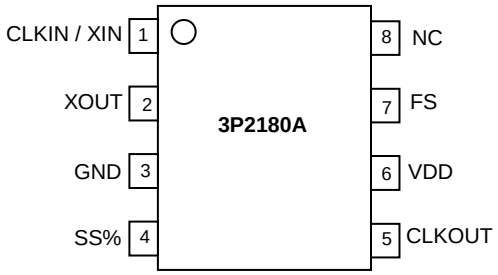
Block Diagram



JANUARY 2010 – Rev. 2

Publication Order Number:
ASM3P2180/D

Pin Diagram



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or external reference clock input.
2	XOUT	O	Connection for an external crystal. If using an external reference, this pin must be left unconnected.
3	GND	P	Ground to entire chip.
4	SS%	I	Spread Selection Input. Has an internal pull-up resistor.
5	CLKOUT	O	Modulated Clock Output.
6	VDD	P	Power supply for the entire chip.
7	FS	I	Frequency selection bit. This pin selects the frequency range of operation. (*Refer to the Frequency Range Selection Table*). Has an internal pull-up resistor.
8	NC	-	No connect.

Frequency Range Selection

FS	Frequency Range (MHz)
0	6-10
1	18-30

Spread Selection table

SS%	Frequency (MHz)		Deviation (%) (typ)
	FS=0	FS=1	
0	6	18	-2
	8	24	-1.5
	10	30	-1
1	6	18	-4
	8	24	-3
	10	30	-2

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	2.8	3.7	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	℃
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND – 0.3		0.8	V
V_{IH}	Input high voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input low current (pull-up resistors on inputs SS%, FS)			-27	µA
I_{IH}	Input high current			18	µA
I_{XOL}	X_{OUT} output low current (@ 0.4V, V_{DD} = 3.3V)		3		mA
I_{XOH}	X_{OUT} output high current (@2.5V, V_{DD} = 3.3V)		4		mA
V_{OL}	Output low voltage (V_{DD} = 3.3V, I_{OL} = 4mA)			0.4	V
V_{OH}	Output high voltage (V_{DD} = 3.3V, I_{OH} = 4mA)	2.5			V
I_{CC}	Dynamic supply current normal mode (3.3V and 10pF loading)	10	15	25	mA
I_{DD} *	Static supply current standby mode			7	mA
V_{DD}	Operating voltage	2.8	3.3	3.7	V
t_{ON}	Power up time (first locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock output impedance		50		Ω

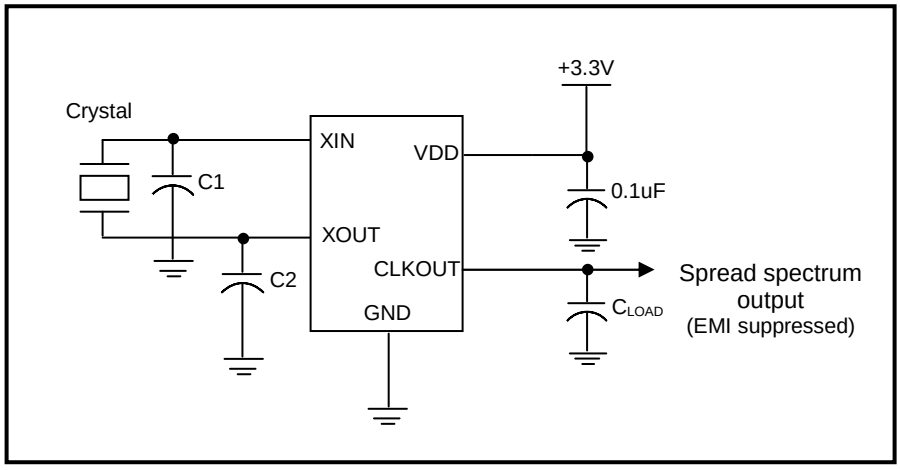
*CLKIN pin pulled to GND

AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN	Input frequency	FS=0	6		10	MHz
		FS=1	18		30	
CLKOUT	Output frequency	FS=0	6		10	MHz
		FS=1	18		30	
t_{LH}*	Output rise time (measured at 0.8V to 2.0V)		1.2	1.3	1.4	nS
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)		0.8	0.9	1.0	nS
t_{JC}	Jitter (cycle to cycle)			±325		pS
t_D	Output duty cycle		45	50	55	%

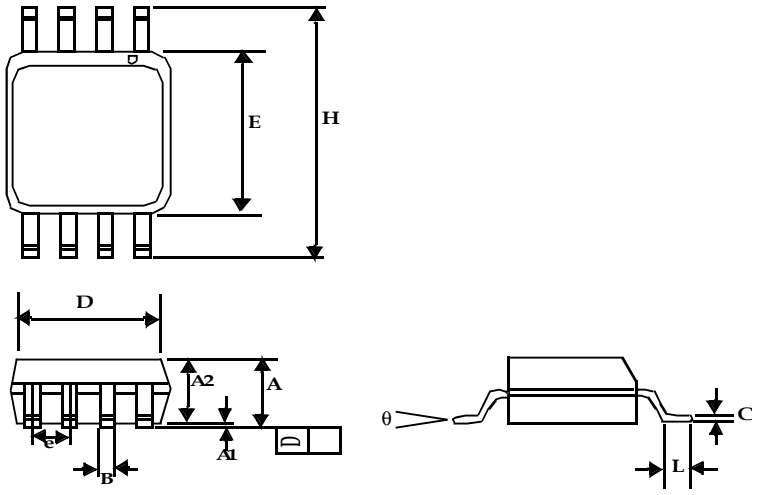
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

Typical Test Circuit



Package Information

8-Pin SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Ordering Codes

Part Number	Marking	Package Type	Temperature
ASM3P2180AF-08ST	ACT	8-pin SOIC, tube, Pb Free	0℃ to +70℃
ASM3P2180AF-08SR	ACT	8-pin SOIC, tape and reel, Pb Free	0℃ to +70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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