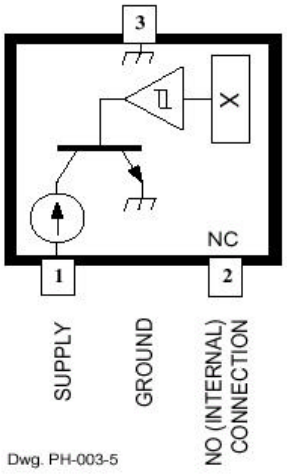
A1140/42/43/45

Preliminary Data Sheet

PRELIMINARYL DATA SHEET
SUBJECT TO CHANGE WITHOUT NOTICE

Suffix Code 'LH' Pinning
(SOT23W)



Pinning is shown viewed from branded side.

See typical application drawing for UA pinning.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V_{CC} ..... **26.5 V**
Reverse-Battery Voltage
V_{RB} ..... **-18 V**
Magnetic Flux Density
B ..... **Unlimited**
Package Power Dissipation θ_{ja},
UA..... **206 °C/W**
LH[1].....**248 °C/W**
Junction Temperature, T_J ..... **+170°C**
Operating Temperature Range,T_A
Suffix 'E'.....**-40 °C to +85 °C**
Suffix 'L'..... **-40 °C to +150 °C**
Storage Temperature Range
T_S ..... **-65 °C to +170 °C**

Two-Wire, Factory-Programmed, Chopper-Stabilized, Unipolar Hall-Effect Switch

The A114X is a two-wire, unipolar, Hall-effect switch with factory programmability for end-of-line optimization of switch point accuracy. This device uses a patented high frequency chopper-stabilization technique on Allegro's most advanced BiCMOS wafer fabrication process to achieve magnetic stability and to eliminate offset inherent in single-element devices and from harsh-application environments.

This device provides on-chip transient protection. A zener clamp on the power supply protects against over-voltage conditions on the supply line.

The output of the A1143 will switch HIGH in the presence of a sufficiently large south-pole magnetic field and will switch LOW with the removal of the field. The A1140/2/5 has the opposite polarity as the A1143, switching LOW in the presence of a sufficiently large south-pole magnetic field.

Two package styles provide a magnetically optimized package for most applications. Suffix "LH" is a miniature low profile package for surface-mount applications; suffix "UA" is a three-lead ultra-mini Single Inline Package (SIP) for through-hole mounting.

FEATURES / BENEFITS

- Chopper Stabilization
  - Low switch-point drift over temperature
  - Low stress sensitivity
- Factory programmed at end-of-line
  - Optimized switch Points
- On-chip Protection
  - Supply transient protection
  - Robust ESD/EMC protection
  - Reverse-battery protection
- On-board Voltage Regulator
  - 3.8 V to 24 V operation

Order by complete part number (i.e. A1142LUA).

[1] The "LH" PPD is based on a 0.062" thick FR4, single-sided board using 2 oz. copper, with a 0.55 mm^2 area of copper attached to the ground lead.

CHARACTERISTICS

Valid over operating temperature range unless otherwise noted.

Part Number	Characteristics	Symbol	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS							
A114X	Supply Voltage	V_{CC}	Operating	3.8	-	24	V
A1140	Supply Current	$I_{GND(L)}$	Output I Low	2	-	5	mA
		$I_{GND(H)}$	Output I High	12	-	17	mA
A1142/3/5	Supply Current	$I_{GND(L)}$	Output I Low	5	-	6.9	mA
		$I_{GND(H)}$	Output I High	12	-	17	mA
A114X	Output Rise Time[2]	t_r	R_L=100 Ohms, C_{BYP}=0.1uF	-	20	-	us
	Output Fall Time[2]	t_f	R_L=100 Ohms, C_{BYP}=0.1uF	-	20	-	us
	Chopping Frequency	f_C	-	-	340	-	kHz
	Power-Up Time	t_{on}	-	-	-	25	µs
	Power-Up State	POS	$t < t_{on}$, $t_r < 5$us, no bypass capacitor	-	HIGH	-	-
	Zener Voltage	V_Z	I = 10mA	28	36	40	V

MAGNETIC CHARACTERISTICS							
A1140/2/3	Operate Point, Bop	1140/2	B > B_{op}, I_{GND} = Low	50	85	115	G
		1143	B > B_{op}, I_{GND} = High				
	Release Point, Brp	1140/2	B < B_{RP}, I_{GND} = High	45	-	110	G
		1143	B < B_{RP}, I_{GND} = Low				
	Hysteresis	B_{HYS}	B_{OP} - B_{RP}	5	15	30	G
A1145	Operate Point, Bop	1145	B > B_{op}, I_{GND} = Low	10	37	60	G
	Release Point, Brp		B < B_{RP}, I_{GND} = High	5	-	55	G
	Hysteresis	B_{HYS}	B_{OP} - B_{RP}	5	15	30	G

[2] Typical rise and fall time of the Hall sensor is 1us, the true rise and fall time is dependent on the load circuit as indicated by the 20us specification.

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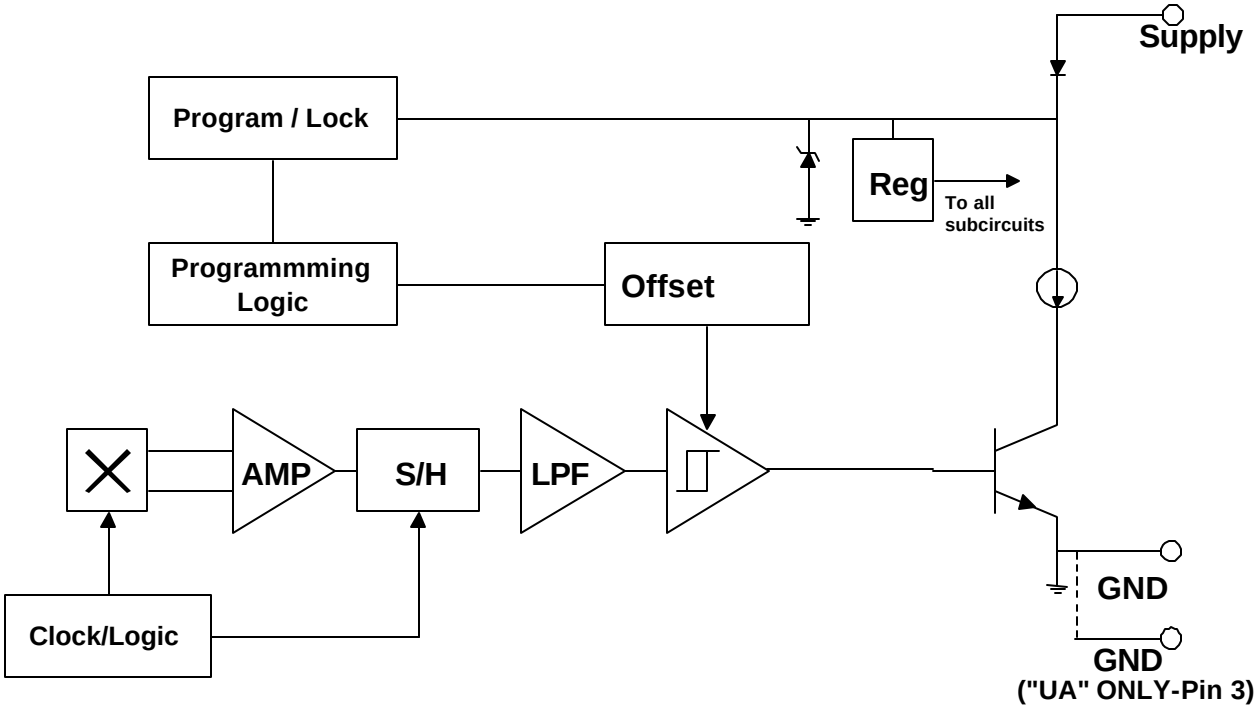
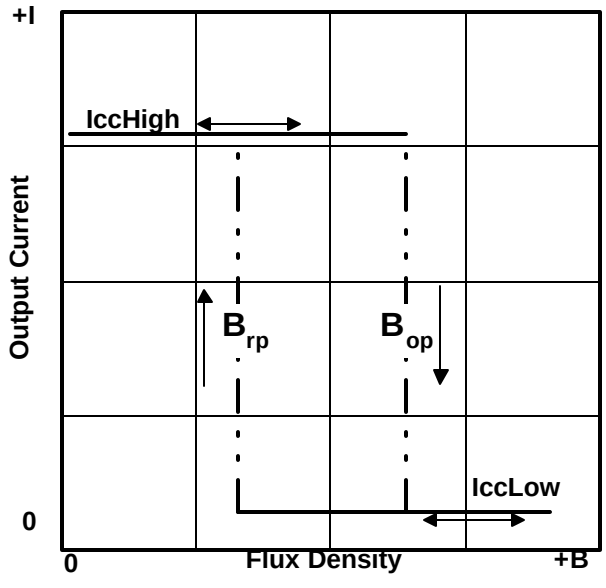
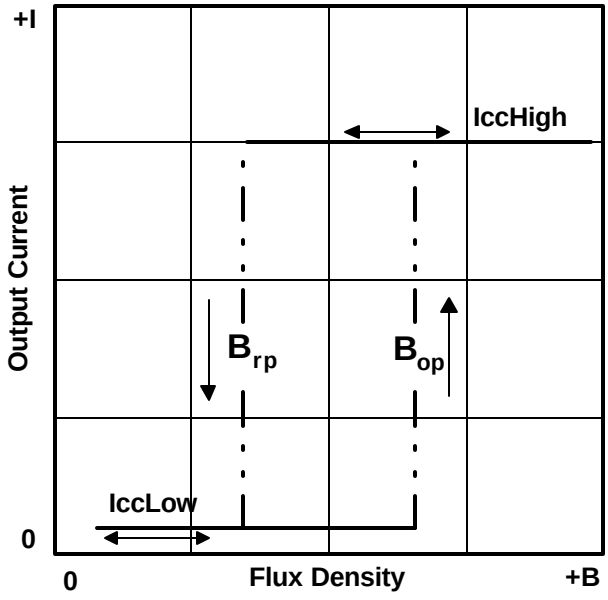
FUNCTIONAL BLOCK DIAGRAM



A1140/2/5 Hysteresis Curve



A1143 Hysteresis Curve



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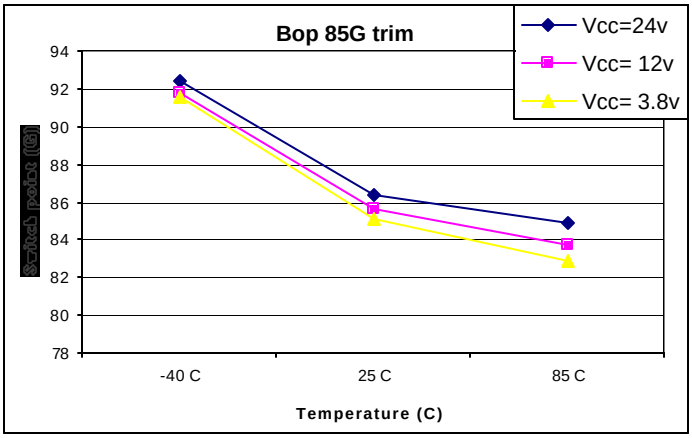
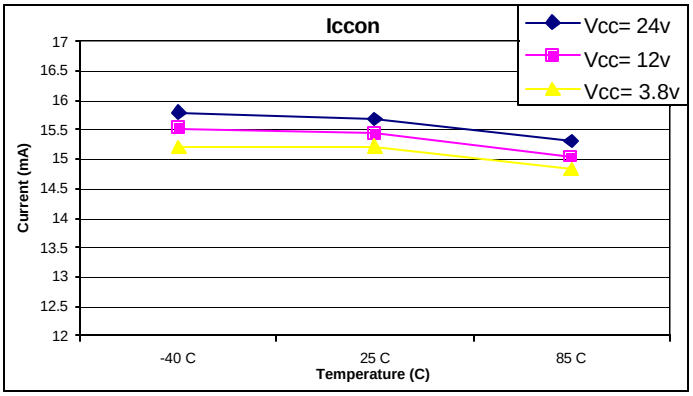
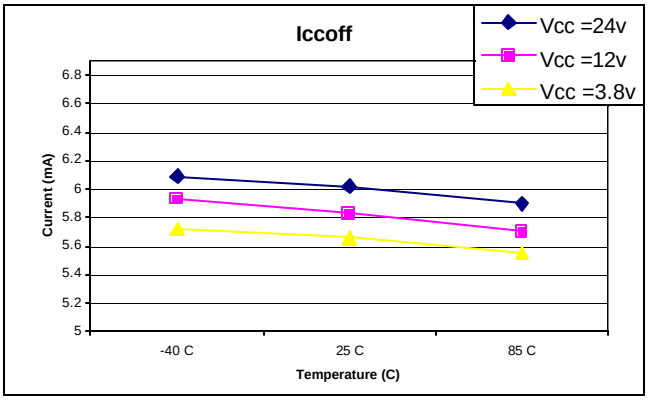
Typical Characterization Data

All data is the average of 1 Lot, >1000 Units







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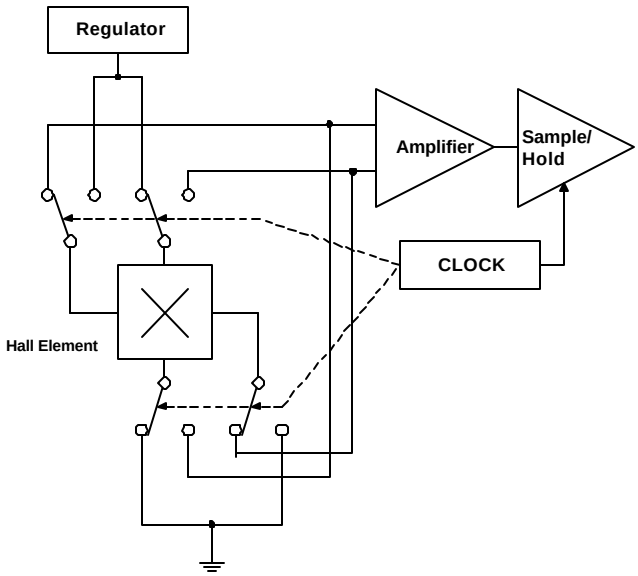
Functional Description

Chopper-Stabilization Technique. A limiting factor for switch point accuracy when using Hall effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range.

Chopper Stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro patented technique; dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at base band while the dc offset becomes a high frequency signal. Then, using a low-pass filter the signal passes while the modulated dc offset is suppressed.

The chopper stabilization technique uses a 170 kHz high frequency clock. The Hall plate chopping occurs on each clock edge resulting in a 340 kHz chop frequency. The high frequency operation allows for a greater sampling, which produces higher accuracy and faster signal processing capability. Using this chopper stabilization approach, the chip is de-sensitized to the effects of temperature and stress. This technique produces devices that have an extremely stable quiescent Hall output voltage, is immune to thermal stress, and has precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic integration and sample and hold circuits.

The repeatability of switching with a magnetic field is slightly affected using a chopper technique. Allegro's high frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that may notice the degradation are those that require the precise sensing of alternating magnetic fields such as ring magnet speed sensing. For those applications, Allegro recommends the "low jitter" family of digital sensors.



Concept of Dynamic Quadrature Offset Cancellation

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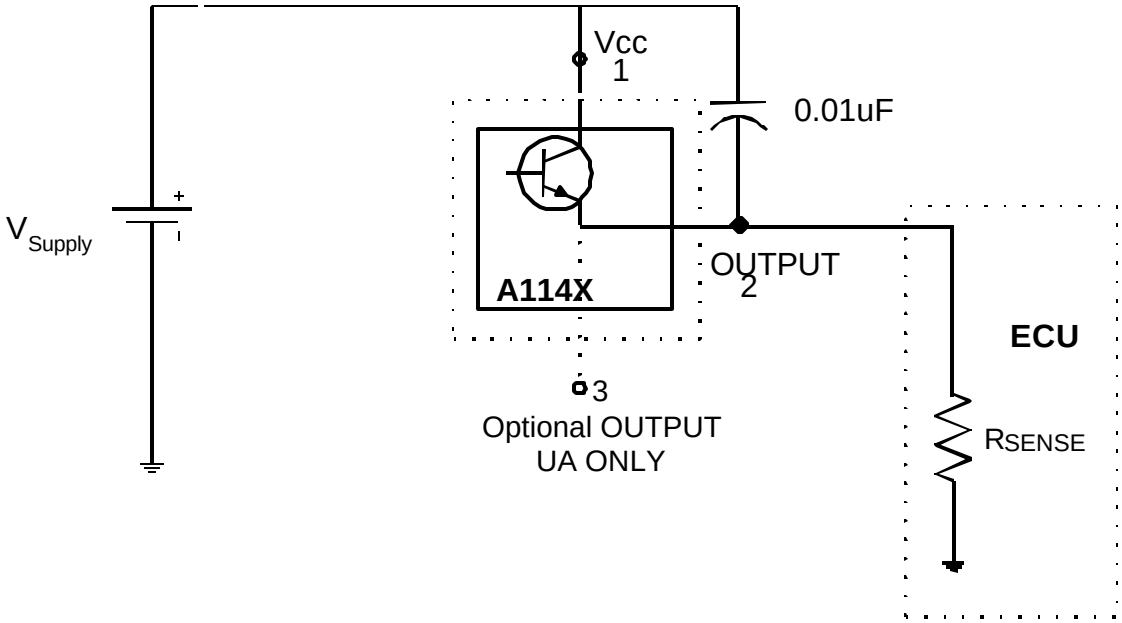
TYPICAL APPLICATION CIRCUIT

Applications. It is *necessary* that an external bypass capacitor be connected between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. (The diagram below shows a 0.01uF bypass capacitor) *The bypass capacitor should be no further than 5 mm away from the Hall sensor.* The bypass capacitor is to protect the Hall IC only. All high frequency interferences conducted along the supply lines will be passed directly to the load through the bypass capacitor. Therefore, the ECU must have sufficient protection other than the bypass capacitor placed in parallel with the Hall IC.

A series resistor on the supply side, Rs (not shown), in combination with the bypass capacitor will create a filter for EMC pulses. (See the ISO Transient Table). The series resistor (Rs) and/or sense resistor (Rsense) will have voltage drops across them that must be considered for the minimum Vcc requirement of the device. The preferred sense resistor value is approximately 100 ohms.

Typical Application (UA pkg):



Extensive applications information on magnets and Hall-effect sensors including Chopper-Stabilization is available in the *Allegro Electronic Data Book* CD, or at the website: http://www.allegromicro.com .

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DEVICE QUALIFICATION PROGRAM

Test Name	Test Conditions	Test Length	# of Lots	Sample / lot	Comments
Pre/Post Test	Ta = room, hot, cold				
High Temperature Operating Life (HTOL)	Ta = 150°C, Tj ? 170°C	408 hrs	1	77	JESD22-A108
High Temperature Bake (HTB)	Ta = 170°C	1000 hrs	1	77	JESD22-A103
Pre Conditioning (PC)	85°C/85%RH	168 hrs	1	231	JESD22-A112 & A113
Temperature Humidity Bias (THB) or HAST	85°C/85%RH 130°C/85%RH	1000 hrs 50 hrs	1	77	JESD22-A101 JESD22-A110
Autoclave (AC)	121°C/15 psig	96 hrs	1	77	JESD22-A102
Temperature Cycle (TC)	-65°C to +150°C or -50°C to +150°C	500 cycles 1000 cycles	1	77	JESD22-A104
External Visual (EV)					
Physical Dimensions (PD)			1	30	
Lead Integrity			1	45	
Bond Pull Strength			1	30	
ESD	HBM & MM		1	3 per model per V step	JESD22-A114 & A115,CDF-AEC-Q100-002, 003 & 011
Solderability (SD)			1	15	JESD22-B102
Early Life Failure Rate (ELFR)	125°C or 150°C	48 hrs 24 hrs	1	800	JESD22-A108
Gate Leakage (GL)			1	6	CDF- AEC-Q100-006
Electrical Distributions (ED)	Ta = room, hot, cold		3	30	

EMC Requirements (Electromagnetic Compatibility)

Please contact your local representative for EMC results

Test Name	Reference Specification
ESD – Human Body Model	AEC-Q100-002
ESD – Machine Model	AEC-Q100-003
Conducted Transients	ISO 7637-1
Direct RF Injection	ISO 11452-7
Bulk Current Injection	ISO 11452-4
TEM Cell	ISO 11452-3

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POWER DE-RATING

Due to internal power consumption, the junction temperature of the IC, Tj, is higher than the ambient environment temperature, Ta. To ensure that the device does not operate above the maximum rated junction temperature use the following calculations:

$$\Delta T = P_D * R\theta ja$$

Where: $P_D = Vcc * Icc$

$$\therefore \Delta T = Vcc * Icc * R\theta ja$$

Where ΔT denotes the temperature rise resulting from the IC's power dissipation.

$$Tj = Ta + \Delta T$$

For the sensor :

Tj(max) = 170°C
Rθja (UA Pkg) = 206°C/W

Typical Tj calculation:

Ta = 25 °C
Vcc = 12 V
$Icc = Icc_{ONtyp}$ = 14.5 mA

$P_D = Vcc * Icc = 12\ V * 14.5\ mA = 174\ mW$

$\Delta T = P_D * R\theta ja = 174\ mW * 206°C/W = 35.8\ °C$

$Tj = Ta + \Delta T = 25\ °C + 35.8\ °C = 60.8\ °C$

Maximum Allowable Power Dissipation Calculation for A118X Family[3]:

Assume:

$Ta = Ta_{max} = 150\ °C$
Tj(max) = 170°C
$Icc = I_{ONmax} = 17\ mA$

If:

$$Tj = Ta + \Delta T$$

Then:

$$\Delta T_{max} = Tj_{max} - Ta_{max} = 170\ °C - 150\ °C = 20\ °C$$

If:

$$\Delta T = P_D * R\theta ja$$

Then:

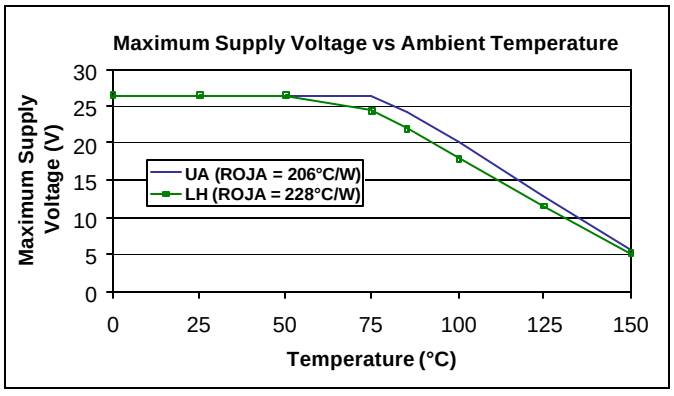
$P_{Dmax} = \Delta T_{max} / R\theta ja = 20\ °C / 206\ °C/W = 97.1\ mW$

If:

$$P_D = Vcc * Icc$$

Then the maximum Vcc at 150°C is therefore:

$Vccmax = P_{Dmax} / Icc = 97.1\ mW / 17\ mA = 5.7\ V$



[3] The "LH" PPD is based on a 0.062" thick FR4, single-sided board using 2 oz. copper, with a 0.55 mm^2 area of copper attached to the ground lead.

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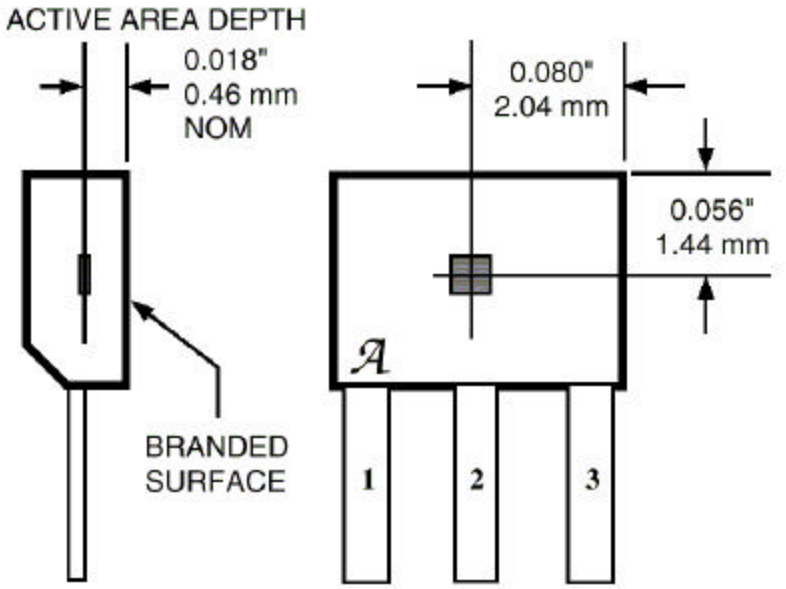
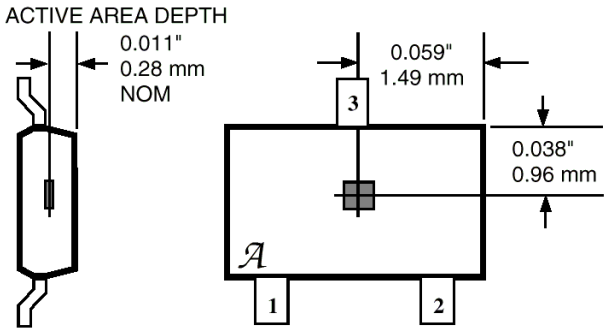
Package Designators 'UA' and 'UA-TL'



Dwg. MH-011-9A

Package Designator 'LH'



Dwg. MH-025

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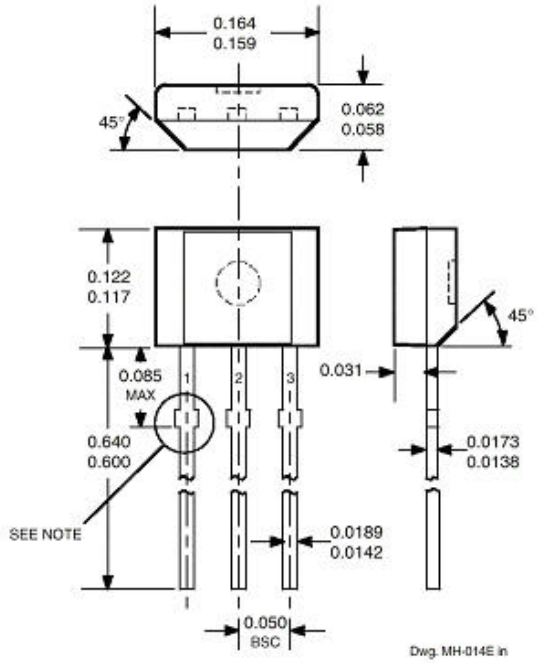
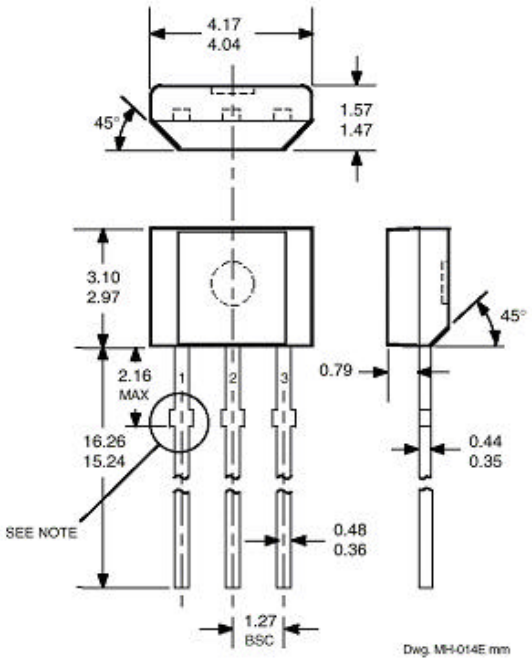
PACKAGE DESIGNATOR 'UA'

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.

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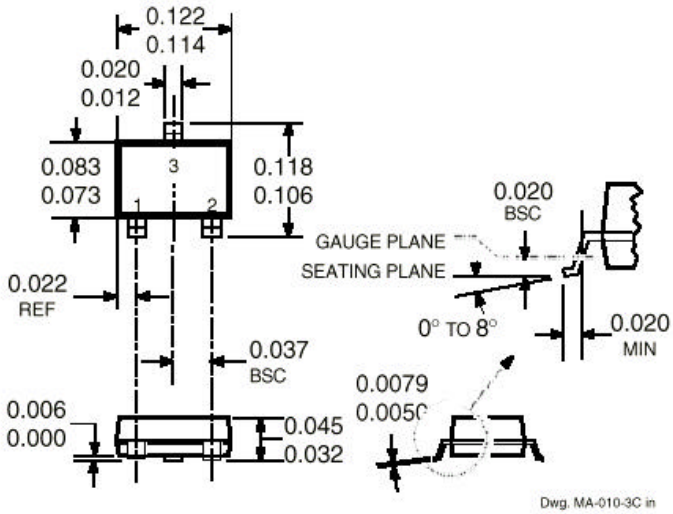
PACKAGE DESIGNATOR 'LH'

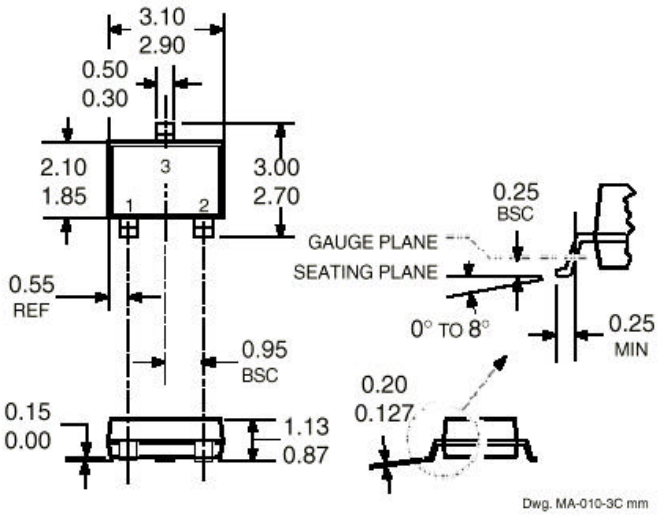
(fits SC-74A solder-pad layout)

Dimensions in Inches
(for reference only)

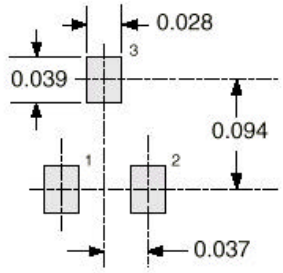


Dwg. MA-010-3C in

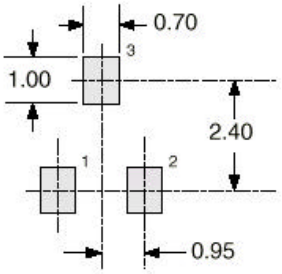
Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-010-3C mm



Dwg. MA-011-3 in



Dwg. MA-011-3 mm

NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Where no tolerance is specified, dimension is nominal.
5. Add "LT" to part number for tape and reel.

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The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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