



STB100NH02L

N-CHANNEL 24V - 0.0052 Ω - 60A D²PAK STripFET™ III POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB100NH02L	24 V	< 0.006 Ω	60 A (2)

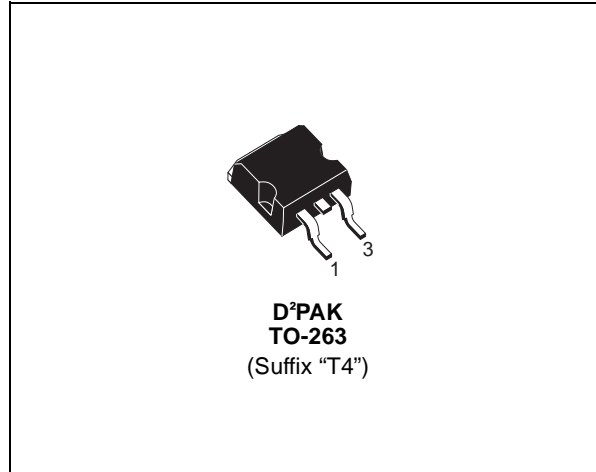
- TYPICAL R_{DS(on)} = 0.0052 Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.007 Ω @ 5 V
- R_{DS(ON)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D²PAK (TO-263)
POWER PACKAGE IN TUBE (NO SUFFIX) OR
IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

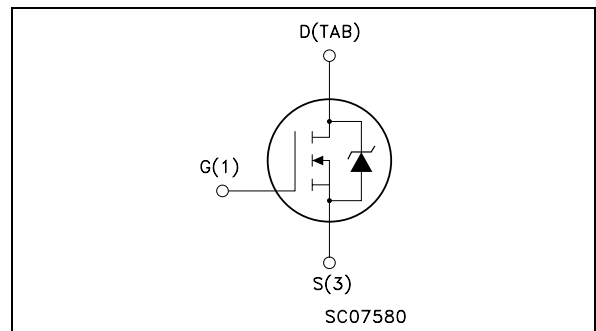
The STB100NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter applications where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{spike(1)}	Drain-source Voltage Rating	30	V
V _{DS}	Drain-source Voltage (V _{GS} = 0)	24	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	24	V
V _{GS}	Gate- source Voltage	± 20	V
I _{D(2)}	Drain Current (continuous) at T _C = 25°C	60	A
I _{D(2)}	Drain Current (continuous) at T _C = 100°C	60	A
I _{DM(3)}	Drain Current (pulsed)	240	A
P _{tot}	Total Dissipation at T _C = 25°C	100	W
	Derating Factor	0.67	W/°C
E _{AS(4)}	Single Pulse Avalanche Energy	600	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 25 mA, V _{GS} = 0	24			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = 20 V V _{DS} = 20 V T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (5)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1	1.8		V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 30 A V _{GS} = 5 V I _D = 15 A		0.0052 0.007	0.006 0.011	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (5)	Forward Transconductance	V _{DS} = 10 V I _D = 30 A		40		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 15V f = 1 MHz V _{GS} = 0		2850 800 120		pF pF pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level =20 mV Open Drain		1		Ω

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ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		13 75		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 10\text{ V}$ $I_D = 60\text{ A}$ $V_{GS} = 10\text{ V}$		47.5 10 7	64	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 10\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		50 18	24.3	ns ns

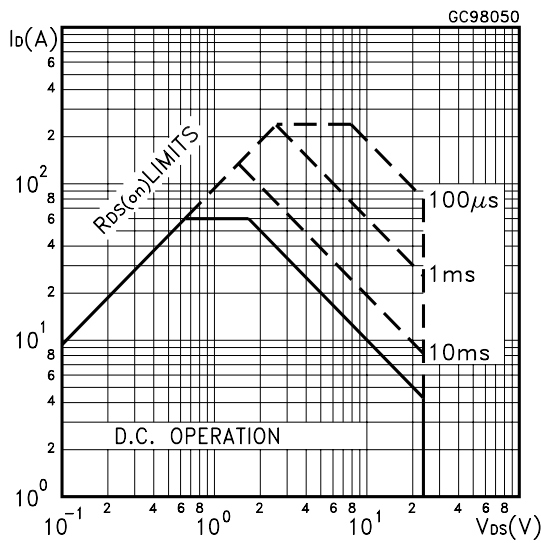
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(3)}$	Source-drain Current Source-drain Current (pulsed)				80 320	A A
$V_{SD}^{(5)}$	Forward On Voltage	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 60\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 16\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		35 35 2		ns nC A

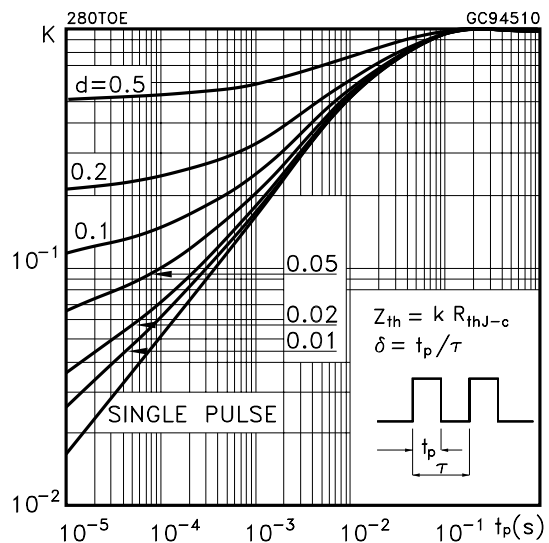
(1) Guaranteed when external $R_g = 4.7\ \Omega$ and $t_r < t_{rmax}$.
 (2) Value limited by wire bonding
 (3) Pulse width limited by safe operating area.
 (4) Starting $T_j = 25^\circ\text{C}$, $I_D = 30\text{A}$, $V_{DD} = 15\text{V}$

(5) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (6) $Q_{OSS} = C_{OSS} \cdot \Delta V_{in}$, $C_{OSS} = C_{gd} + C_{ds}$. See Appendix A
 (7) Gate charge for synchronous operation

Safe Operating Area

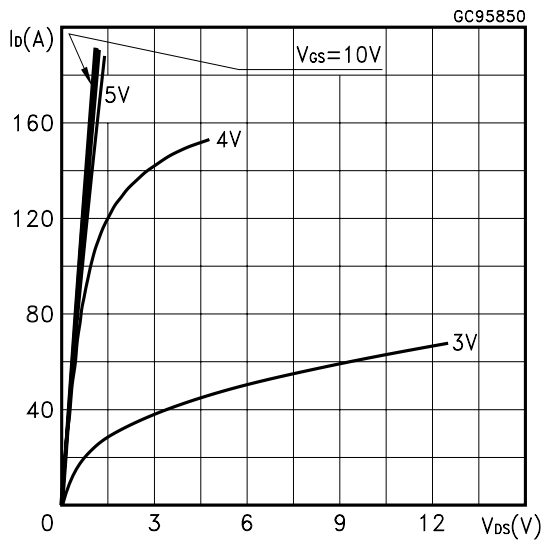


Thermal Impedance

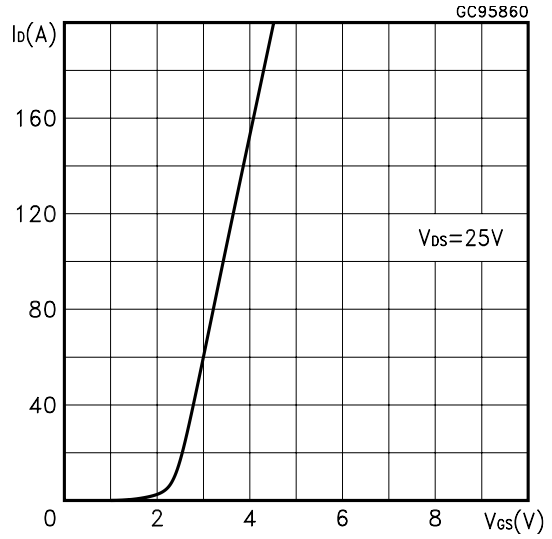


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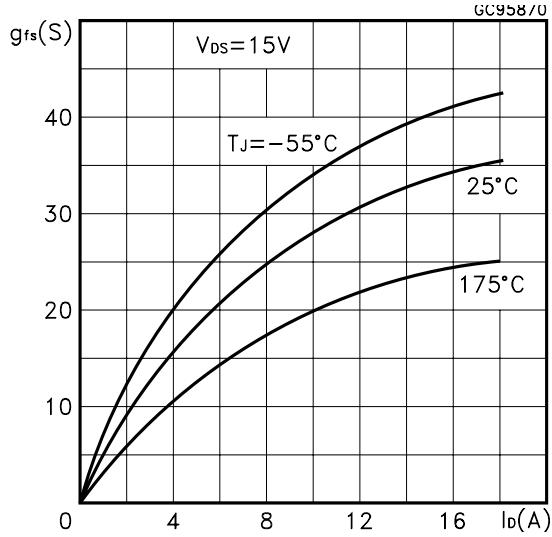
Output Characteristics



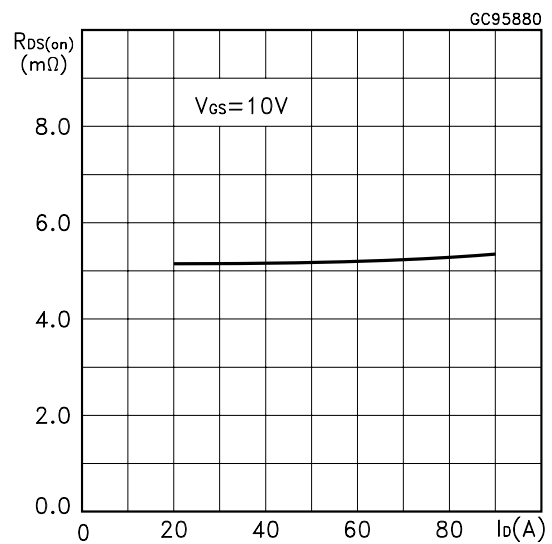
Transfer Characteristics



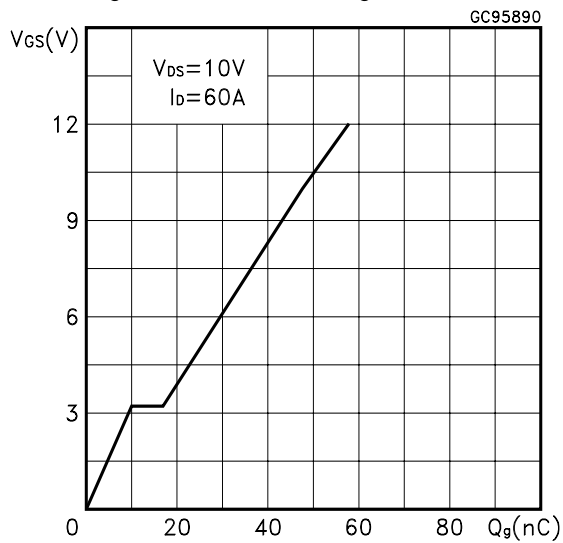
Transconductance



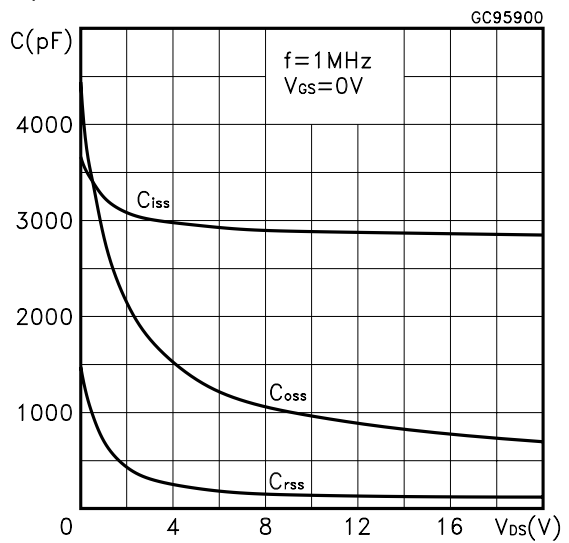
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

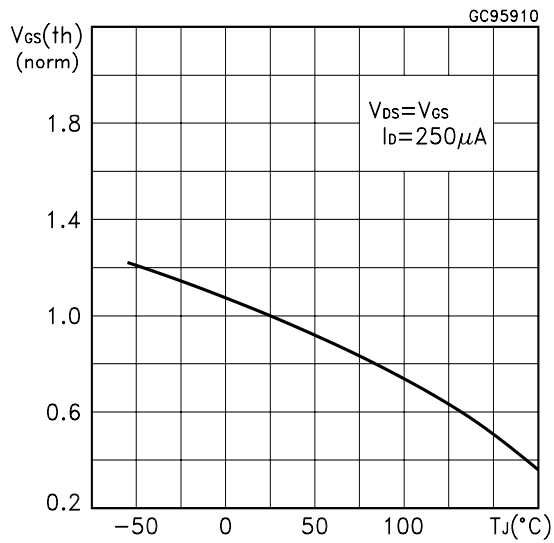


Capacitance Variations

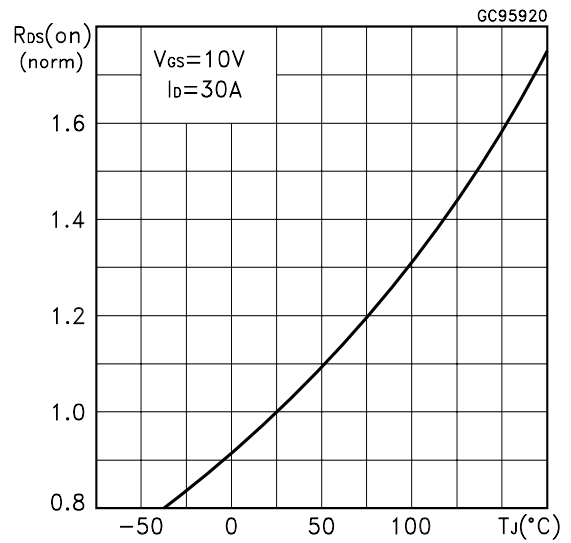


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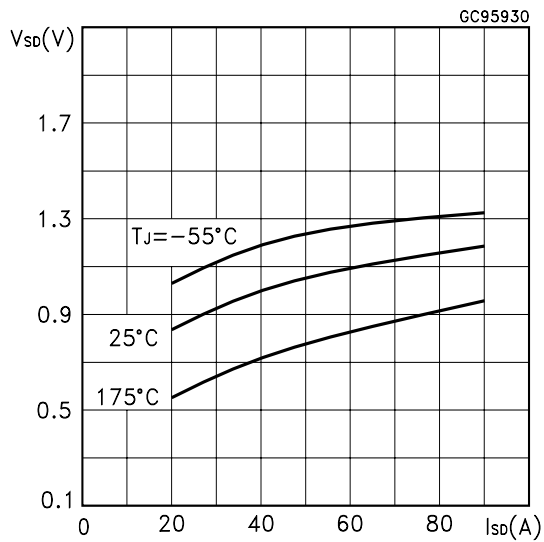
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.

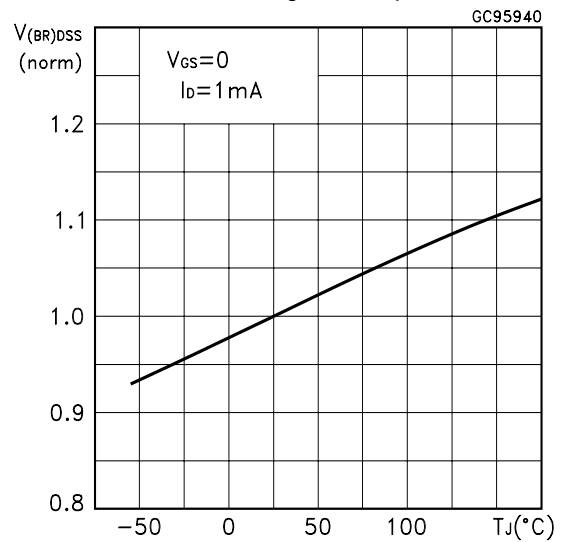


Fig. 1: Unclamped Inductive Load Test Circuit

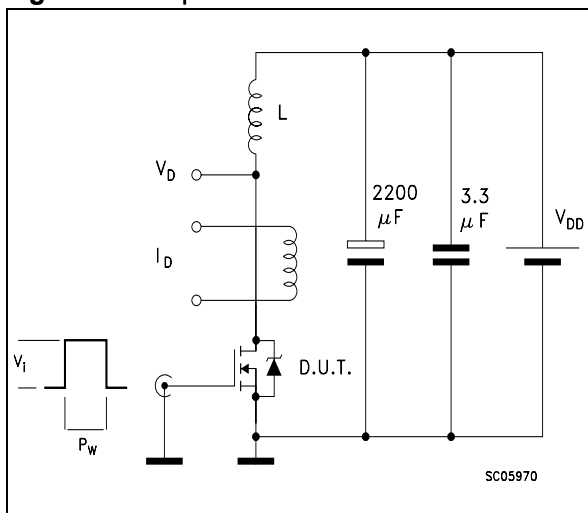


Fig. 2: Unclamped Inductive Waveform

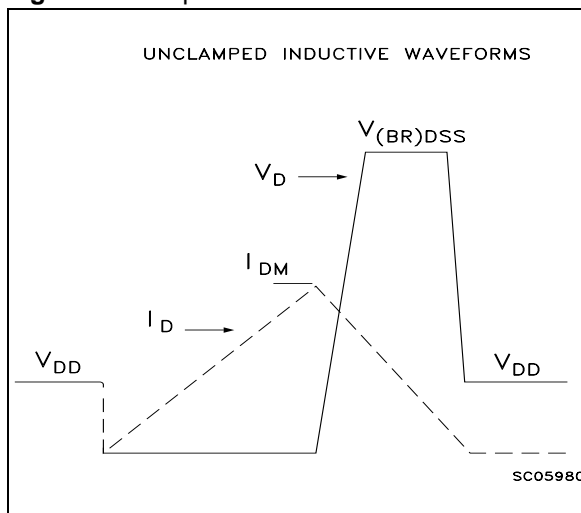


Fig. 3: Switching Times Test Circuits For Resistive Load

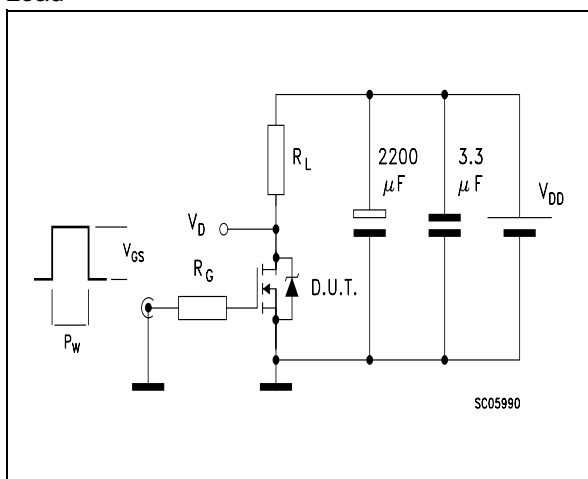


Fig. 4: Gate Charge test Circuit

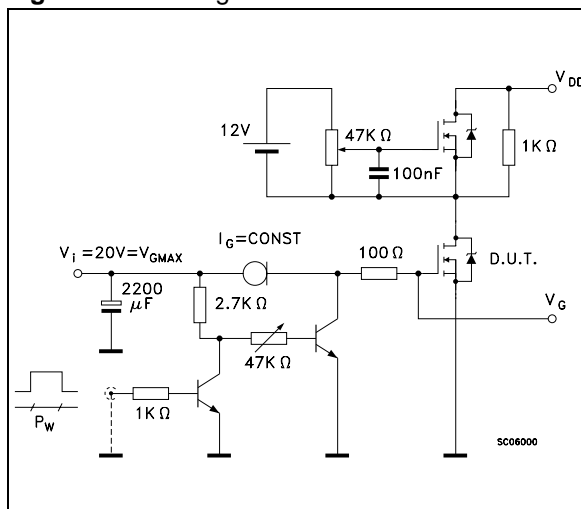
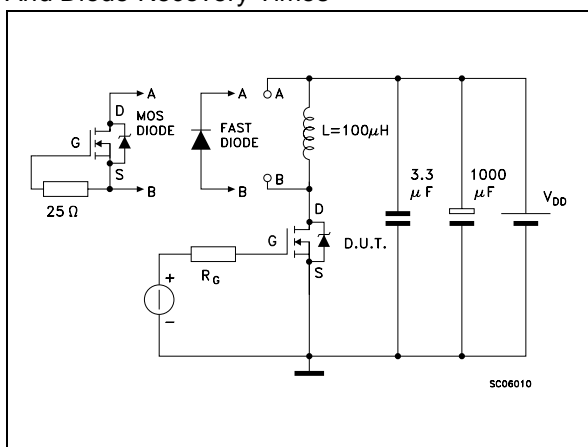
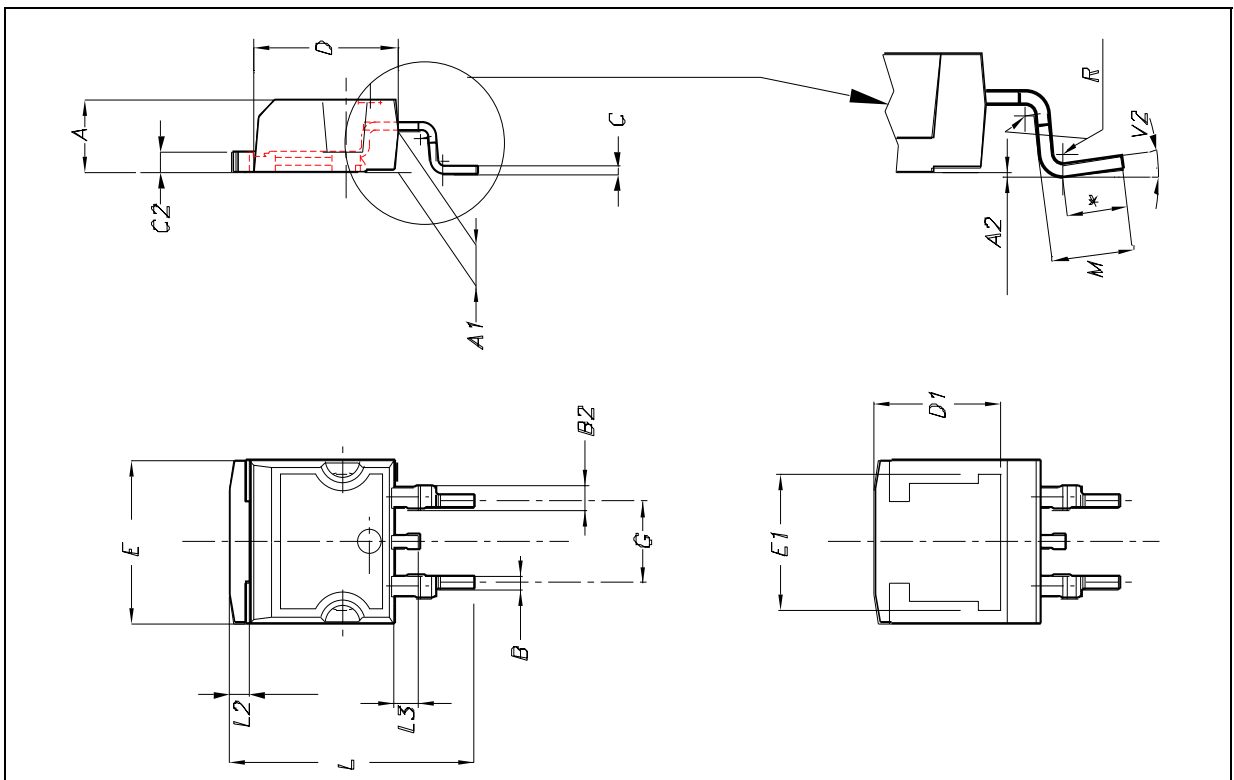


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

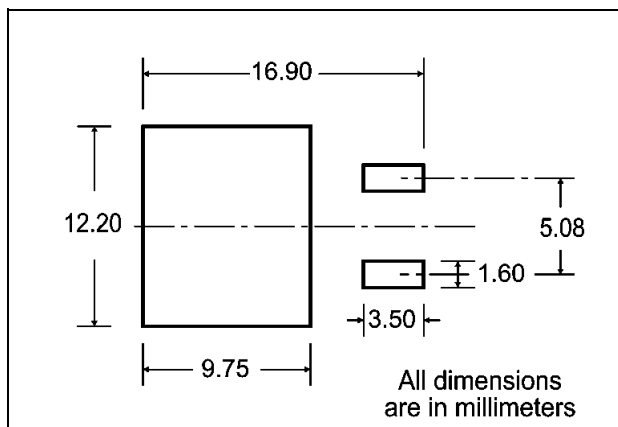


D²PAK MECHANICAL DATA

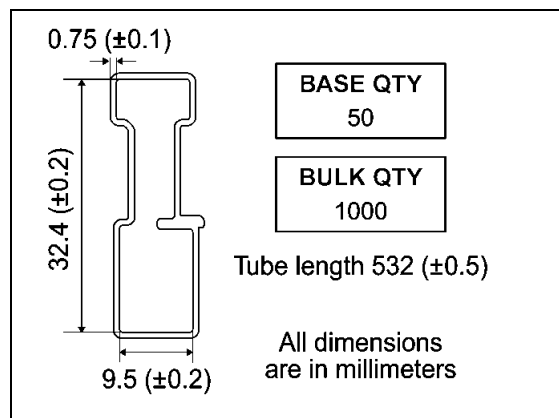
DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°	0°		4°



D2PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

Diagram showing the tape and reel shipment details. The reel diameter is A. The tape width is B. The distance from the center of the reel to the center of the tape is C. The distance from the center of the reel to the center of the tape slot is D. The distance from the center of the reel to the center of the tape slot is N. The distance from the center of the reel to the center of the tape slot is G, measured at the hub. The tape slot in the core for tape start has a width of 2.5 mm min. and a full radius. The access hole at the slot location has a diameter of 40 mm min.

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

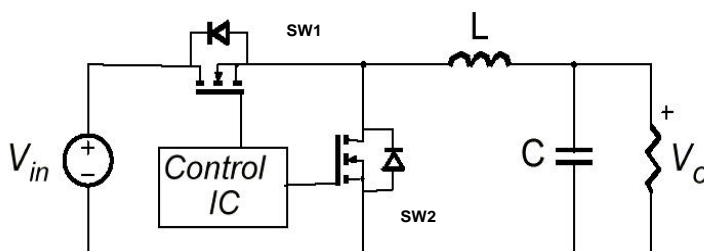
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

Diagram showing the tape mechanical data. The top cover tape has a thickness of K0. The distance from the center of the tape to the center of the cavity is D. The distance from the center of the tape to the center of the cavity is P2. The distance from the center of the tape to the center of the cavity is P0. The distance from the center of the tape to the center of the cavity is E. The distance from the center of the tape to the center of the cavity is F. The distance from the center of the tape to the center of the cavity is W. The distance from the center of the tape to the center of the cavity is A0. The distance from the center of the tape to the center of the cavity is P1. The center line of the cavity is shown. The user direction of feed is indicated. The bending radius is R min. The feed direction is indicated.

* on sales type

APPENDIX A

Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW₁ during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * d$	$R_{DS(on)SW2} * I_L^2 * (1-d)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$^1 V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_G)}$		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
PQoss	Output capacitance losses

¹ Dissipated by SW1 during turn-on

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