SIEMENS

3.3V SDRAM Modules HYS64Vx00(2)0G(C)D-10

144 pin SO-DIMM SDRAM Modules
16MB, 32MB, 64MB & 128 MB density

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual-In-Line Synchronous DRAM Modules for PC notebook applications
- One bank 2M x 64, 4M x 64, 8M x 64 and 16M x 64 non-parity module organisation
- Two bank 16M x 64 organisation
- Performance:

		-10	
		PC66	Units
f_{CK}	Clock frequency (max.)	66	MHz
t_{AC}	Clock access time $\overline{CAS}$ latency = 2 & 3	8	ns

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{CAS}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- 4096 refresh cycles every 64 ms
- Gold contact pad
- HYS64V8000GCD and HYS64V160(2)0GCD in COB techniques with 1” height only
- This SDRAM product familiy is intended to be fully pin and architecture compatible with the 144 pin SO-DIMM DRAM module family.

This SIEMENS module family are industry standard 144 pin 8-byte Synchronous DRAM (SDRAM) Small Outline Dual In-line Memory Modules (SO-DIMM) which are organised as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs use SDRAMs in TSOPII packages. Decoupling capacitors are mounted on the board.

The DIMMs use optional serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67,5 mm long footprint. This module family is available in conventional and COB module assembly technique.

Product Spectrum:

		SDRAMs used	RowAddr.	Bank Select	Column Addr.	Refresh	Period
2M x 64	HYS64V2000GD-10	8 2Mx8	11	BA0	9	4k	64 ms
4M x 64	HYS64V4000GD-10	4 4Mx16	12	BA0, BA1	8	4k	64 ms
8M x 64	HYS64V8000G(C)D-10	8 8Mx8	12	BA0, BA1	9	4k	64 ms
16M x 64	HYS64V1600GCD-10	16 16Mx4	12	BA0,BA1	10	4k	64 ms
16M x 64	HYS64V1620GCD-10	16 8M x 8	12	BA0,BA1	9	4k	64 ms

Card Dimensions:

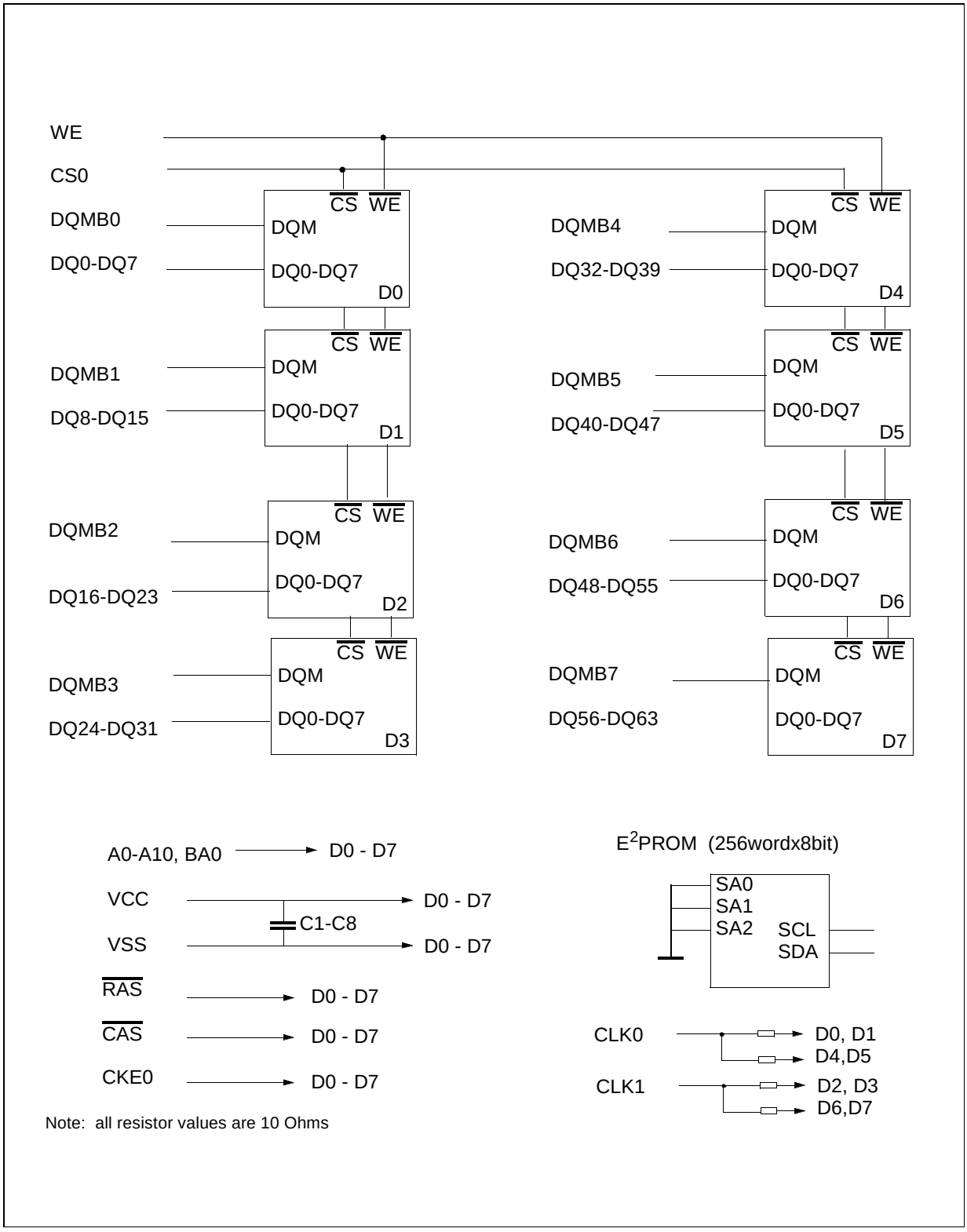
Organisation	PCB-Board	L x H x T [mm]
2M x 64	L-DIM-144-6	67.60 x 25.40 x 3.80
4M x 64	L-DIM-144-7	67.60 x 25.40 x 3.80
8M x 64	L-DIM-144-8	67.60 x 31.75 x 3.80
8M x 64 COB	L-DIM-144-C6	67.60 x 25.40 x 3.80
16M x 64 COB	L-DIM-144-C7	67.60 x 25.40 x 3.80

Pin Names

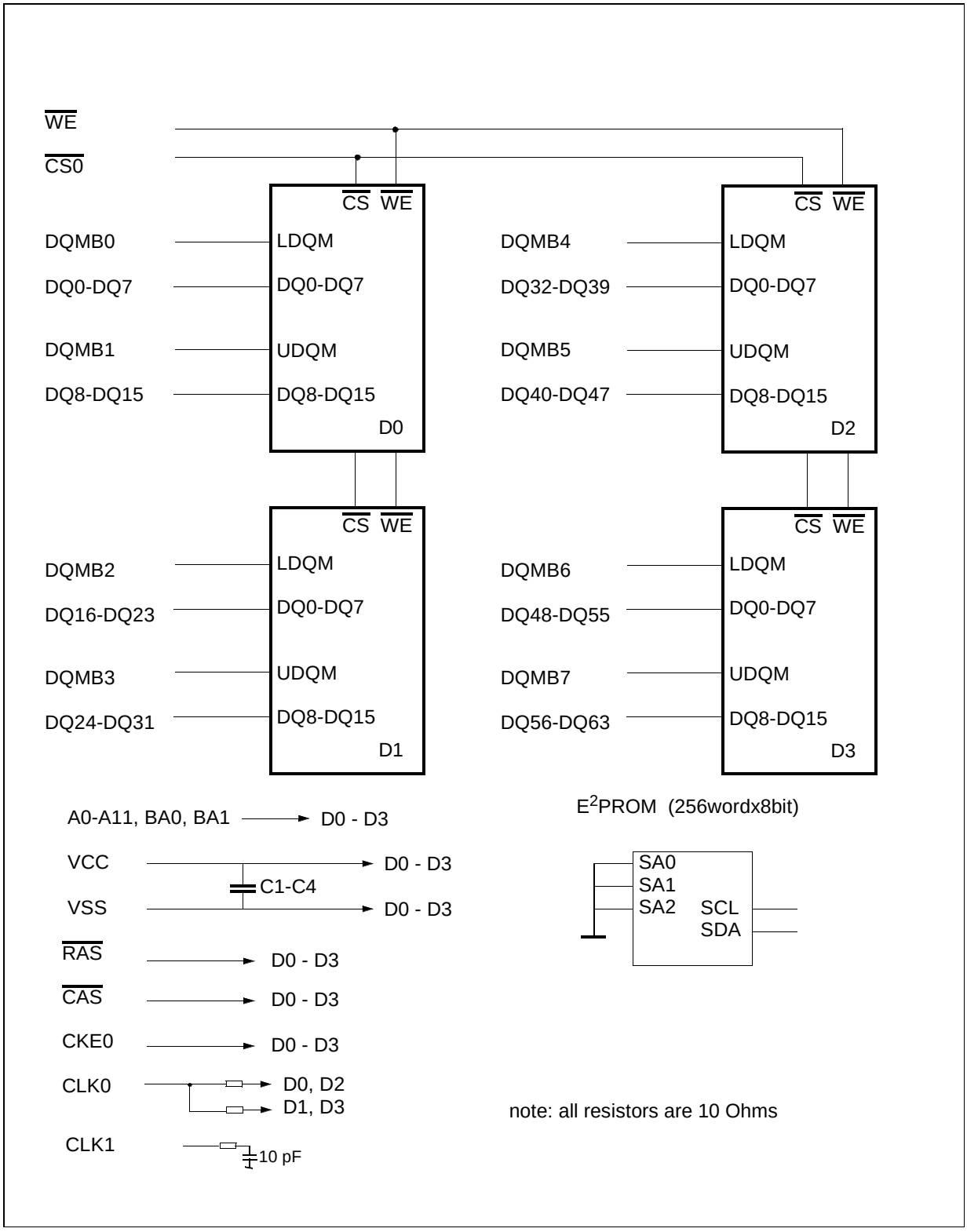
A0-A10	Address Inputs for 2M x 64 modules
A0-A11	Address Inputs for 4M x 64, 8M x 64 & 16M x 64 modules
BA0	Bank Select for 2M x 64 modules
BA0,BA1	Bank Selects for 4M x 64, 8M x 64& 16M x 64 modules
DQ0 - DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read / Write Input
$\overline{CKE0}$	Clock Enable
CLK0	Clock Input
DQMB0 - DQMB7	Data Mask
$\overline{CS0}$ - $\overline{CS3}$	Chip Select
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

Pin Configuration

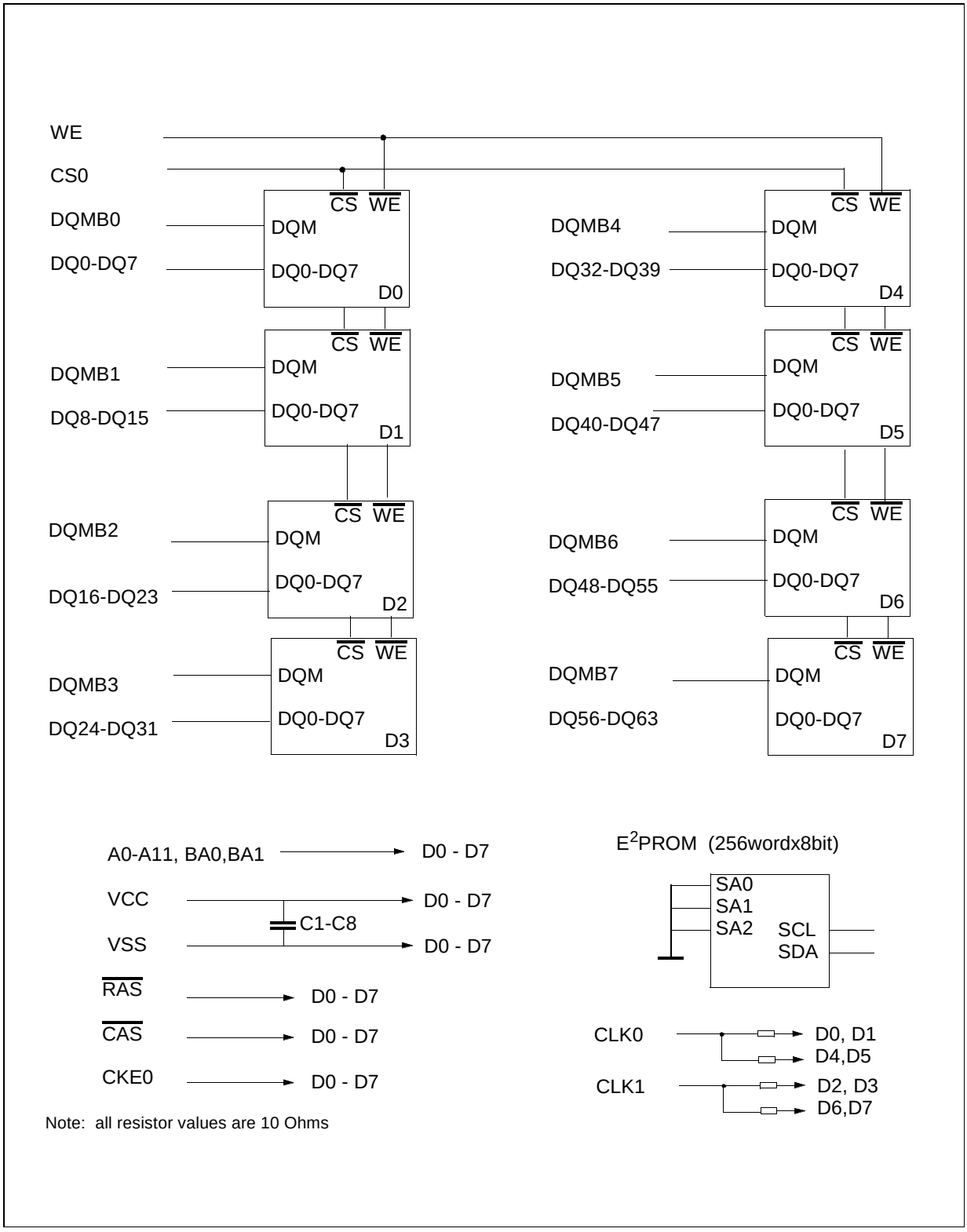
PIN #	Front Side	PIN #	Back Side		PIN #	Front Side	PIN #	Back Side
1	VSS	2	VSS		73	NC	74	CKL1
3	DQ0	4	DQ32		75	Vss	76	Vss
5	DQ1	6	DQ33		77	NC	78	NC
7	DQ2	8	DQ34		79	NC	80	NC
9	DQ3	10	DQ35		81	Vcc	82	Vcc
11	VCC	12	Vcc		83	DQ16	84	DQ48
13	DQ4	14	DQ36		85	DQ17	86	DQ49
15	DQ5	16	DQ37		87	DQ18	88	DQ50
17	DQ6	18	DQ38		89	DQ19	90	DQ51
19	DQ7	20	DQ39		91	Vss	92	Vss
21	Vss	22	Vss		93	DQ20	94	DQ52
23	DQMB0	24	DQMB4		95	DQ21	96	DQ53
25	DQMB1	26	DQMB5		97	DQ22	98	DQ54
27	Vcc	28	Vcc		99	DQ23	100	DQ55
29	A0	30	A3		101	Vcc	102	Vcc
31	A1	32	A4		103	A6	104	A7
33	A2	34	A5		105	A8	106	BA0
35	Vss	36	Vss		107	Vss	108	Vss
37	DQ8	38	DQ40		109	A9	110	BA1
39	DQ9	40	DQ41		111	A10	112	A11
41	DQ10	42	DQ42		113	Vcc	114	Vcc
43	DQ11	44	DQ43		115	DQMB2	116	DQMB6
45	Vcc	46	Vcc		117	DQMB3	118	DQMB7
47	DQ12	48	DQ44		119	Vss	120	Vss
49	DQ13	50	DQ45		121	DQ24	122	DQ56
51	DQ14	52	DQ46		123	DQ25	124	DQ57
53	DQ15	54	DQ47		125	DQ26	126	DQ58
55	Vss	56	Vss		127	DQ27	128	DQ59
57	NC	58	NC		129	Vcc	130	Vcc
59	NC	60	NC		131	DQ28	132	DQ60
61	CKL0	62	CKE0		133	DQ29	134	DQ61
63	Vcc	64	Vcc		135	DQ30	136	DQ62
65	$\overline{\text{RAS}}$	66	$\overline{\text{CAS}}$		137	DQ31	138	DQ63
67	$\overline{\text{WE}}$	68	$\overline{\text{CKE1}}$		139	Vss	140	Vss
69	$\overline{\text{CS0}}$	70	(A12)		141	SDA	142	SCL
71	NC ($\overline{\text{CS1}}$)	72	(A13)		143	Vcc	144	Vcc



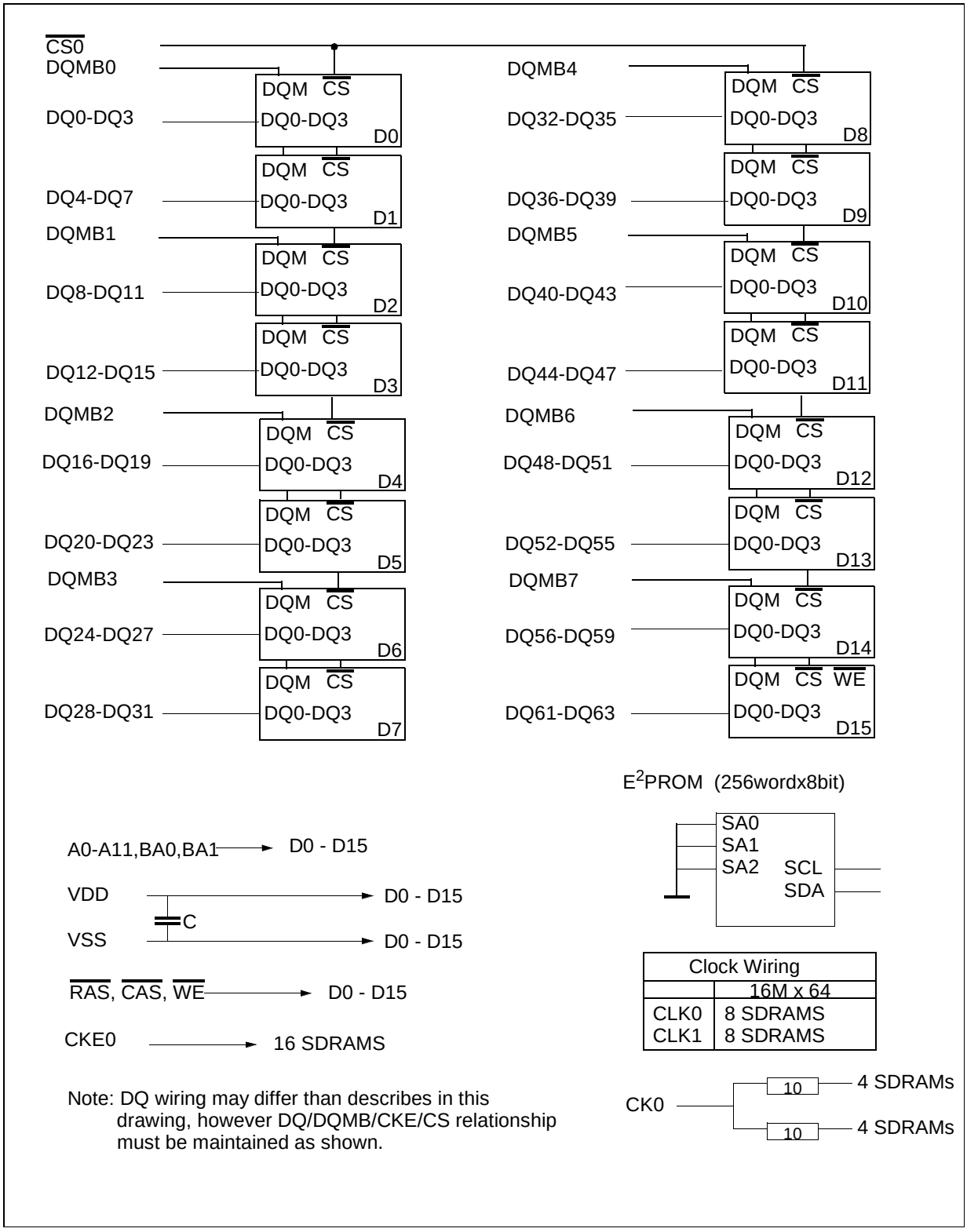
Block Diagram for 2M x 64 SDRAM - DIMM module



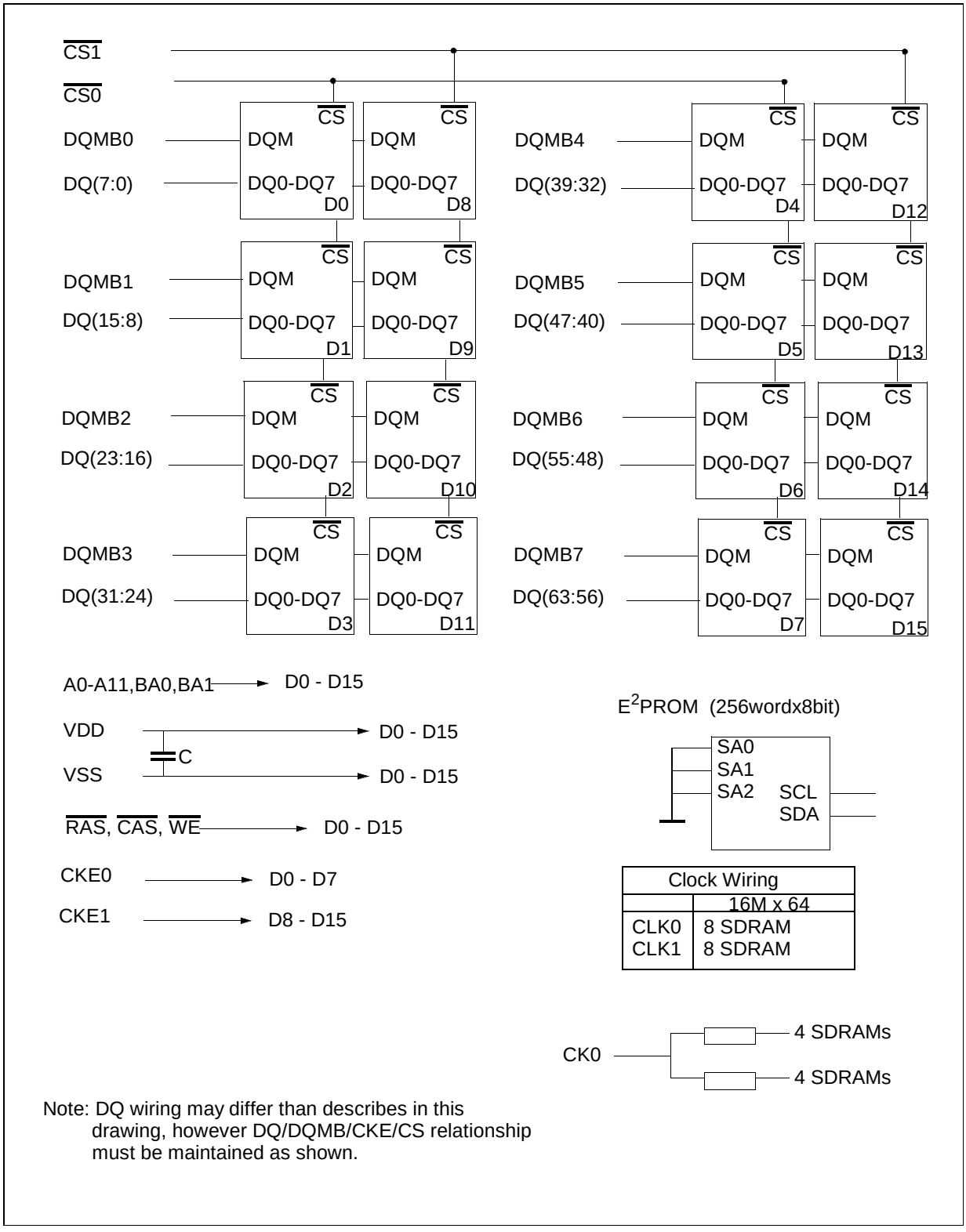
Block Diagram for 4M x 64 SDRAM - DIMM module



Block Diagram for 8M x 64 SDRAM DIMM - Module



Block Diagram for one bank 16M x 64 SDRAM DIMM - Module (16M x 4 based)



Note: DQ wiring may differ than describes in this drawing, however DQ/DQMB/CKE/CS relationship must be maintained as shown.

Block Diagram for two bank 16M x 64 SDRAM DIMM - Module (8M x 8 based)

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; $V_{DD,}V_{DDQ}$ = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	Vcc+0.3	V
Input low voltage	V_{IL}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 20	20	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 20	20	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values				Unit
		2M x 64 max.	4M x 64 max.	8M x 64 max.	16Mx 64 max.	
Input capacitance (A0 to A11, BA0, BA1)	C_{I1}		18		45	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0)	C_{I2}		18		50	pF
Input Capacitance (CLK0, CLK1)	C_{I3}		25		45	pF
Input capacitance (CS0)	C_{I4}		18		45	pF
Input capacitance (DQMB0-DQMB7)	C_{I5}		7		10	pF
Input / Output capacitance (DQ0-DQ63)	C_{IO}		8		9	pF
Input Capacitance (SCL,SA0-2)	C_{sc}		8		8	pF
Input/Output Capacitance	C_{sd}		10		10	pF

AC Characteristics 1)2)

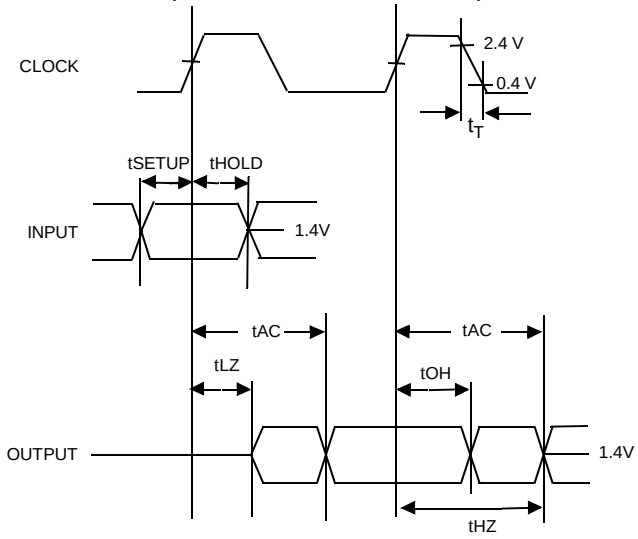
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V ± 0.3 V, t_T = 1 ns

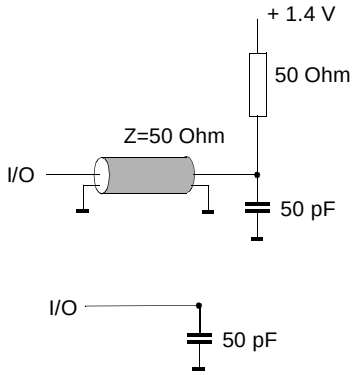
Parameter	Symbol	Limit Values		Unit	Note
		-10			
		min.	max.		
Clock and Clock Enable					
Clock Cycle Time	t_{CK}				
$\overline{CAS}$ Latency = 3		10		ns	
$\overline{CAS}$ Latency = 2		15		ns	
System Frequency	f_{CK}				
$\overline{CAS}$ Latency = 3		–	100	MHz	
$\overline{CAS}$ Latency = 2		–	66	MHz	
Clock Access Time	t_{AC}				
$\overline{CAS}$ Latency = 3		–	8	ns	2, 4,
$\overline{CAS}$ Latency = 2		–	8	ns	
Clock High Pulse Width	t_{CH}	3	–	ns	6
Clock Low Pulse Width	t_{CL}	3	–	ns	6
Input Setup time	t_{CS}	3	–	ns	7
Input Hold Time	t_{CH}	1	–	ns	7
CKE Setup Time (Power down mode)	t_{CKSP}	3	–	ns	8
CKE Setup Time (Self Refresh Exit)	t_{CKSR}	8	–	ns	9
Transition time (rise and fall)	t_T	1	–	ns	
Common Parameters					
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	30	–	ns	2 CLK
Cycle Time	t_{RC}	75	–	ns	7 CLK
Active Command Period	t_{RAS}	45	–	ns	3 CLK
Precharge Time	t_{RP}	30	–	ns	2 CLK
Bank to Bank Delay Time	t_{RRD}	20	–	ns	1 CLK
$\overline{CAS}$ to $\overline{CAS}$ delay time (same bank)	t_{CCD}	1	–	CLK	
Refresh Cycle					
Self Refresh Exit Time	t_{SREX}	2CLK +tRC		ns	9)
Refresh Period (4096 cycles)	t_{REF}	–	64	ms	8)

Parameter	Symbol	Limit Values		Unit	Note
		-10			
		min.	max.		
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	2, 4
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	10	ns	10
DQM Data Out Disable Latency	t_{DQZ}	2		CLK	
Write Cycle					
Data Inut to Precharge (write recovery)	t_{WR}	2	–	CLK	
Data In to Active / Refresh	t_{DAL}	5	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	CLK	

Notes:

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{il} = 0.4 V and V_{ih} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shown.Specified tac and toh parameters are measured with a 50





Measurement conditions for tac and toh

pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.

3. If clock rising time is longer than 1ns, a time (t_T -0.5) ns has to be added to this parameter.
4. If t_T is longer than 1ns, a time (t_T -1) ns has to be added to this parameter.
5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to “wake-up“ the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
8. t_{DAL} is equivalent to t_{DPL} + t_{RP}.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

Serial Presence Detects:

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus)

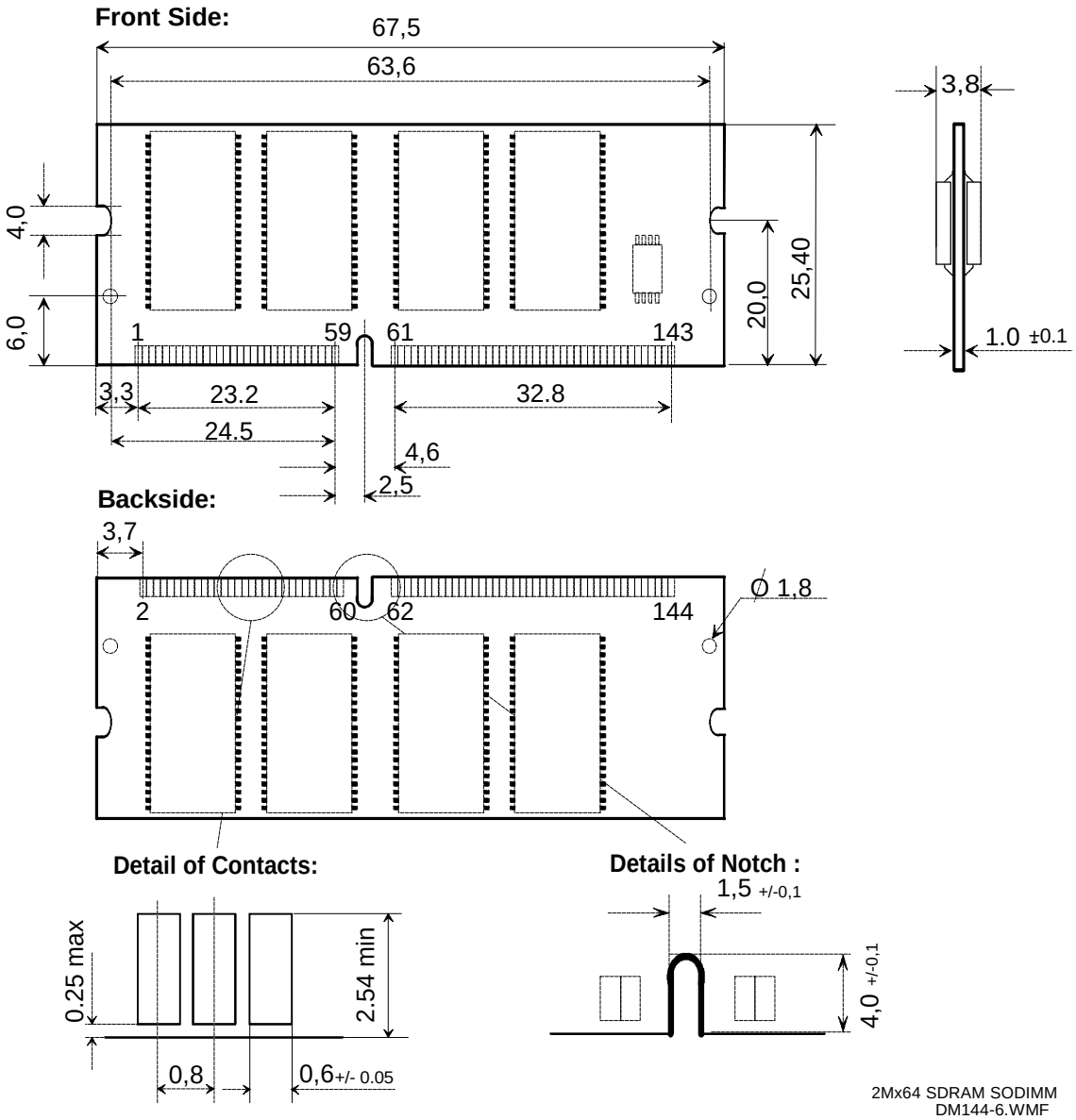
SPD-Table:

Byte#	Description	SPD Entry Value	Hex				
			2Mx64 -10	4Mx64 -10	8Mx64 -10	16Mx64 -10	16Mx64 -10
0	Number of SPD bytes	128	80	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04	04
3	Number of Row Addresses (without BS)		0B	0C	0C	0C	0C
4	Number of Column Addresses		09	08	09	09	0A
5	Number of DIMM Banks	1	01	01	01	02	01
6	Module Data Width	64	40	40	40	40	40
7	Module Data Width (cont'd)	0	00	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	8.0 ns	80	80	80	80	80
11	Dimm Config (Error Det/Corr.)	none	00	00	00	00	00
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80	80
13	SDRAM width, Primary		08	10	08	08	04
14	Error Checking SDRAM data width	n/a / x8	00	00	00	00	00
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F	8F
17	Number of SDRAM banks	2	02	04	04	04	04
18	Supported CAS Latencies	2, & 3	06	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/ non reg.	00	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06	06
23	SDRAM Cycle Time at CL = 2	15.0 ns	F0	F0	F0	F0	F0
24	SDRAM Access Time from Clock at CL=2	8.0 ns	80	80	80	80	80
25	SDRAM Cycle Time at CL = 1	not supported	FF	FF	FF	FF	FF
26	SDRAM Access Time from Clock at CL=1	not supported	FF	FF	FF	FF	FF
27	Minimum Row Precharge Time	30 ns	1E	1E	1E	1E	1E

SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex				
			2Mx64 -10	**4Mx64 -10**	**8Mx64 -10**	**16Mx64 -10**	**16Mx64 -10**
28	Minimum Row Active to Row Active delay	20 ns	14	14	14	14	14
29	Minimum RAS to CAS delay	30 ns	1E	1E	1E	1E	1E
30	Minimum Ras pulse width	45 ns	2D	2D	2D	2D	2D
31	Module Bank Density (per bank)		04	08	10	10	20
32	SDRAM input setup time	3 ns	30	25	25	25	25
33	SDRAM input hold time	1 ns	10	10	10	10	10
34	SDRAM data input setup time	3 ns	30	25	25	25	25
35	SDRAM data input hold time	1 ns	10	10	10	10	10
36-61	Superset information		FF	FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12	12
63	Checksum for bytes 0 - 62		91	89	8A	8B	97
64-125	Manufactures's information (optional)		FF	FF	FF	FF	FF
126	Frequency Specification	PC66	66	66	66	66	66
127	Details		C7	87	C7	C7	C7
128+	Unused storage locations		FF	FF	FF	FF	FF

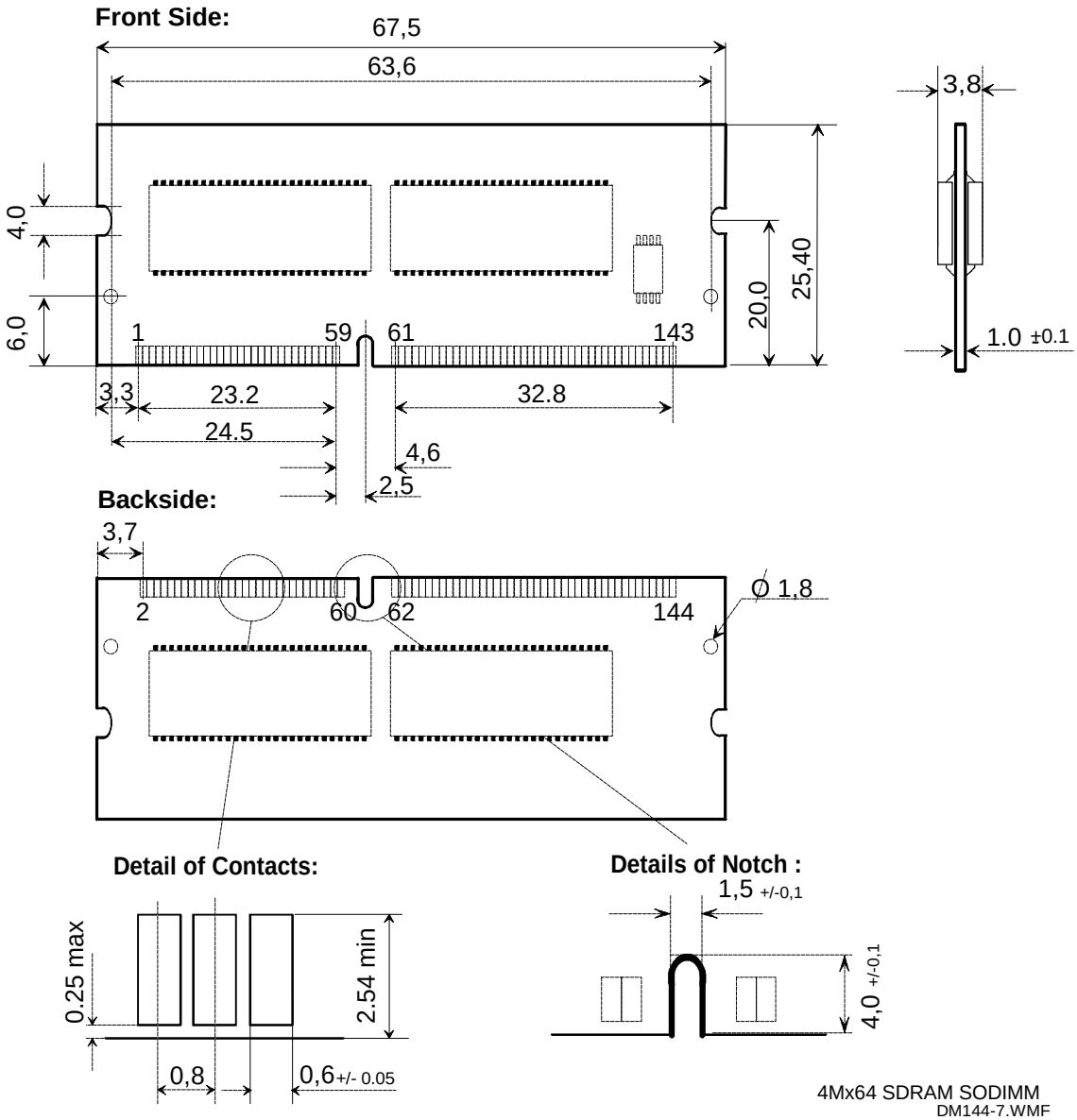
L-DIM-144-6
16 MByte SO-DIMM Module package
(144 pin, dual read-out, single in-line memory module)



2Mx64 SDRAM SODIMM
DM144-6.WMF

preliminary drawing

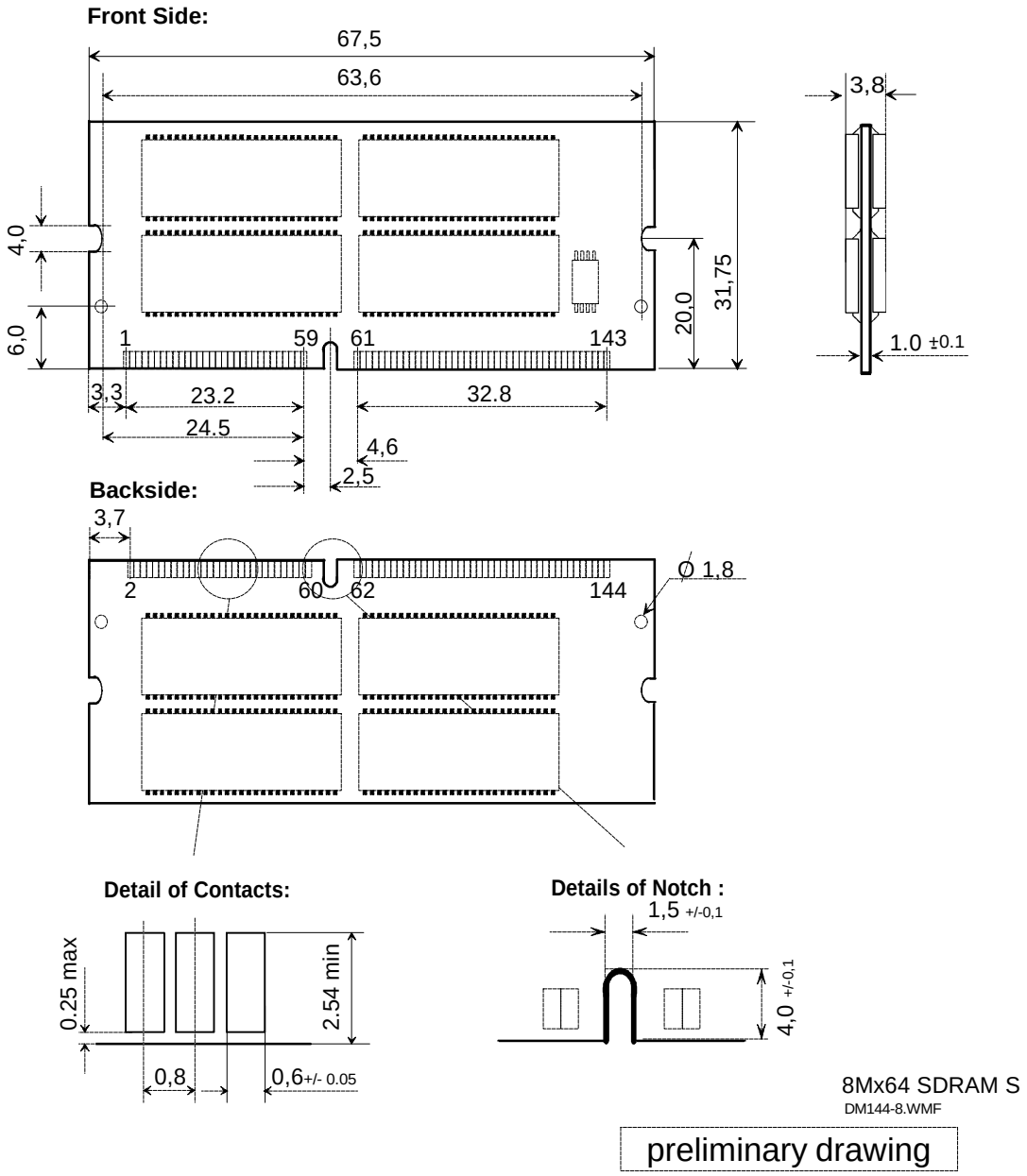
L-DIM-144-7
32 MByte SO-DIMM Module package
(144 pin, dual read-out, single in-line memory module)



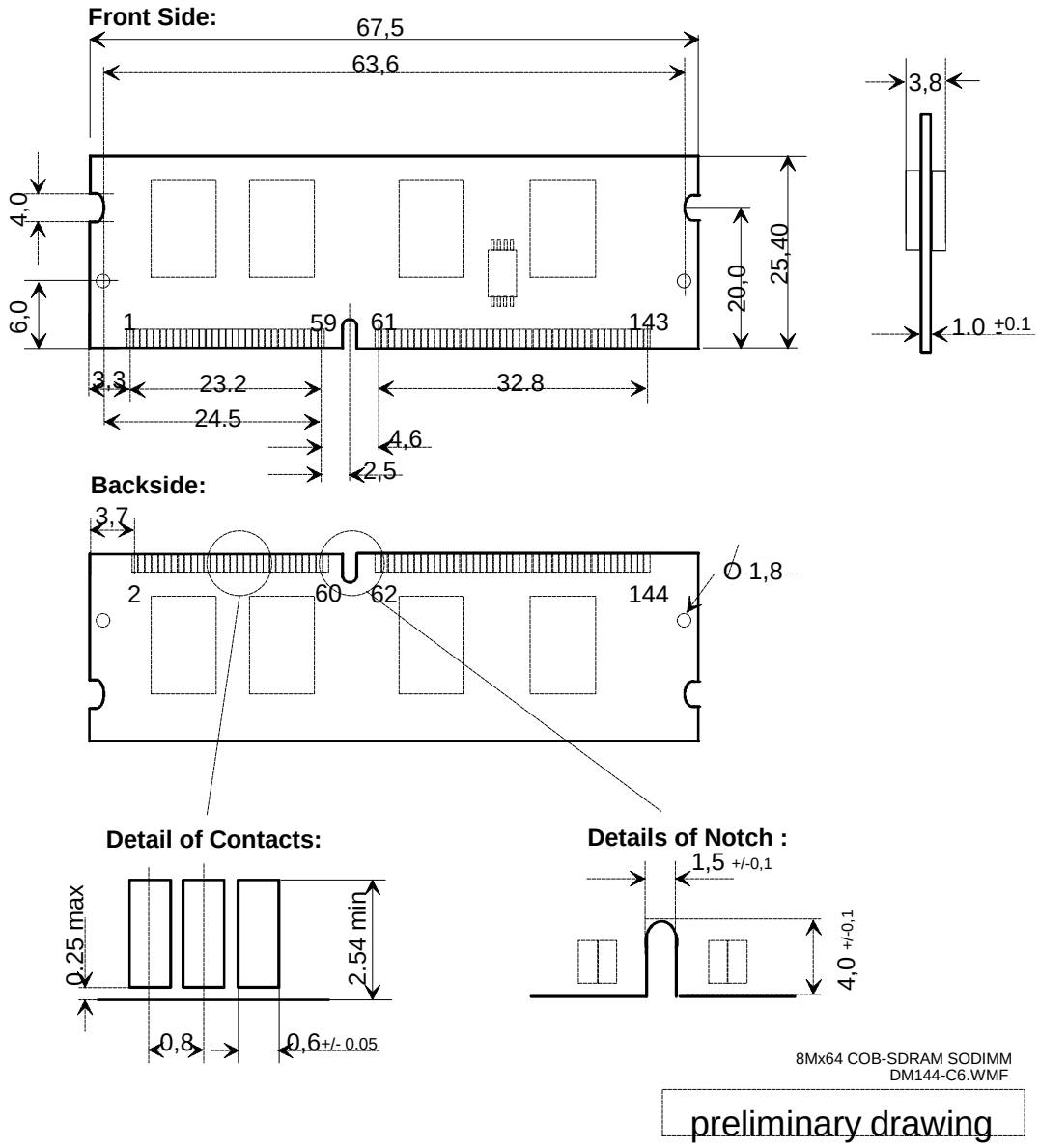
4Mx64 SDRAM SODIMM
DM144-7.WMF

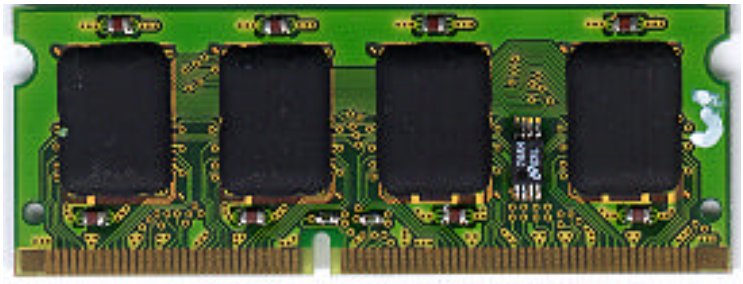
preliminary drawing

L-DIM-144-8
64 MByte SO-DIMM Module package
(144 pin, dual read-out, single in-line memory module)



L-DIM-144-C6
64 MByte COB SO-DIMM Module package
(144 pin, dual read-out, single in-line memory module)





L-DIM-144-C7
128 MByte COB SO-DIMM Module package
(144 pin, dual read-out, single in-line memory module)