CIRRUS LOGIC®

Errata: CS42406 Silicon Errata

Rev CB Silicon

- The left channel of the ADC is delayed by one ADC_LRCK cycle. This is true for all speed modes, in both Master and Slave. Therefore, the group delay for the left channel is increased by one ADC_LRCK cycle:

	Left Channel Group Delay	Right Channel Group Delay
Single-Speed Mode	13/Fs	12/Fs
Double-Speed Mode	10/Fs	9/Fs
Quad-Speed Mode	6/Fs	5/Fs

- Analog performance of the ADC does not meet datasheet specifications. The affected specifications are listed below:

Parameter	Datasheet Specification	Current Silicon Performance
THD+N (-1dBFS Input)	-95 dB	-80 dB
Dynamic Range (A-wgted)	102 dB	98 dB
Interchannel Isolation	90 dB	73 dB

Note: Performance shown is for Single-Speed Mode, Fs = 48 kHz, VA = 5.0 V.

- A ± 10mA current source or sink on the MCLK, AINL, and AINR pins (pins 3, 24, and 26 respectively) may cause an internal latch-up condition. The device will recover if the current is then dropped below ± 10mA.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com.

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