
EMC Improvement Guidelines



Introduction

High-speed digital Integrated Circuits operate in frequency bands where passive components (PCB, decoupling capacitors, PCB connections, packages, ...) cannot be considered as ideal – and to the contrary contain, parasitic elements (inductance, resistance, ..). Because their impedances depend on the frequency, the emission levels generated by voltage and current drops may not be compliant to the different EMC standards. It is impossible to predict the compliance of a system. However, it is possible to reduce the risk by implementing rules and design techniques in most applications. This application note gives a brief checklist of major points which can degrade EMC and demonstrates how some basic techniques can help to reduce emission levels and harden the electronic system.

8051

Microcontrollers

Application Note

EMC Definitions

Some basic terms are used in this application note and are explained hereafter:

- **EMC:** *Electromagnetic Compatibility*, the ability of a product to coexist in its intended electromagnetic environment without causing or suffering functional degradation or damage.
- **EMI:** *Electromagnetic Interference*, a process by which disruptive electromagnetic energy is transmitted from one electronic device to another via radiated or conducted paths (or both).
- **Radiated:** Energy transmitted by the air via antenna or loops.
- **Conducted:** Energy transmitted via solid medium like cables, PCB connections, packages,....

There are three elements in the EMC model to analyze and understand an EMC problem:

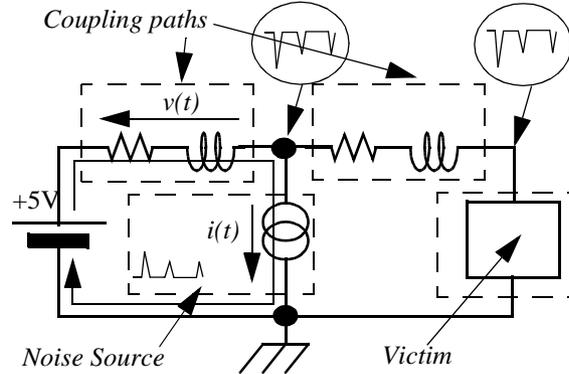
- A **Noise source**, a source that generates an electromagnetic perturbation,
- A **victim**, an electronic device that receives a perturbation which causes dysfunctionalities,
- A **coupling path**, a medium that transmits energy from the noise source to the victim.

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Figure 1 shows the topology of an EMC environment. A noise source drives a current $i(t)$. This current flows through the left coupling path (PCB connection for example) and causes voltage drops. This voltage perturbation is transmitted to the victim through the right coupling path and can cause a dysfunctionality if the level is high enough.

Figure 1. Elements of EMC Environment



To significantly improve the EMC quality of the design the EMC environment through these elements have to be analyzed.

Basic Checklist to be Compliant with EMC

The basic rules to decrease the conducted and radiated emissions through the power-supply are to:

- Reduce the speed of the system:
 - Choose the lowest system clock frequency,
 - Adapt the technology to the system constraints.
- Reduce all the magnetic loops of the Printed Circuit Board:
 - Decrease the surface of the magnetic loops,
 - Maintain the signal trace closed to the ground,
 - Shorten the loops around the oscillator and crystal.
- Cancel H field:
 - Opposite magnetic loops,
 - Choose a package with a VCC and VSS pins close together,
 - Choose a package with several VSS and VCC pins connected in opposite side.
- Reduce the parasitic inductance of all devices (PCB traces, package, capacitors,...):
 - Increase the PCB connection widths,
 - Use ground and power planes,
 - Adapt the decoupling capacitors to the working frequency of IC's,
 - Shorten the capacitor connection length,
 - Select the smaller package.
- Reduce the Equivalent Series Resistance (ESR):
 - Put identical capacitors in parallel to reduce the ESR,
 - Choose COG and NPO dielectric types.

All these rules are detailed in the following sections.

Reduce the Speed of the System

Maintain the System Clock Frequency as low as Possible

A key parameter to improve EMC is to reduce the working frequency of the system. The system clock frequency is defined by evaluating the following guidelines:

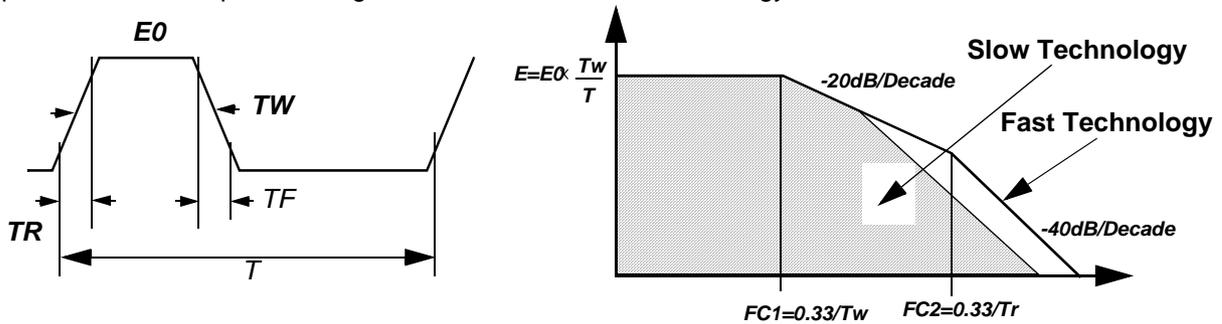
- the real-time events such as interrupts, serial link,....
- the CPU time to process all the tasks attached to these events,
- the most critical window where the CPU has to process a sequence of real-time events,
- the clock frequency to achieve this window time.

and then increase the clock frequency by 20 to 30% to have a good margin.

Adapt the Technology to the System Constraints

Another key parameter to reduce EMI is to select the slowest technology of the components used in the system (address latch, memories, buffers,...). The spectral envelope has two cut-off frequencies and is shown on Figure 2. The first one (FC1) depends on the pulse width of the signal and the second (FC2) depends on the sharpness of the transition mainly due to the technology. The slower the technology lower the EMI.

Figure 2. Spectrum of the Trapezoidal Signal for a Fast and Slow Technology



A timing analysis of the system has to be done to choose the slowest technology of the components to determine the electrical characteristics of such devices. When the maximum operation frequency limit is divided by two, EMI is reduced by 12 dB.

Reduce all the Magnetic Loops of the Printed Circuit Board

Decrease the Magnetic Loop Surface

A current flowing around a loop generates a magnetic field (H) proportional to the area of the loop. The following equations give the mathematical expressions when the observation distance is in the near and far field conditions:

$$H_{near} A/m = I \times \frac{S}{4 \times \pi \times D^3}, \quad H_{far} A/m = \pi \times I \times \frac{S}{\lambda^2 \times D}$$

where,

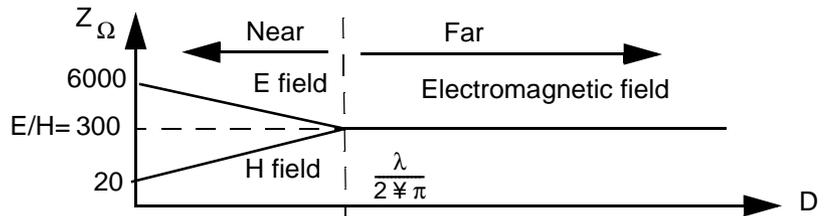
$I(A)$: loop current, $S(m^2)$: loop surface $D(m)$: observation distance $\lambda(m)$: current wavelength.

The near field and far condition is expressed by the following formula:

$$\frac{D}{\lambda} = \frac{1}{2 \times \pi}$$

This ratio indicates the transition where the emission is in far field or in near field conditions (see Figure 3). The far field condition is a specific distance where the electrical and magnetic fields are coupled and perpendicular. In that condition the ratio E/H is the intrinsic impedance of free space equal to 300Ω. In the near field condition the nature of the fields depends on the connection impedance. For a high impedance ($Z \gg 300 \Omega$) the field is electric and magnetic if impedance is low ($Z \ll 300 \Omega$).

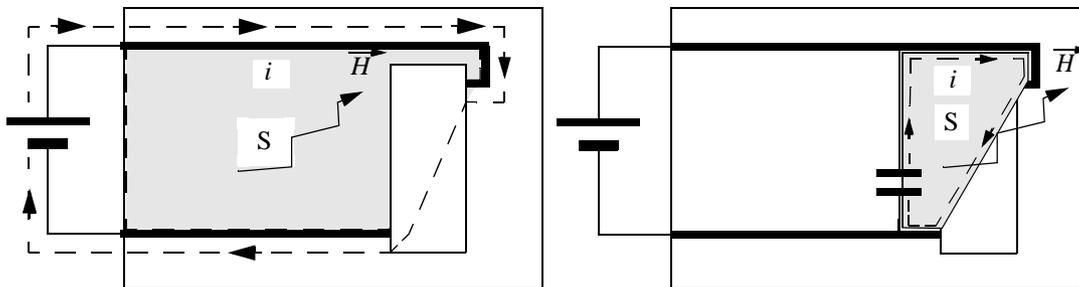
Figure 3. Far and Near Field Conditions



For example at 3 meters, $F = 30 \text{ MHz}$ and $I = 0.1 \text{ A}$, the magnetic field intensity is $-19.6 \text{ dB}\mu\text{A}$ for a 1 cm^2 surface loop and $-13.6 \text{ dB}\mu\text{A}$ when the loop surface is doubled. Reducing the surface by a factor of two leads to decrease H field by a factor of 6dB. This can be achieved by carefully checking the PCB lay-out.

The decoupling capacitor acts in this way as well. It supplies locally the fast transient current and reduces the length of the current discharging path. It contributes to reduce the closed contour taken by the current and finally the radiation surface as shown in Figure 4.

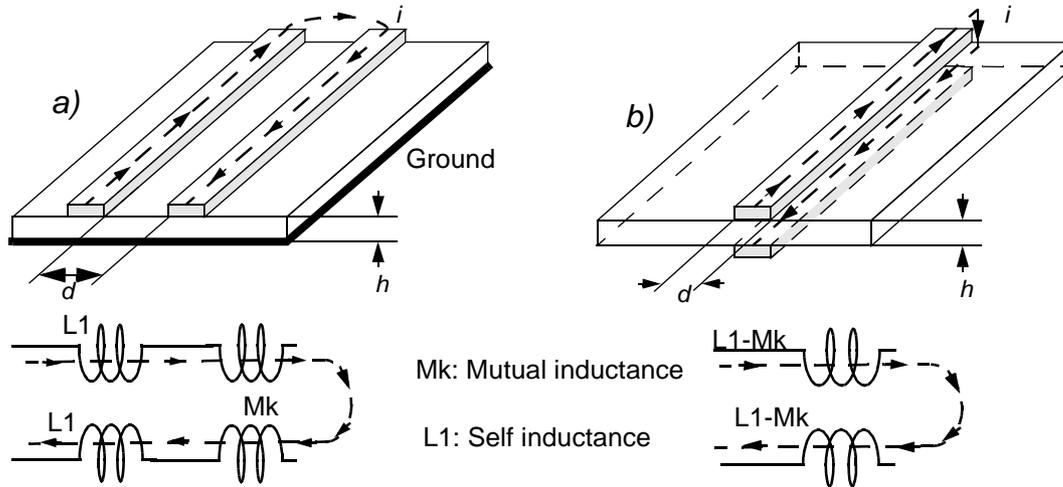
Figure 4. Decoupling Capacitor Reduces the Magnetic Field and the Loop Surface



Maintain the Signal Trace close to the Ground

To maintain a low parasitic inductance of a signal trace, the distance to the ground has to be maintained short. The parasitic inductance of two parallel conductors carrying uniform current in opposite direction consists of self and mutual inductances as shown in Figure 5. This figure depicts the two kinds of parallel conductors which can be found and their electrical equivalent model.

Figure 5. Structure of a Parasitic Inductance



The total inductance for such topology is equal to:

$$LT = L1 + L2 - 2 \times Mk$$

$$Mk = k \times \sqrt{L1 \times L2}$$

where L1 and L2 are the self-inductance of the individual conductors and Mk is the mutual inductance between them. If the VCC and VSS are identical then LT is reduced to:

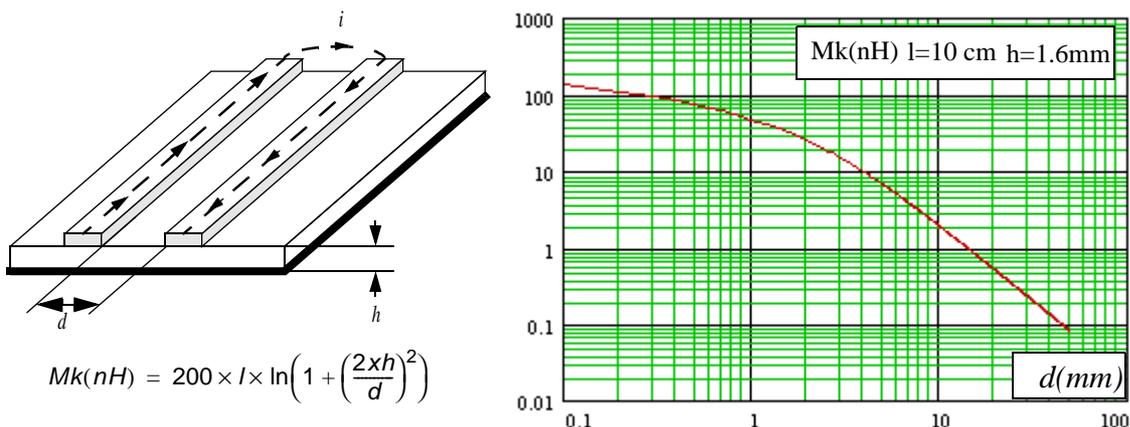
$$LT = 2 \times (L1 - Mk)$$

If the coefficient of magnetic coupling k between the two conductors is unity, the mutual inductance would be equal to the self-inductance of one conductor, since

$$Mk = L1$$

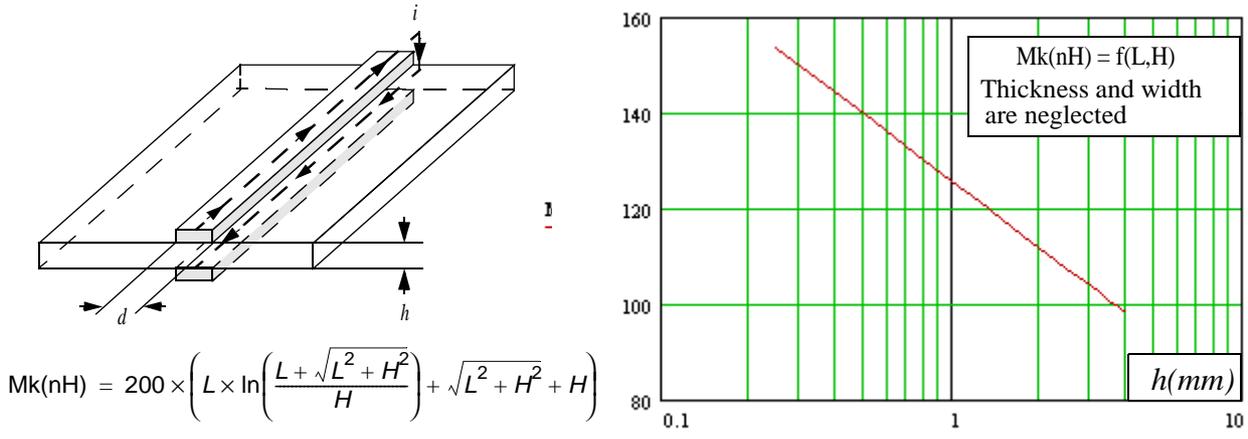
and the total inductance of the closed loop would be zero. So to minimize the total inductance of the complete current path, the mutual inductance between the conductors must be maximized. Therefore the two conductors should be placed as close as possible to minimize the area between them. Figure 6 and Figure 7 give the mutual inductance for different spacings.

Figure 6. Mutual Inductance for l = 10 cm and h = 1.6 mm



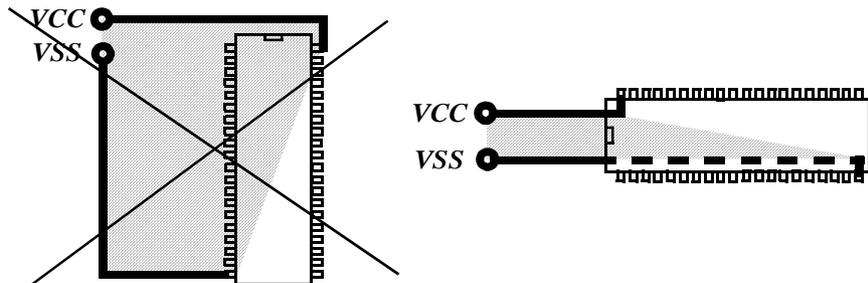
For this configuration the formula is applicable only if the direct and return currents are flowing through these two traces. Figure 7 plots different M_k values for some PCB trace dimensions.

Figure 7. Mutual Inductance Versus the Length and the Height of PCB Traces



If there is no dedicated plane for the power it is recommended to maintain as close as possible the tracks to reduce the surface of loop and the parasitic inductance as shown in Figure 8.

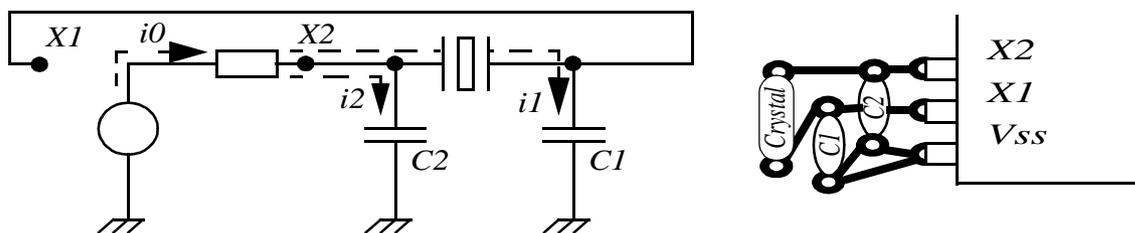
Figure 8. The Surface of the VCC and VSS Network has to be Reduced



Shorten the Loops around Oscillator and Crystal

Figure 9 shows the electrical model of a common oscillator implemented in a microcontroller. At the resonance the fundamental currents i_1 and i_2 have the same amplitude. In the closed loop mode the oscillator is stabilized in the saturation region of the amplifier that generates some harmonics in HF. So the output loop (X_2 , C_2 , and V_{SS}) has to be optimized first and then the input loop (X_1 , C_1 and V_{SS}). In both cases they have to be as small as possible.

Figure 9. Oscillator Lay-out

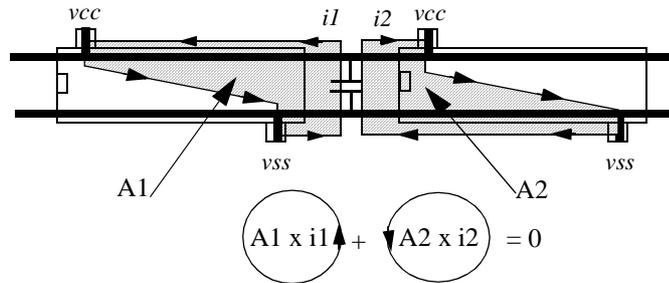


Cancel the H Field

Opposite Magnetic Loops

Identical circuits have to be implemented as in Figure 10. In this type of implementation the magnetic loop surface is the same and the H field are generated in opposite side which tends to cancel them. Other implementations can be used but this one needs only one decoupling capacitor for two chips.

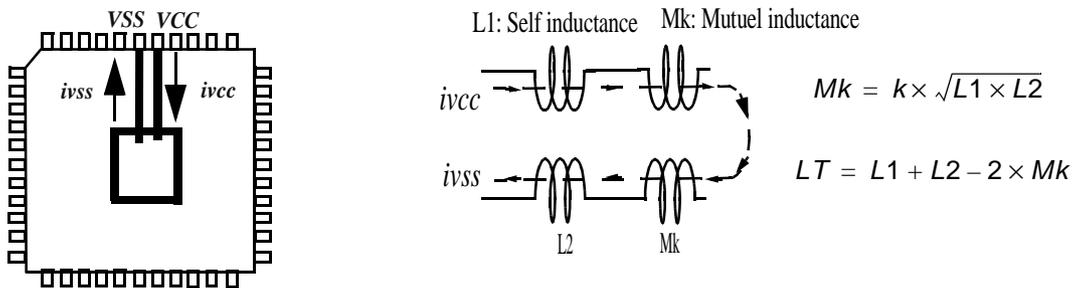
Figure 10. H Field Cancellation



Choose a Package with a VCC and VSS Close Together

When a VSS and VCC pins are close together the magnetic coupling can be close to 0.8 and the mutual inductance can reach the self inductance of one pin and cancel magnetic field of the total inductance of the VSS and VCC pins. This true when i_{vss} and i_{vcc} have the same magnitude and the same phase which is the case for the current flowing through a digital core of an I.C. but not completely true for an output buffer.

Figure 11. VSS and VCC Pins Close Together Can Cancel the Hfield



Choose a Package with Several VSS and VCC Pins Connected in Opposite Side

Double the number of VCC and VSS pins reduce by half the equivalent pin inductance and decrease down to 6dB the H field. If the second pin is mounted in the opposite side, the H field can be further reduced by 3 to 4 dB because a part of the H field is cancelled as shown in Figure 12 and reported in Figure 13.

Figure 12. Double and Opposite VSS Pins Reduce 3 to 4dB the H Field

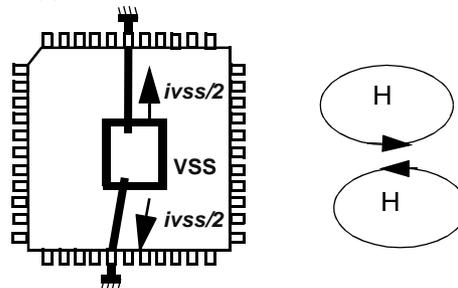
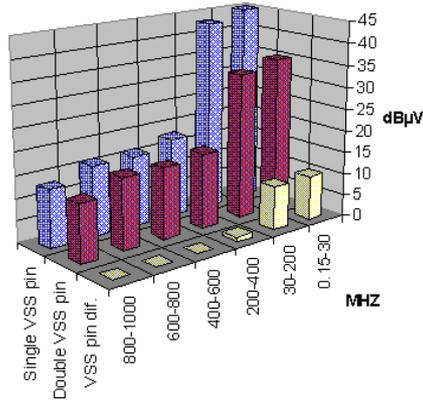


Figure 13. Double and Opposite VSS Pins Reduce the Radiated Emissions Down to 10dB



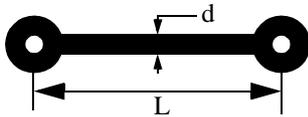
	0.15-30	30-200	200-400	400-600	600-800	800-1000
Single VSS pin	45	43	18	16	16	13
Double VSS pin	35	33	17	16	16	13
VSS pin dif.	10	10	1	0	0	0

Reduce the Inductance of all Devices (PCB traces, package, capacitors,...)

Increase the Width of the PCB Connections

Because the real world is not an ideal, a power-supply connection is not a pure short-circuit but a trace with parasitic elements such as resistors and inductors.

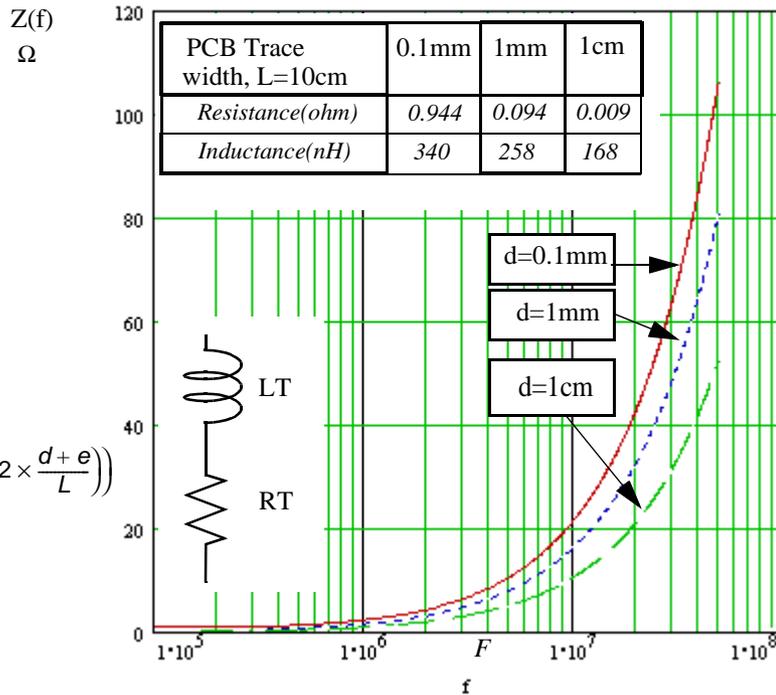
Figure 14. PCB Trace Modelization



e: PCB trace thickness in mm,
d: PCB trace width mm,
L: PCB length in m.
e=36µm for typical PCB

$$LT(\mu H) = 0,2 \times L \times \left(\ln\left(\frac{2 \times L}{d+e}\right) + 0,5 + 0,22 \times \frac{d+e}{L} \right)$$

$$RT(m\Omega) = 17 \times \frac{L}{d \times e}$$



This PCB trace is a complex impedance which varies with the frequency. Figure 14 plots the impedance versus the frequency for three different trace widths and for a length and a thickness trace assumed to be 10 cm and 36µm respectively. A PCB trace introduces voltage ripples and the width of PCB traces have to be large enough not to introduce a voltage drop which could be high. For example, when a 0.1A current at 30 MHz flows a PCB trace with 10 cm length and 0.1 mm width, this causes a 0.62V voltage drop. If the width is 100 times the previous one the voltage drop is reduced by a factor of two.

Used Power and Ground Planes

Microstrip Topology

The total inductance of a loop (LT) is drastically reduced when using a VSS plane because the equivalent inductance of the plane ($LPlane$) is much lower than the PCB trace ($LTrace$) as shown in Figure 15. This is mainly due to the contour taken by the H field which is much larger than the contour taken around the signal trace. These two inductances are rather independent and can be evaluated separately. The ground plane inductance is not affected by the PCB trace width and can be evaluated using the following expression:

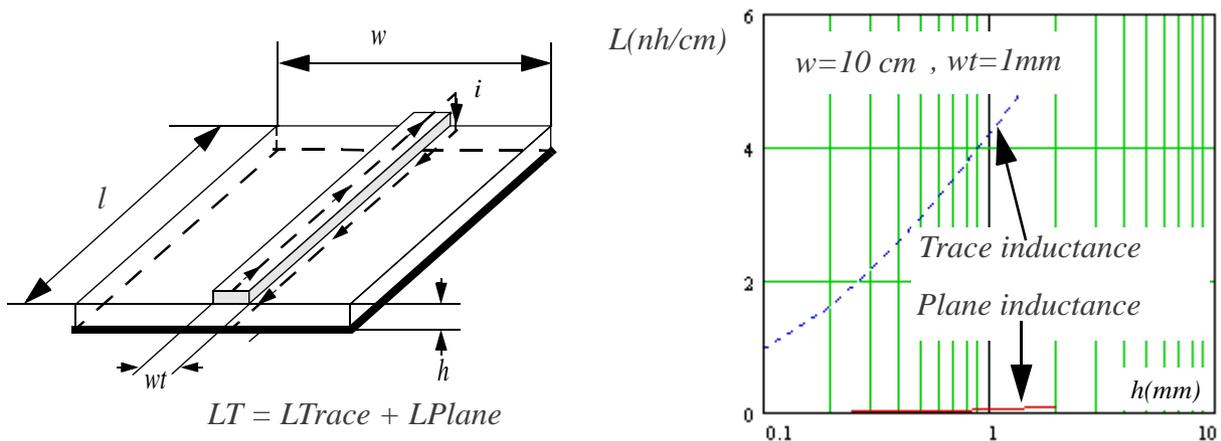
$$LPlane(nH/cm) = \frac{5 \times h}{w}$$

The PCB trace inductance can be evaluated using the following expression:

$$LTrace(nH/cm) = 10^{-9} \times \ln \left(1 + \frac{32 \times h^2}{wt^2} \times \left(1 + \sqrt{\pi \times \frac{wt}{8 \times h}} \right) \right)$$

This inductance is independent of the PCB ground width. For example a trace of 10 cm length and 1mm width and separated from the ground plane by 1.6mm presents an inductance of 51nH. A plane with the same dimensions and 10 cm width presents an inductance of 0.8nH. So the total inductance is the sum of the PCB trace and plane (51nH). The same trace without the ground plane has an inductance equal to 115nH. Thanks to the plane the trace inductance is reduced down to 2.5 factors.

Figure 15. A VSS Plane has a Lower Trace Inductance and Reduces the PCB Track Inductance

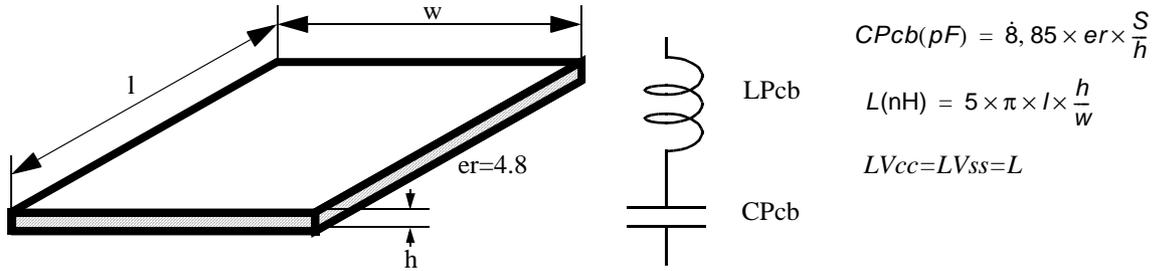


Power and Ground Planes

This is the best solution to reduce the parasitic elements because the parasitic inductance is very small due to a very large contour and a good magnetic coupling factor. It can be modeled by an LC circuit if the largest dimension between the source and the

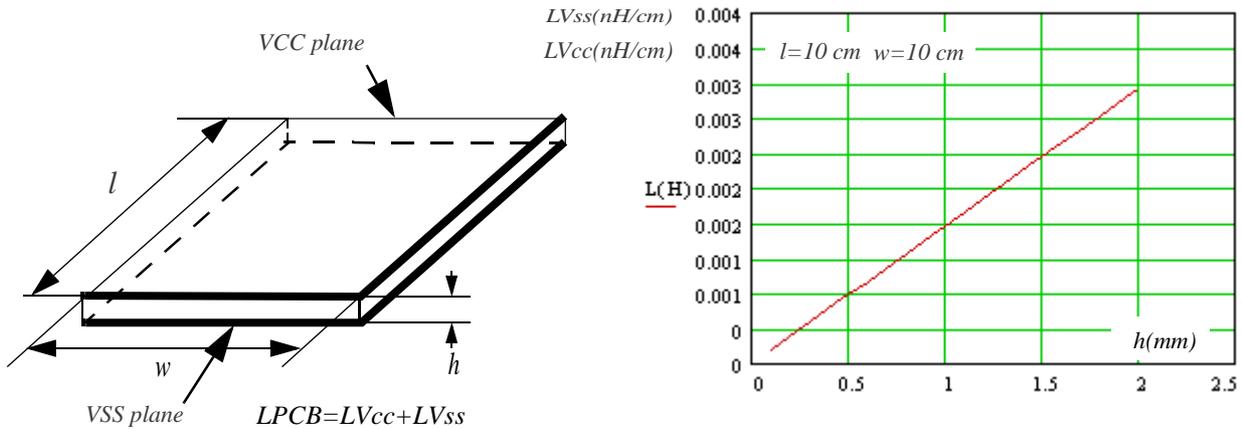
load is less than 1 tenth of the minimum wave length. Otherwise the PCB acts as a line or an antenna.

Figure 16. VCC and VSS Planes are Equivalent to an LC Model



The PCB capacitor consists in two copper planes with a dielectric inserted between the two planes. The equivalent capacitor (CP_{cb}) is evaluated using the formula in Figure 16. For example a 10 cm by 10 cm plane with 35 μ m thickness and separated by 1.6 mm has a total inductance of 0.05 nH and a capacitor equal to 271 pF. The frequency resonance of the plane is 1.4 GHz. So the power-plane technique is efficient for high frequencies if the distance between the source and the load is short. These plans are not so efficient in low frequency because the equivalent capacitor is not so high and the impedance across the circuit increases and the emission levels too. In low and medium frequency ranges additional decoupling capacitors help to maintain this impedance low.

Figure 17. Power-supply Planes Characteristics



The next table shows the value of the PCB inductance for the three configurations seen above. The Vcc and Vss Power plane configuration gives the best result and a large decoupling capacitor.

Table 1. Comparison of PCB inductance for w = 1mm, wt = 10cm, l = 10cm, h = 1.6mm

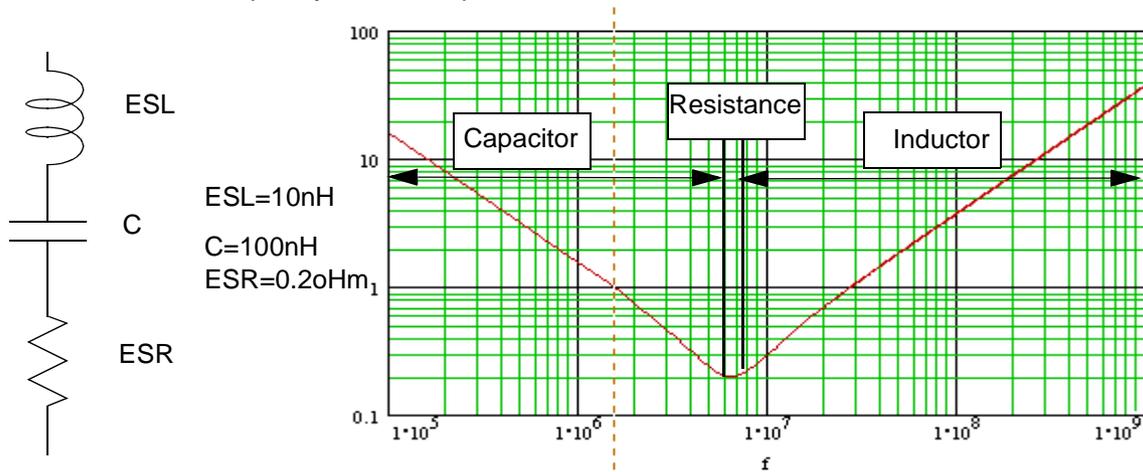
	Vcc PCB trace Vss PCB trace	Vcc PCB trace Vss plane	Vcc Plane Vss Plane
Inductance(nH)	115 + 115=230	51 + 0.8=51.8	0.025 + 0.025=0.05
Capacitance(pF)	5 pF	20 pF	271 pF

Adapt Decoupling Capacitors to the Working Frequency

A capacitor is not pure and can be modeled like an RLC circuit. The surface mount devices (SMD) have the smallest internal and external inductances and have to be selected to get the best results. Figure 18 shows the equivalent electrical model and plots the frequency response for a SMD 100 nF capacitor. The capacitor acts like a capacitor, a resistor or an inductor but depends on the frequency bands:

- *Medium frequency band:* 0 Hz to 6 MHz: the capacitor is a pure capacitor,
- *Resonance frequency:* 6-7 MHz: the capacitor is a pure resistance,
- *High frequency:* > 7 MHz: the capacitor acts as a pure inductance.

Figure 18. Self-Resonance Frequency of True Capacitor



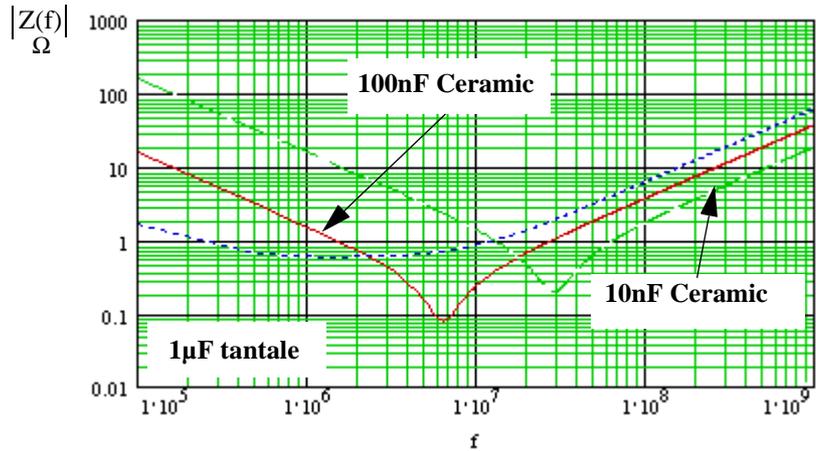
The frequency behavior depends on the type of capacitor. Table 2 gives the electrical characteristics for different capacitors.

Table 2. Capacitor Characteristics Comparison

	1 μ F Tantale	100 nF Ceramic	10 nF Ceramic
R	0.8	0.08	0.2
L(nH)	6	3	3
Fr(MHz)	2	7.1	29

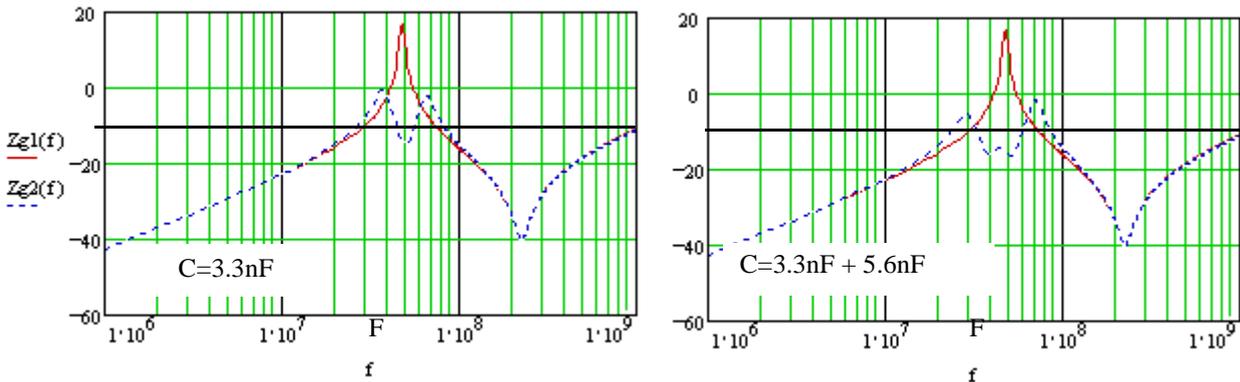
Figure 19 plots the frequency response for different types of capacitors.

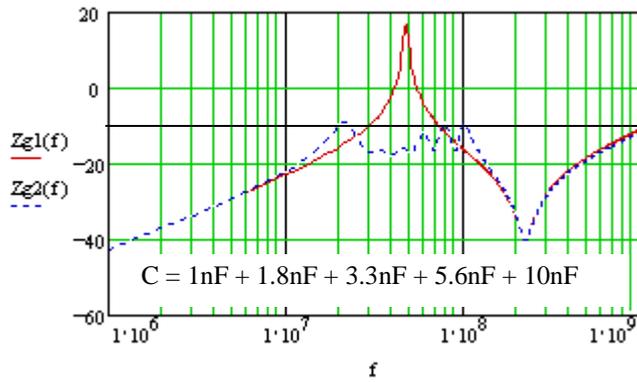
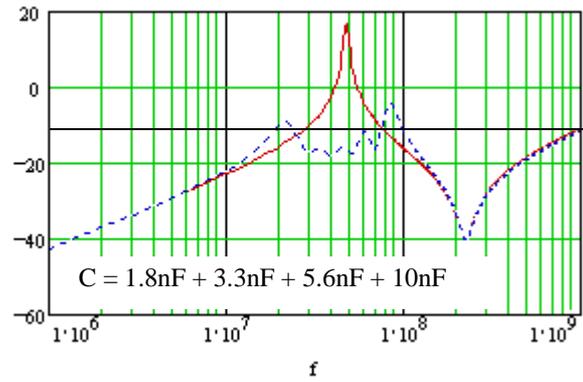
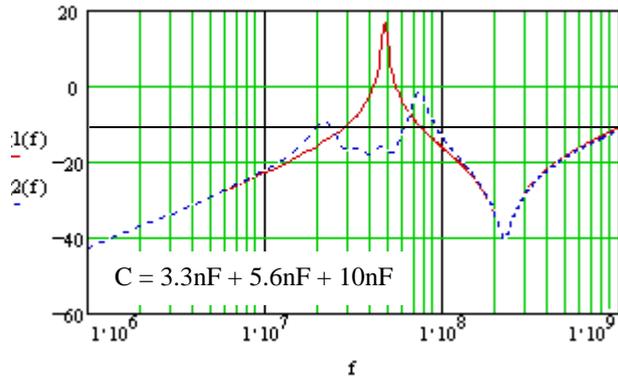
Figure 19. Plots Versus Frequency of Several Types of Capacitors



Assuming the frequency band of the noise is in the range 10MHz to 100MHz and to be compliant the network impedance has to be less than -10dBohms. Figure 20 plots the power network impedance versus the frequency and the impact of the decoupling capacitors on the impedance of the network. Five decoupling capacitors have to be added to be in the -10dBohms specification. Each capacitors is calculated to damp the pic of each frequency resonances.

Figure 20. Decoupling Effects on the Network





Shorten the Capacitor Connection Length

When the capacitor value is assumed to be constant, the resonance frequency depends on the inductance. The total inductance of the circuit consists of the intrinsic capacitor inductance and the inductance of the connections. The higher the inductance, the lower the resonance frequency. It is recommended to maintain as short as possible the length of the connections.

Figure 21. Connection Increase the Impedance in H.F

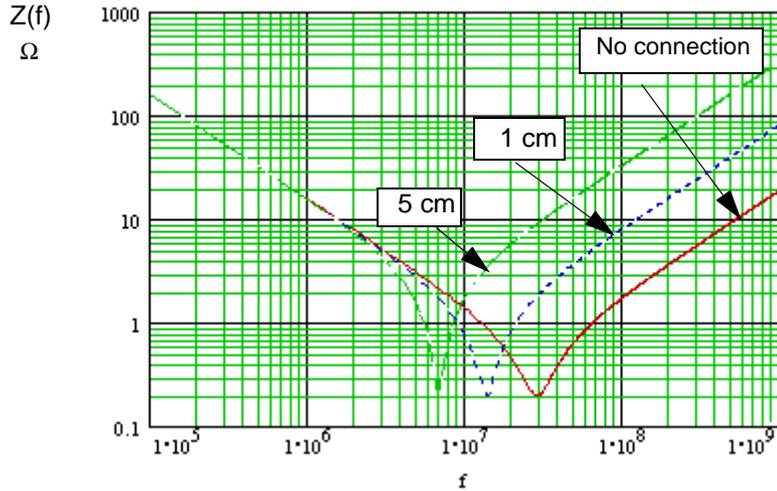


Figure 21 plots the capacitor impedance versus three different connection lengths. The resonance varies from 7 MHz to 30 MHz when the connection length varies from 0 to 5 cm.

Select the Smallest Package

The package is used to connect the die to the pins but this connection consists of an inductance and a resistance. The die has an internal capacitance and the package in series with the die can be modeled like an RLC circuit which has a resonance frequency. It is recommended to use the smallest package in order to reduce the Q factor. Figure 22 shows the effect on the Q factor for a DIL and PLCC package and the die without the package (COB).

Figure 22. Impedance for a DIL, PLCC and a COB

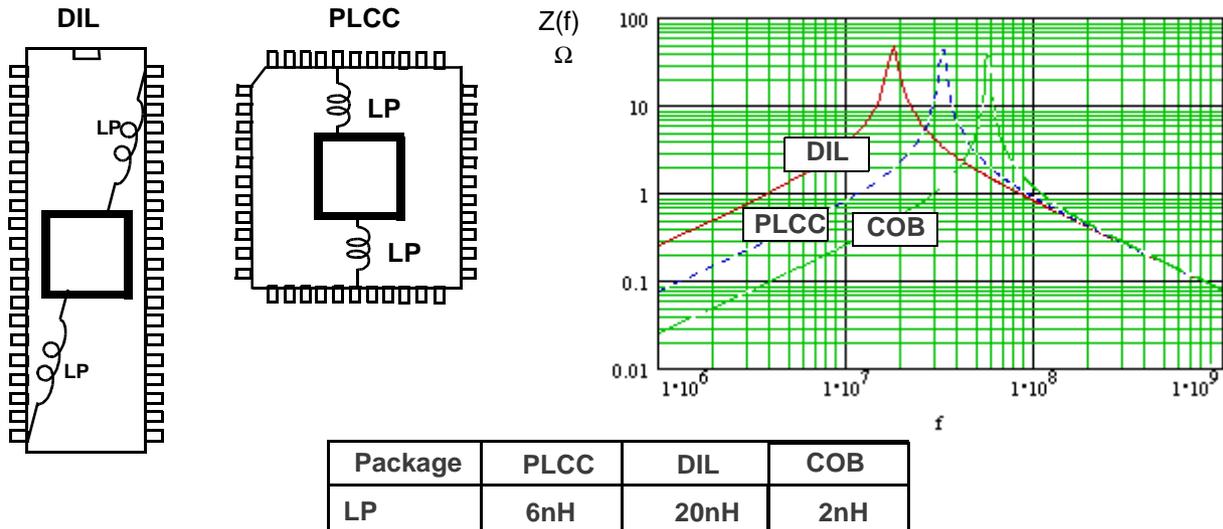
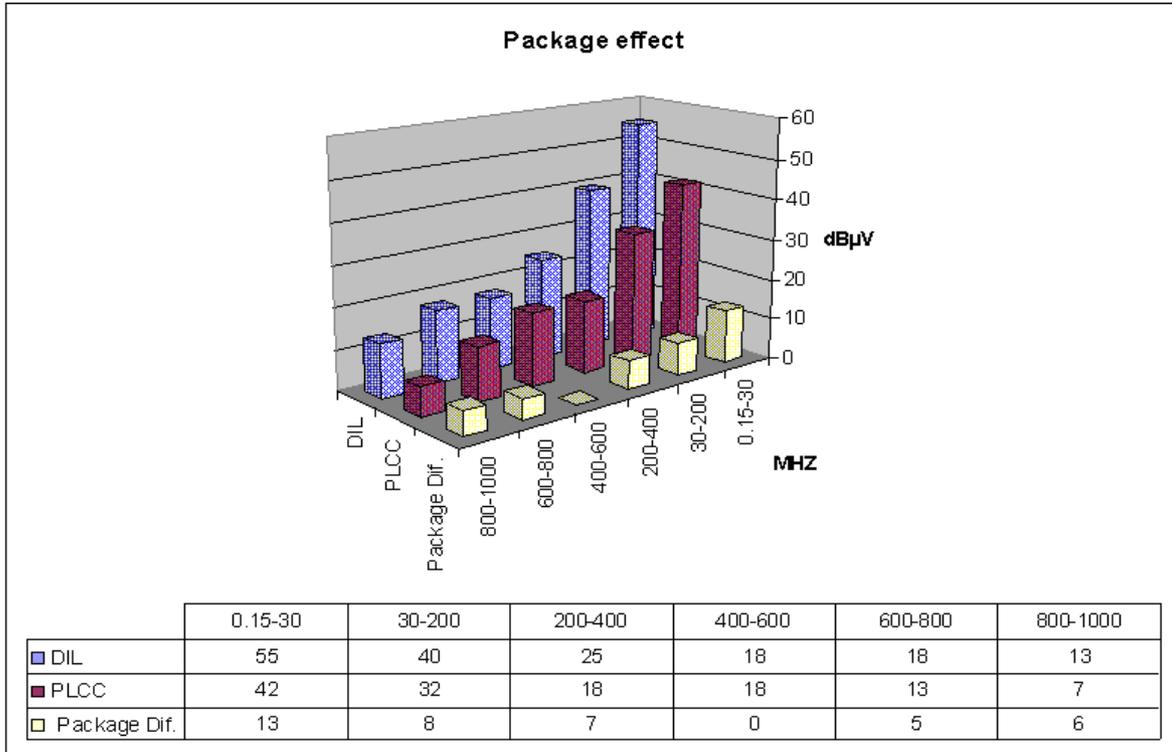


Figure 23 compares the radiated emissions between a DIL and PLCC package. Emissions can be reduced down to 7dB in the range 0.15 MHz to 400 MHz using a PLCC package instead of a DIL package.

Figure 23. Package Effect on Radiated Emissions

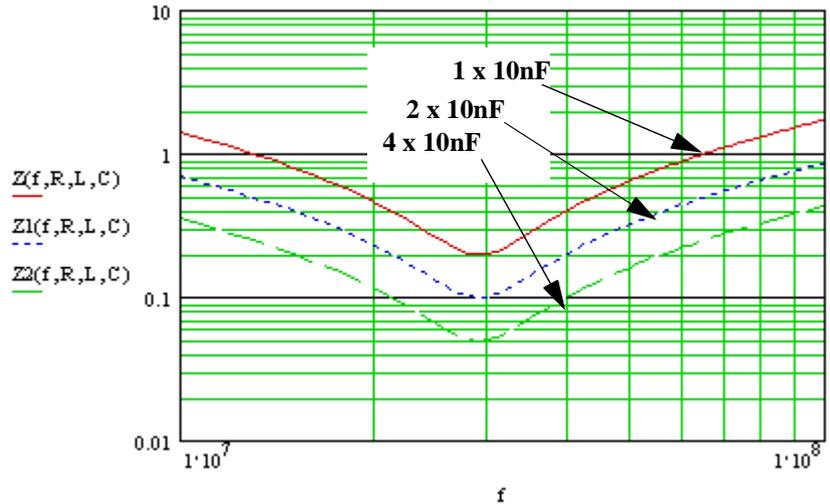


Reduce the Equivalent Series Resistance

Identical Capacitors in Parallel to Reduce the ESR

If the impedance of the power network is out of specification in some frequency bands, several identical capacitors can be connected in parallel to reduce the equivalent ESR. This impedance is reduced by a factor of two each time the number of capacitors is doubled (see Figure 24).

Figure 24. ESR is Reduced by Connected Several Identical Capacitors in Parallel



Choose COG, NPO and X7R dielectric types

Capacitors that have these dielectrics have the lowest ESR and a good stability in temperature and the value can cover from few pF to several tens of nF.

Conclusion

Most of the EMC improvements detailed in this application note are already known but they are not always applied. There is not a unique solution to improve the EMC of a system but most yield to a cumulative improvement. Designers must keep in mind these mechanisms and apply them early in the conception phase of a system to ensure EMC compliance.

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