APPLICATION NOTE

A NEW APPROACH TO PARAMETER EXTRACTION FOR THE SPICE POWER MOSFET MODEL

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ABSTRACT

The increasing complexity of Power MOSFET technology and the inclusion, on the same chip, of more and more intelligence together with the power switch, requires an accurate simulation of DC and AC characteristics of the power device to obtain a good correlation between simulation results and experimental data.

A robust design has to take the worst cases into consideration as well as the typical conditions. Also the simulation has to make provision for the spread of device characteristics due to manufacturing tolerances.

This paper describes a new approach to parameter extraction for a sub-circuit model of Power MOSFETs to be used in the SPICE circuit simulator which uses a powerful analytical simulator developed by SGS-THOMSON Microelectronics.

This simulator, whose models have been built considering physical structure and layout parameters, allows the optimisation of the most important device characteristics and also takes into account the possible parameter spread due to the process. For this reason the program output can give not only the average values of required parameters but also their statistical distribution.

1. INTRODUCTION

The modelling of power MOSFETs, in spite of the contributions from numerous authors, still exhibits some points to be improved. From the user point of view the choice of the model topology is determined by the degree of accuracy the results require, the computation time, convergence problems and the robustness and simplicity of the parameter extraction method.

One of the weak points of the actual models is due to drain-gate capacitance modelling which complicates the switching behaviour because of its high degree of non-linearity. But leaving apart this drawback which can be mitigated at the cost of time), the usefulness of model accuracy has often increasing model complexity, (and thus computation been limited by the lack of robustness of the parameter extraction method employed. The aim of this paper is to give a contribution to solving this weak point.

The parameter extraction is usually performed by elaboration of experimental measurements, but some parameters are not directly measurable and others are not related to the physics of the device but are simply fit parameters to model the device as close as possible to reality. This paper shows a different way to tackle the problem which employs a new powerful package, COSMOS, entirely developed in-house by SGS-THOMSON Microelectronics. A number of analytical models have been developed to allow the extraction of parameters tied to the elements of the sub-circuit to be very fast and rugged. In the same way this package allows extraction of the worst case parameters because it also takes into account manufacturing tolerances.

2. SGS-THOMSON SPICE MODEL OF POWER MOSFET

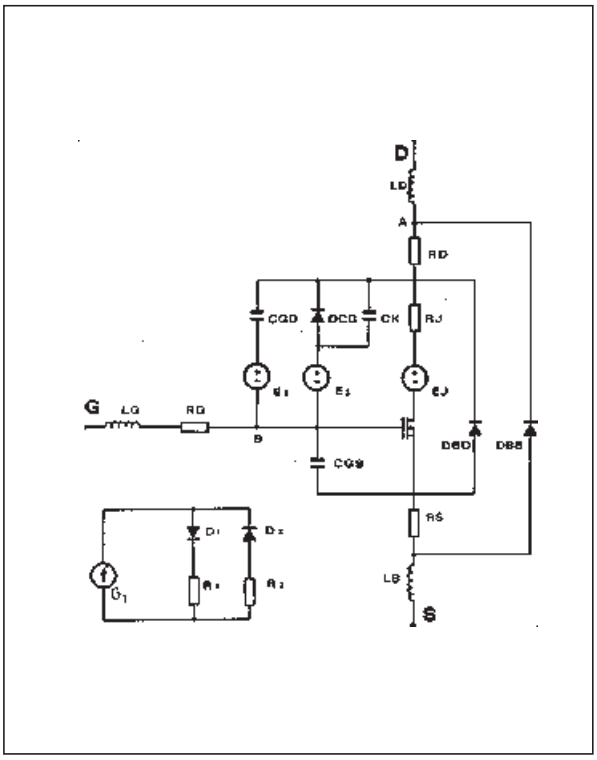
Figure 1 illustrates the components of the sub- circuit model. A Spice MOSFET model is the main switching element in the circuit. The other elements take into account the stray inductances due to the wires (L_s, L_d, L_g), the poly-silicon gate resistance (R_g), the resistance due both to silicon and to bonding (R_s, R_d), the body-drain capacitance modulation (DBD) and the leakage current when the device is in breakdown.

Two points need a more detailed explanation:

a) the additional voltage dependent series drain resistance (R_j, E_j) is used in order to model the extra resistance of the epitaxial layer and substrate due to the depletion modulation of body-drain junction by the drain-source voltage and not accounted for in the ideal MOSFET model;

b) the high non-linearity of the gate-drain capacitance is typical of a MOS structure switching from being strongly inverted to the accumulation state. The only difference is due

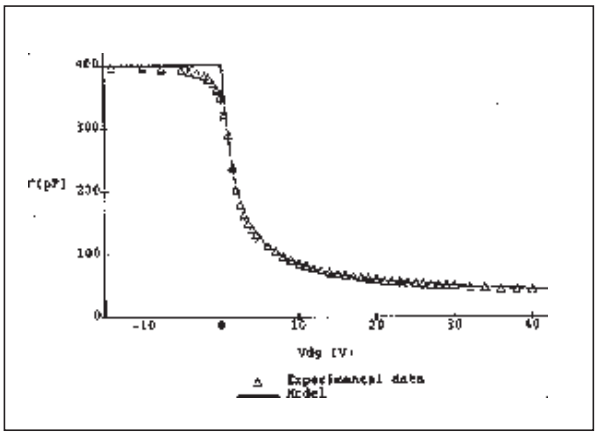
Figure 1. Sub-circuit SPICE model for Power MOSFET



to the fact that modulation of the depletion zone is caused not only by the voltage but also by lateral injection of the charge coming from the channel. This behaviour has been modelled by making the drain-gate and gate-source capacitances of the ideal MOSFET negligible by setting to zero the length of the overlapping regions between the gate and the other two elements.

These capacitances have been replaced by a constant gate-source capacitance, C_{GS}, and a two-element gate-drain capacitance, C_{GD}. Figure 2 shows an experimental CV diagram and its simulation obtained by the model described above. When the drain-gate voltage is positive, i.e. V(a) - V(b) > 0, then the leg containing the diode DD is activated and C_{GD} is modelled by the diode depletion capacitance. The insertion of a capacitance, C_k, in parallel with this diode gives not only a better fitting of C_{GD} for high values of drain- source voltages but also improves the simulation for low values of V_{DS}. When the drain-gate voltage is negative the C_{GD} capacitance is modelled disabling this leg and activating the other one.

Figure 2. C_{rss} modelling



3. COSMOS: AN ANALYTICAL SIMULATOR FOR POWER MOSFET

COSMOS was born as a tool to optimise the Power MOSFET design. It is becoming more and more difficult to do this because of increasing demands of users to improve performance and of the large number of variables involved which interact with each other.

This software package provides some tools to match the most important device characteristics (R_{on}, BV_{DSS}, Capacitances, V_{th}, Gate-charge etc.) with the demands made and the netlist and the model parameters (average value and worst case) for the SPICE sub-circuit.

3.1 Program structure

The schematic is shown in figure 3. The statistical data for manufacturing processes and device design (figure 4) collected in a data base are processed by the analytical models of COSMOS which performs various analyses.

3.1.1 Sensitivity Analysis

This option allows the evaluation of the influence of a single layout or process parameter on the desired characteristic of the device (e.g. R_{on}, BV_{DSS}, C_{iss}. C_{oss}, C_{rss}, gate-charge, etc.).

3.1.2 Statistical Analysis

The statistical input data allows COSMOS to output not only the average value of the required response but also its statistical distribution. The average value is also given divided into its various components to make optimisation of the device easier. Figure 5 shows an example referred to R_{on} and figure 6 to intrinsic capacitances.

Figure 3. COSMOS structure

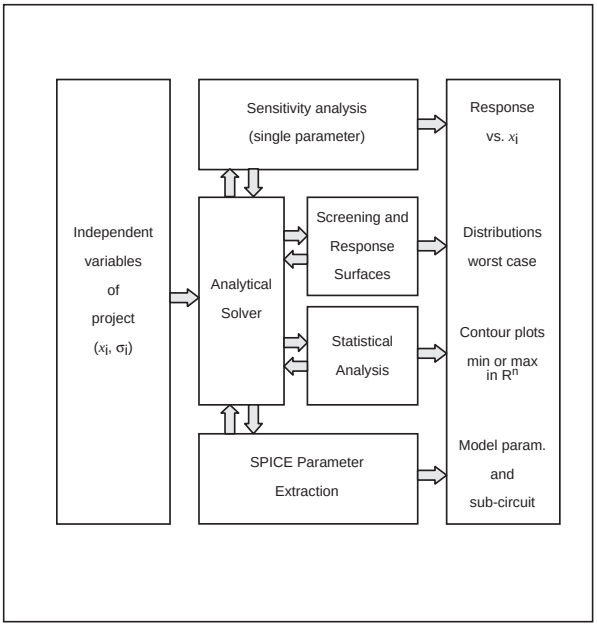


Figure 4. Layout and process parameters

Parameter	
1	Cell dimension
2	Cell spacing
3	Gate-drain area related to gate oxide
4	Gate-drain area related to field oxide
5	Gate-p^+ area related to gate oxide
6	Gate-p+ area related to field oxide
7	Gate-Source metal area
8	Deep Body area
9	Channel width measured on poly mask

Parameter	
1	Gate oxide thickness
2	Field oxide thickness
3	P-Vapox Thickness
4	Oxide charge (Qo + Qss)
5	Channel length
6	Channel doping (peak)
7	Epy layer doping
8	Epy layer width
9	Cs deep body
10	Xj deep body

Figure 5. COSMOS outputs, R_{on} example:
a) Average values
b) Descriptive statistics

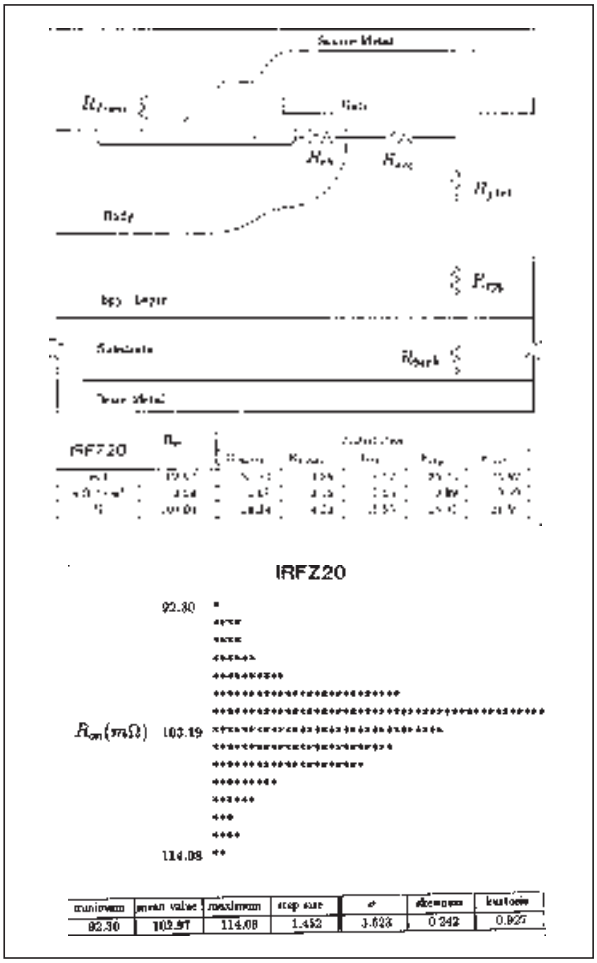
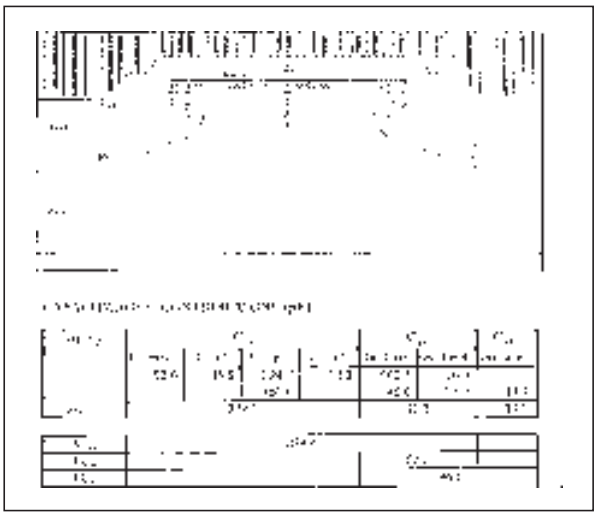


Figure 6. COSMOS output - capacitances



3.1.3 Screening and Response Surfaces.

It is possible to screen between the most important variables influencing the requested response (figure 7) and to obtain the response surfaces related to the simultaneous variation of two or more input factors (figure 8).

3.1.4 Spice Parameters Extraction

This option, which is discussed in more detail later, allows the extraction of the values of the elements of the SPICE sub-circuit model.

3.2 Models

The COSMOS models are derived from the classical ones [1][2][3], but they have been improved taking into account some effects that can not be disregarded due to the most recent technology.

3.2.1 R_{on}

The lateral depletion of the body, due to the built-in voltage and to V_{DS}, which leads to a reduction of the region available for the current flow, now must be considered not only for high voltage devices but also for the low voltage ones. The increased packing density makes this depletion significant with respect to the dimensions of the bodies thus resulting in a magnification of the JFET effect. Moreover, the extremely low values of R_{on} x Area in new High Density devices requires that the model considers not only the silicon contribution but also those due to metallization.

Other effects such as the mobility variation caused by surface scattering and electric fields [4][5] and the influence of doping non-uniformity in the channel [2] are also considered.

3.2.2 BV_{DSS}

In a power MOSFET both breakdown voltage and R_{on} optimisation are directly related. They depend on doping (N_d) and epitaxial layer thickness (W_d) which act on BV and R_{on} optimisation in opposite ways. The problem is finding the pair, N_d, W_d, that minimise R_{on} at a fixed BV_{DSS}. The latter is computed taking into account the body doping profile, the eventual reach-through condition and the efficiency of the edge termination employed. The graphics tools of the program make this search for optimum conditions easier: in fact we can obtain BV and R_{on} maps (vs. N_d, W_d) and the N_d and W_d level lines in a BV-R_{on} coordinate system.

3.2.3 Capacitance

The models of the intrinsic capacitances of a Power MOSFET have been developed taking into account not only the doping non-uniformity but also the influence of the charge associated with the body lateral depletion.

4. COSMOS AS SPICE PREPROCESSOR

The modern design of electronic devices means that the mark must be hit with the first shot to minimise costs in terms of time and money. This can be achieved only by having a set of powerful simulators that make sure that the manufacturing of the first device is very close to the target. COSMOS, figure

Figure 7. COSMOS output - screening example

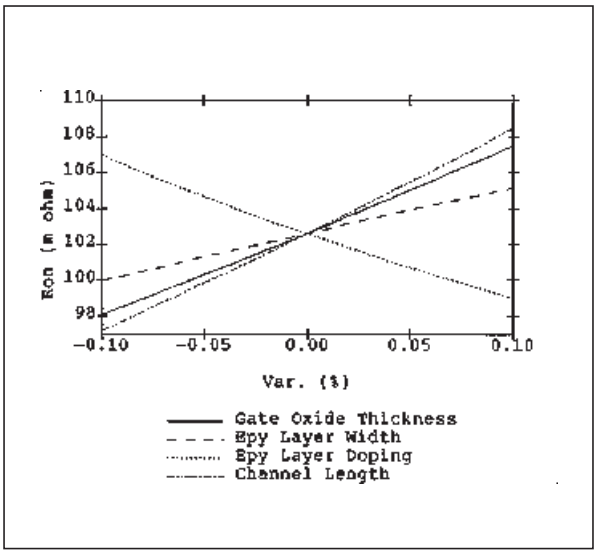
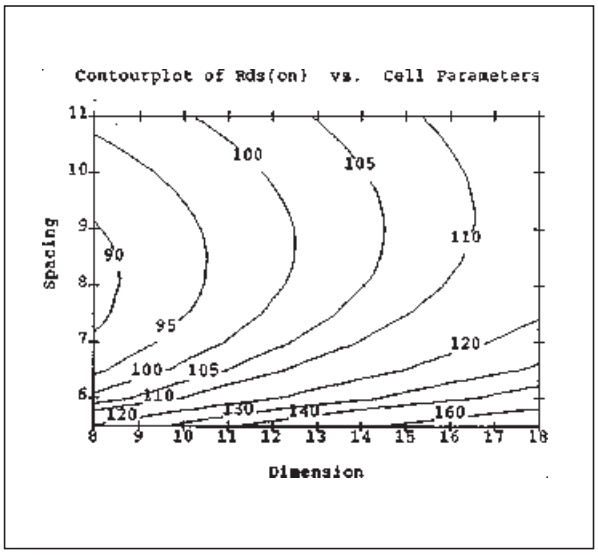


Figure 8. COSMOS output - response surface example



9, is placed between the process simulator (e.g. SUPREM, SUPRA) and the circuit simulator (e.g. SPICE) allowing the device optimisation to match the characteristics requested in the specific application.

4.1 Generation of statistical distribution of parameters and worst case extraction.

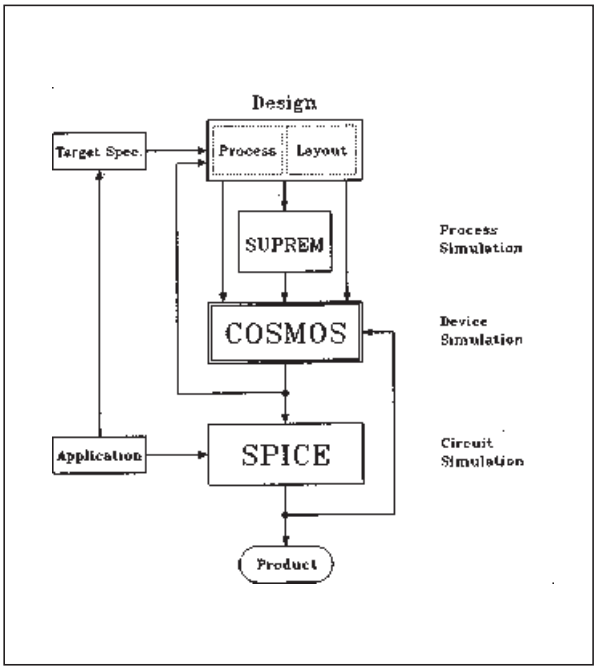
Starting from the distribution of the experimental data of process variables and from the design tolerances, the inherent speed of the analytical method allows the production of a random and statistically relevant set of input variables, using a Box-Muller transformation [6].

This set in turn, is used to generate the distribution of the desired output responses. This is possible also for the parameters of the sub-circuit model for SPICE. The MODEL cards related to typical values and to worst cases are generated taking into account the mean and the boundary values of the distributions above discussed. A typical output file is shown in appendix A.

CONCLUSION

The implementation of analytical models validated by a 2-D numerical simulator [5] is a powerful tool for studying device performance and optimisation. COSMOS allows a very fast computation of the influence of one or more parameters of the final characteristics of the device. Moreover it gives the average and worst case models for SPICE allowing the device designer to have fast feedback thus reducing the time needed for designing.

Figure 9. Total CAD approach to Power MOSFET design



REFERENCES

[1] Modelling of the On-Resistance of LDMOS, VDMOS, and VMOS Power Transistors, S.C. Sun and J.D. Plummer, IEEE Transactions on Electronic Devices, Vol. 27, No. 2, February 1980.

[2] Threshold and Punch-through Behaviour of Laterally Non-uniformally Doped Short-Channel MOSFETs, C.T. Wang and D.H. Navon, IEEE Transactions on Electronic Devices, Vol. 30, No. 7, July 1983.

[3] A Simple Theory to Predict the Threshold Voltage of Short-Channel lGFET's, L.D. Yau, IEEE Transactions on Electronic Devices, Solid State Electronics, 17,1974.

[4] A Physically Based Mobility Model for Numerical Simulation of Non-Planar Devices, C. Lombardi, S. Manzini, A. Saporito, M. Vanzi, IEEE Transactions on Computer-Aided Design, Vol. 7, No. 11, November 1988.

[5] HFlELDS: A Highly Flexible 2-D Semiconductor Device Analysis Program, G. Baccarani et al., Nasecode IV, June 1985.

[6] Numerical Recipes, W.K. Press, B.P. Flannery, S.A. Tenkolsky, W.T. Vetterling, Cambridge University Press, 4

APPENDIX A. TYPICAL SPICE OUTPUT FILE

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*       Sub-circuit for IRFZ20
*
.SUBCKT PWRMOS 1 2 3
*
LG 2 4 0.7500E-08
LS 12 3 0.7500E-08
LD 6 1 0.4500E-08
*
RG 4 5 0.1000E+02
RS 9 12 0.4000E-02
RD 7 6 0.5017E-01
RJ 8 7 0.2071E-01
*
CGS 5 9 0.1430E-09
CGD 7 10 0.5023E-09
*
CK 11 7 0.0000E+00
DGD 11 7 DGD
*
DBS 12 6 DBS
DBD 9 7 DBD
*
MOS 13 5 9 9 MOS L= 0.1800E-05 W=0.4593
*
E1 10 5 101 0 1
E2 11 5 102 0 1
*
EJ 8 13 POLY(2) 6 8 6 12 0 0 0 0 0.03
*
G1 0 100 7 5 1.0E-06
D1100 101 DID
D2 102 100 DID
Rl 101 0 1.0E+06
R2 102 0 1.0E+06
*
.ENDS PWRMOS
*
*
*       Models for IRFZ20
*
*
MODEL MOS NMOS
*
+       LEVEL = 3
+       TOX = 0.8500E-07
+       VTO = 3.134
+       PHI = 0.821
+       NSUB = 0.1150E+18
+       IS = 0.0000E+00
+       JS = 0.0000E+00
+       KAPPA = 0.180
+       UO = 491.335
+       THETA = 0.020
*
*
.MODEL DGD D
*
+       IS = 0.0000E+00
+       CJO = 0.3980E-09
+       VJ = 1.060
+       M = 0.630
*
.MODEL DBD D
*
+       IS = 0.0000E+00
+       CJO = 0.5l00E-09
+       VJ = 0.670
+       M = 0.380
*
.MODEL DBS D
*
+       IS = 0.1950E-ll
+       BV = 72.10
+       N = 1.10
+       TT = 0.1250E-07
+       RS = 0.2275E-01
*
*
.MODEL DID D
*
+       IS = 0.2000E-11
+       RS = 0.0000E+00
*
*       - End Models -
```