1 PRODUCT OVERVIEW

SAM87RI PRODUCT FAMILY

Samsung's SAM87RI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM87RI microcontrollers have an external interface that provides access to external memory and other peripheral devices.

S3C9644/C9648/P9648 Microcontroller

The S3C9644/C9648/P9648 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87RI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The S3C9644 has 4K-bytes of program memory on-chip and S3C9648 has 8K-bytes.

Using the SAM87RI design approach, the following peripherals were integrated with the SAM87RI core:

— Five configurable I/O ports (32 pins)

— 20 bit-programmable pins for external interrupts

— 8-bit timer/counter with three operating modes

— Low speed USB function

The S3C9644/C9648/P9648 is a versatile microcontroller that can be used in a wide range of low speed USB support general purpose applications. It is especially suitable for use as a keyboard controller and is available in a 42-pin SDIP and a 44-pin QFP package.

OTP

The S3C9644/C9648 microcontroller is also available in OTP (One Time Programmable) version, S3P9648. S3P9648 microcontroller has an on-chip 8K-byte one-time-programmable EPROM instead of masked ROM. The S3P9648 is comparable to S3C9644/C9648, both in function and in pin configuration.

FEATURES

CPU

- SAM87RI CPU core

Memory

- 4/8K-byte internal program memory (ROM)
- 208-byte RAM

Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.0 µs at 6 MHz f_{OSC}

Interrupts

- 25 interrupt sources with one vector, each source has its pending bit
- One level, one vector interrupt structure

Oscillation Circuit

- 6 MHz crystal/ceramic oscillator
- External clock source (6 MHz)

General I/O

- Bit programmable five I/O ports (34 pins total)
  — (D+/PS2, D-/PS2 Included)

Timer/Counter

- One 8-bit basic timer for watchdog function and programmable oscillation stabilization interval generation function
- One 8-bit timer/counter with Compare/Overflow

USB Serial Bus

- Compatible to USB low speed (1.5 Mbps) device 1.0 specification.
- 1 Control endpoint and 2 Data endpoint
- Serial bus interface engine (SIE)
  — Packet decoding/generation
  — CRC generation and checking
  — NRZI encoding/decoding and bit-stuffing
- 8 bytes each receive/transmit USB buffer

Operating Temperature Range

- – 40 _C to + 85 _C

Operating Voltage Range

- 4.0 V to 5.25 V

Package Types

- 42-pin SDIP
- 44-pin QFP

BLOCK DIAGRAM

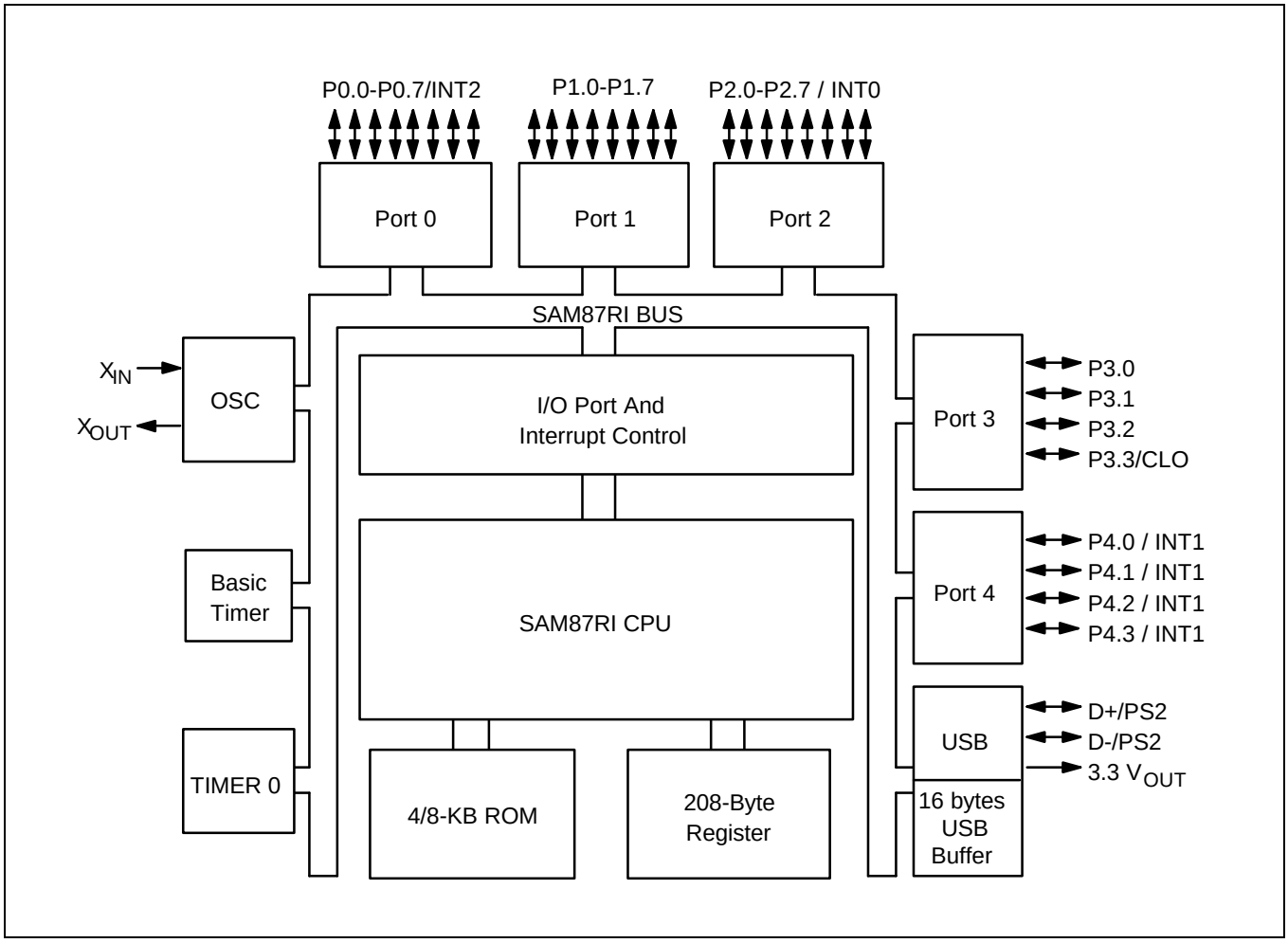


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

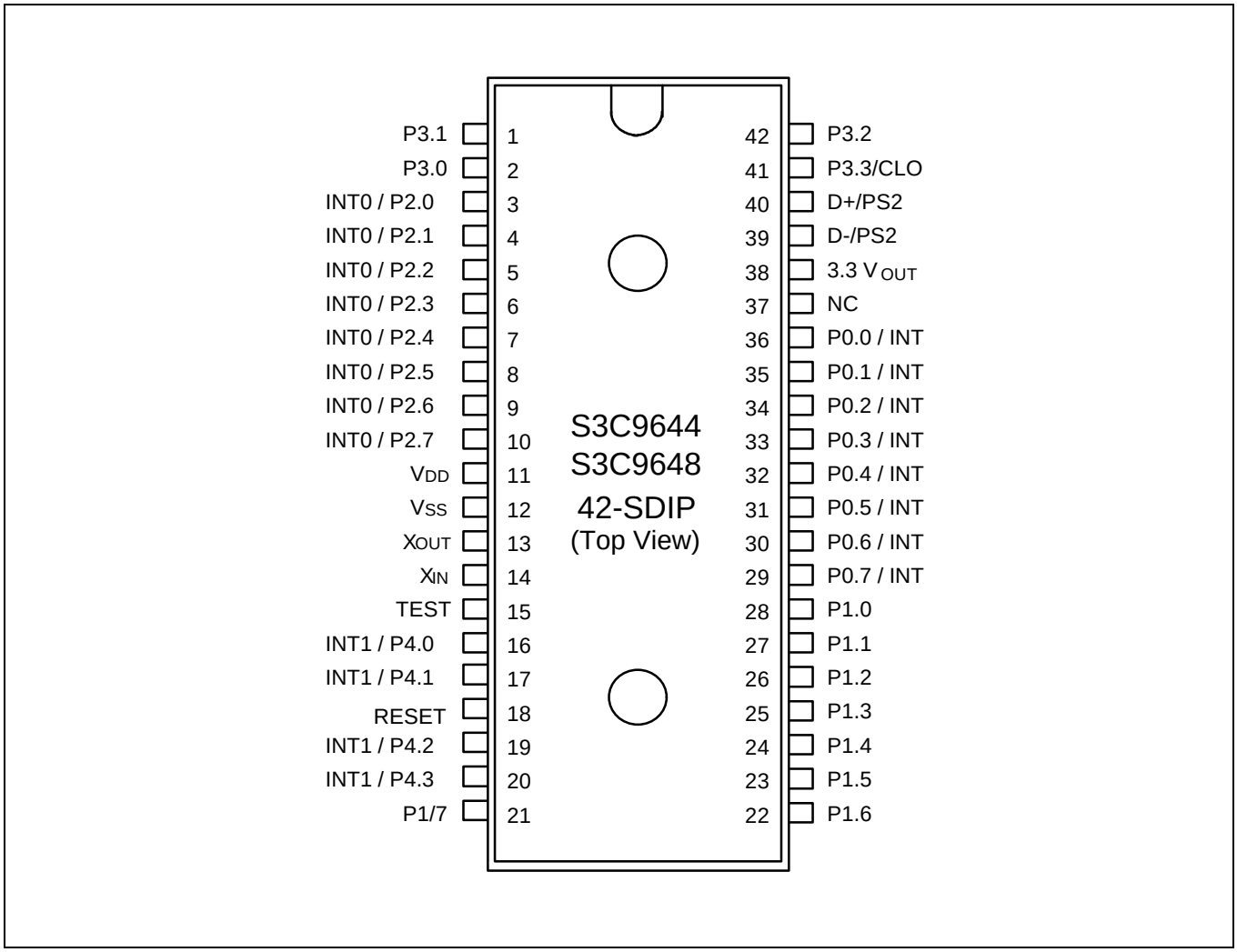


Figure 1-2. Pin Assignment Diagram (42-Pin SDIP Package)

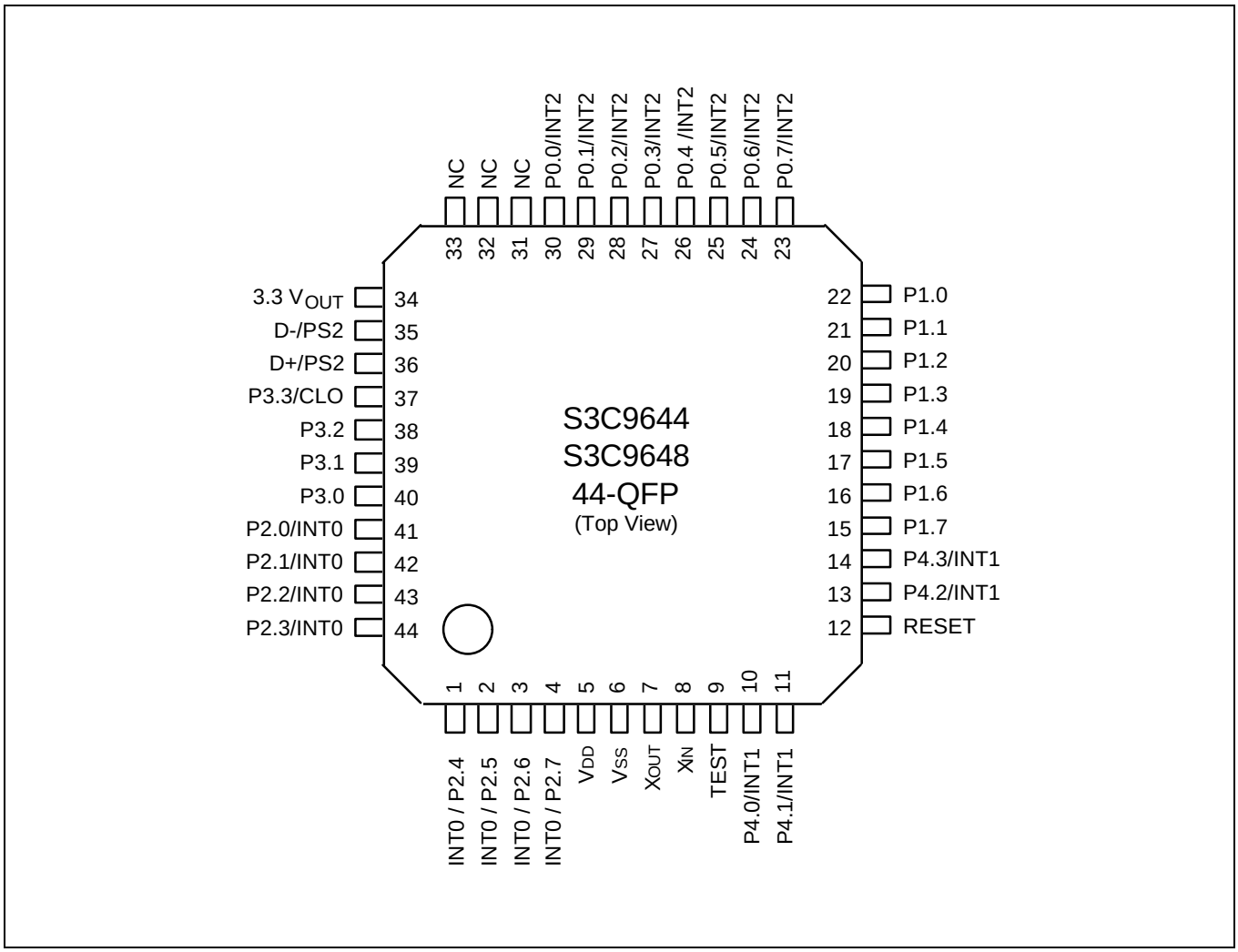


Figure 1-3. Pin Assignment Diagram (44-Pin QFP Package)

PIN DESCRIPTIONS

Table 1-1. S3C9644/C9648/P6408 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
P0.0-P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port0 can be individually configured as external interrupt inputs. Pull-up resistors are assignable by software.	B	36-29 (30-23)	INT2
P1.0-P1.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Pull-up resistors are assignable by software.	B	28-21 (22-15)	–
P2.0-P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port2 can be individually configured as external interrupt inputs. Pull-up resistors are assignable by software.	B	3-10 (41-44, 1-4)	INT0
P3.0-P3.3	I/O	Bit-programmable I/O port for Schmitt trigger input, open-drain or push-pull output. P3.3 can be used to system clock output(CLO) pin.	C	2, 1, 42, 41 (40-37)	P3.3/CLO
P4.0-P4.3	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output or push-pull output. Port4 can be individually configured as external interrupt inputs. In output mode, pull-up resistors are assignable by software. But in input mode, pull-up resistors are fixed.	D	16, 17, 19, 20 (10, 11, 13, 14)	INT1
D+/PS2 D-/PS2	I/O	Programmable port for USB interface or PS2 interface.	–	40-39 (36-35)	–
3.3 V_{OUT}	–	3.3 V output from internal voltage regulator	–	38 (34)	–
X_{IN}, X_{OUT}	–	System clock input and output pin (crystal/ceramic oscillator, or external clock source)	–	14, 13 (8, 7)	–
INT0 INT1 INT2	I	External interrupt for bit-programmable port0, port2 and port4 pins when set to input mode.	–	3-10, 16,17, 19, 20, 29-36 (30-23, 41-44, 1-4, 10, 11, 13, 14)	PORT2/ PORT4/ PORT0
RESET	I	RESET signal input pin. Input with internal pull-up resistor.	A	18 (12)	–
TEST	I	Test signal input pin (for factory use only; connected to V_{SS})	–	15 (9)	–
V_{DD}	–	Power input pin	–	11 (5)	–
V_{SS}	–	Ground input pin	–	12, (6)	–
NC	–	No connection	–	37 (31,32, 33)	–

NOTE: Pin numbers shown in parenthesis '( )' are for the 44-QFP package; others are for the 42-SDIP package.

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the S3C9644/C9648/P6408

Circuit Number	Circuit Type	S3C9644/C9648/P6408 Assignments
A	I	RESET signal input
B	I/O	Ports 0, 1, and 2
C	I/O	Port 3
D	I/O	Port 4

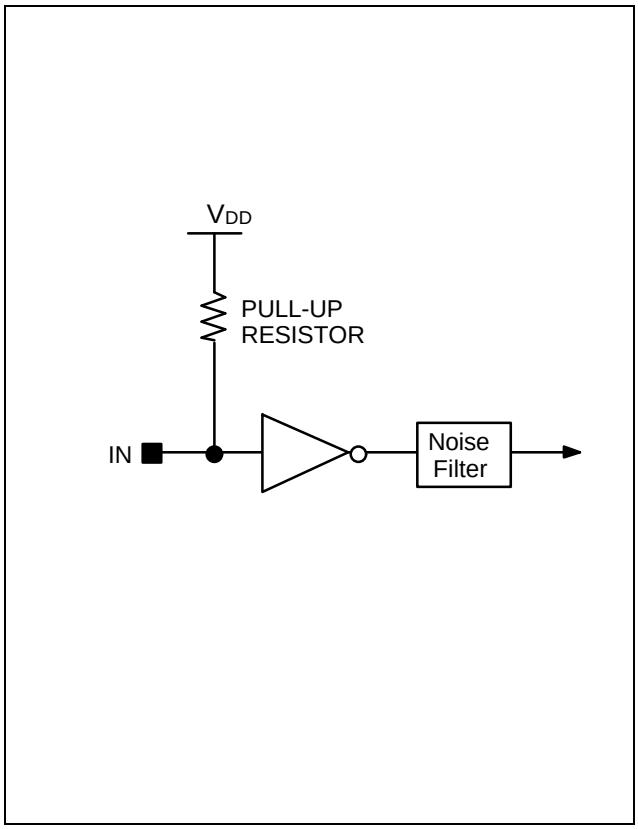


Figure 1-4. Pin Circuit Type A (RESET)

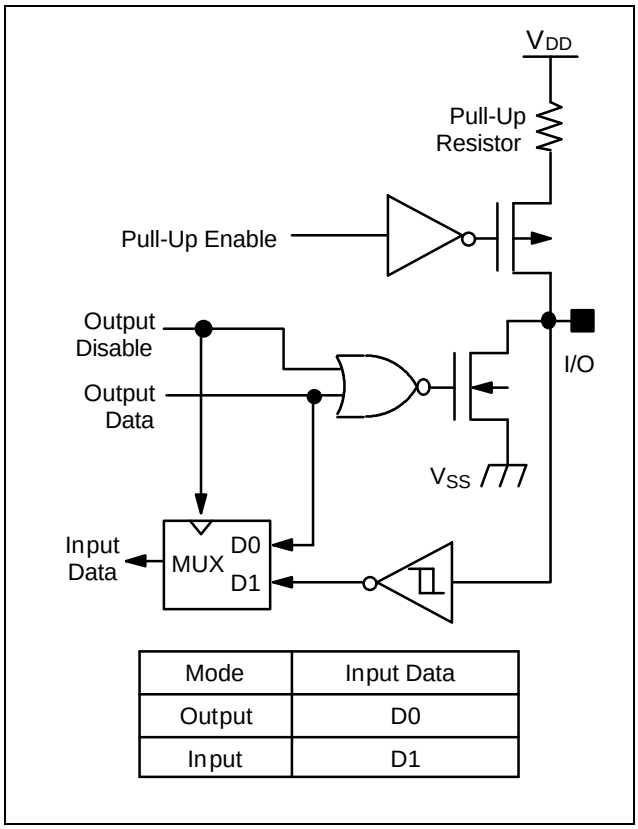
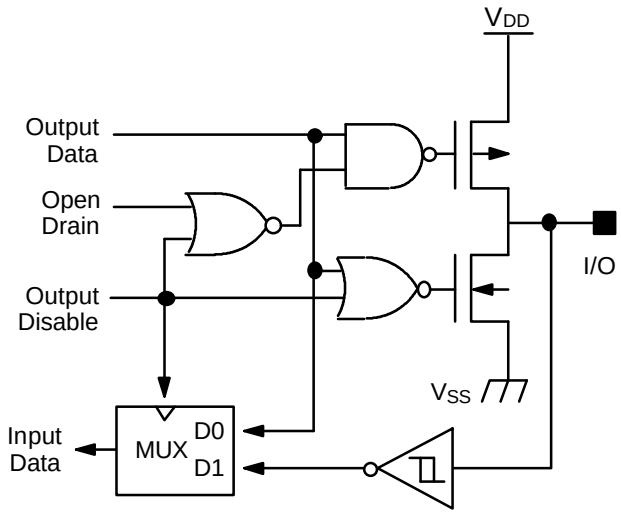
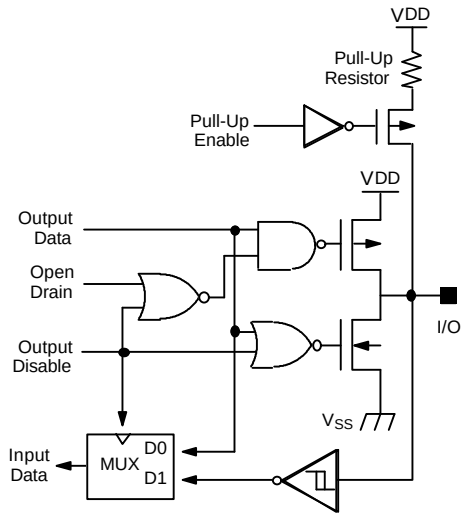


Figure 1-5. Pin Circuit Type B (Ports 0, 1 and 2)



Mode	Input Data
Output	D0
Input	D1

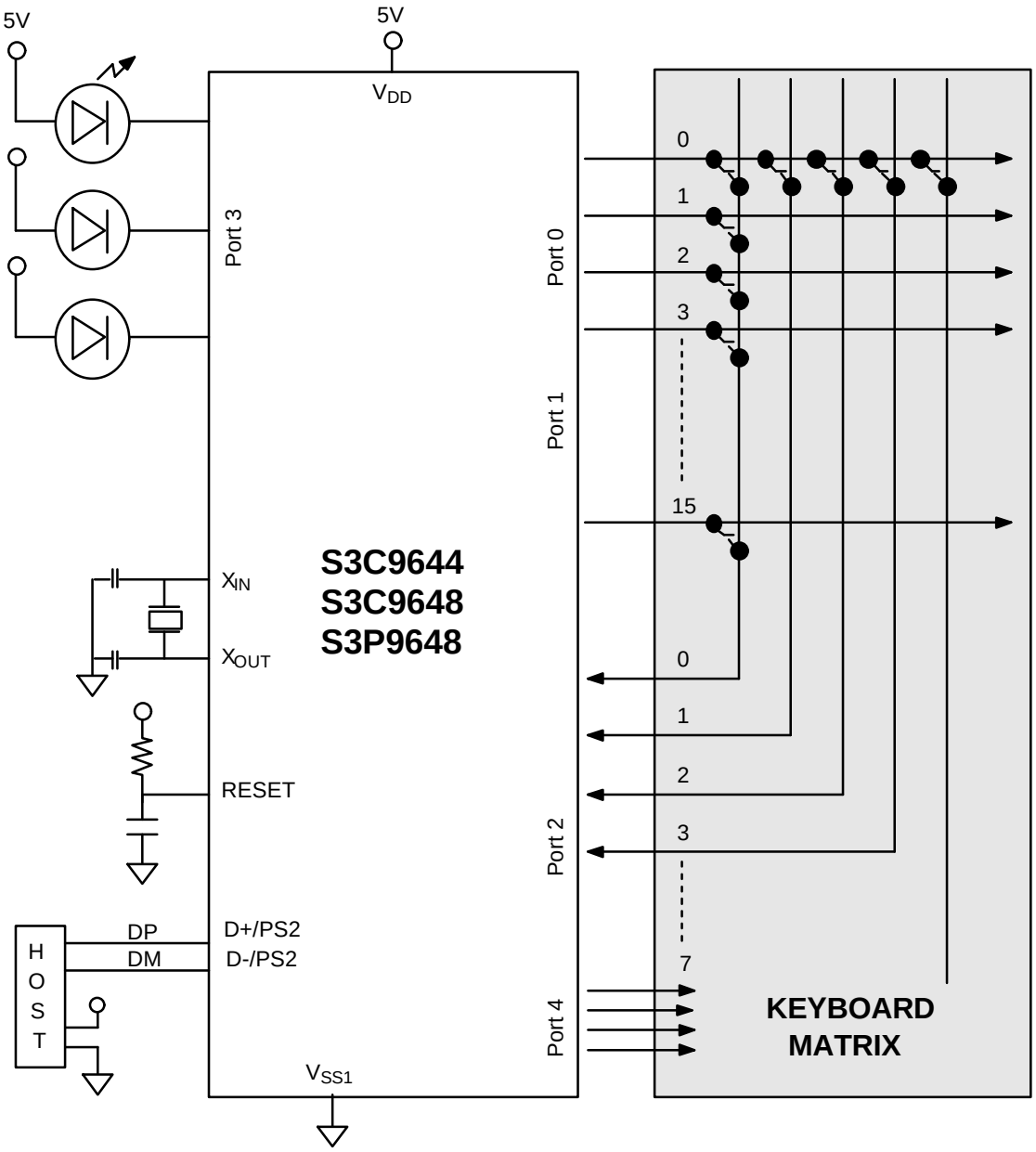
Figure 1-6. Pin Circuit Type C (Port 3)



Mode	Input Data
Output	D0
Input	D1

Figure 1-7. Pin Circuit Type D (Port 4)

APPLICATION CIRCUIT



NOTE: Port4 can use expend keyboard MATRIX.
D+/PS2, D-/PS2 can use PS2 keyboard interface (see PS2CONINT, page 4-25).
Port 4.2, 4.3 can use PS2 mouse interface.
Port 3 can use LED direct drive.

Figure 1-8. Keyboard Application Circuit Diagram

12 ELECTRICAL DATA

OVERVIEW

In this section, the following S3C9644/C9648/P9648 electrical characteristics are presented in tables and graphs:

— Absolute maximum ratings
— D.C. electrical characteristics
— Input/Output capacitance
— A.C. electrical characteristics
— Input timing for external interrupt (Ports 0, 2 and 4) D+/PS2, D-/PS2 : PS2 Mode Only
— Input timing for RESET
— Oscillator characteristics
— Oscillation stabilization time
— Clock timing measurement points at X_{IN}
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by a reset
— Stop mode release timing when initiated by an external interrupt
— Characteristic curves

Table 12-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	VDD	–	– 0.3 to + 6.5	V
Input Voltage	VIN	All input ports	– 0.3 to VDD + 0.3	V
Output Voltage	VO	All output ports	– 0.3 to VDD + 0.3	V
Output Current High	IOH	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	IOL	One I/O pin active	+ 30	mA
		Total pin current for ports 3	+ 100	
		Total pin current for ports 0, 1, 2, 4	+ 100	
Operating Temperature	TA	–	– 40 to + 85	°C
Storage Temperature	TSTG	–	– 65 to + 150	°C

Table 12-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 6 MHz (instruction clock = 1 MHz)	4.0	5.0	5.25	V
Input High Voltage	V_{IH1}	All input pins except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5		V_{DD}	
	V_{IH3}	RESET		0.5V_{DD}		
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
	V_{IL2}	RESET		0.5V_{DD}		
Output High Voltage	V_{OH}	I_{OH} = – 200 µA; All output ports except ports 0, 1 and 2, D+, D–	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 1 mA All output port except D+, D–	–	–	0.4	V
Output Low Current	I_{OL}	V_{OL} = 3V Port 3 only	8	15	23	mA
Input High Leakage Current	I_{LIH1} (3)	V_{IN} = V_{DD} All inputs except I_{LIH2} except D+, D–	–	–	3	µA
	I_{LIH2} (3)	V_{IN} = V_{DD} X_{IN}, X_{OUT}, RESET	–	–	20	µA
Input Low Leakage Current	I_{LIL1} (3)	V_{IN} = 0 V All inputs except I_{LIL2} except D+, D–	–	–	– 3	µA
	I_{LIL2} (3)	V_{IN} = 0 V X_{IN}, X_{OUT}, RESET	–	–	– 20	µA

Table 12-2. D.C. Electrical Characteristics (continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output High Leakage Current	I_{LOH} (1)	$V_{OUT} = V_{DD}$ All I/O pins and output pins except D+, D–	–	–	3	µA
Output Low Leakage Current	ILOL (1)	V_{OUT} = 0 V All I/O pins and output pins except D+, D–	–	–	– 3	µA
Pull-up Resistors	R_{L1}	V_{IN} = 0 V Ports 0, 1, 2, 4.2-3, Reset	25	50	100	kΩ
	R_{L2}	V_{IN} = 0 V; P4.0-1		2.4		
Supply Current (2)	I_{DD1}	Normal operation mode 6 MHz CPU clock	–	5.5	12	mA
	I_{DD2}	Idle mode; 6 MHz oscillator		2.2	5	mA
	I_{DD3}	Stop mode		180	300	µA

NOTES:
1. Except X_{IN} and X_{OUT}.
2. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
3. When USB Mode Only in 4.2 V to 5.25 V, D+ and D– satisfy the USB spec 1.0.

Table 12-3. Input/Output Capacitance

(T_A = – 40 °C to + 85 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are connected to V_{SS}	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 12-4. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.0 V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	P0, P2 and P4	–	200	–	ns
RESET Input Low Width	t_{RSL}	RESET	10	–	–	µs

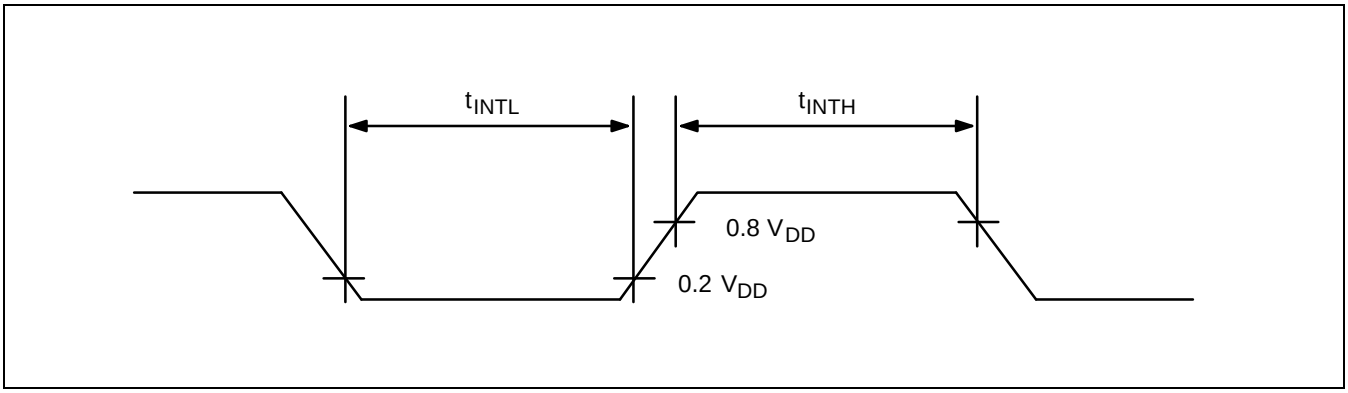


Figure 12-1. Input timing for external interrupt (Ports 0, 2, and 4)

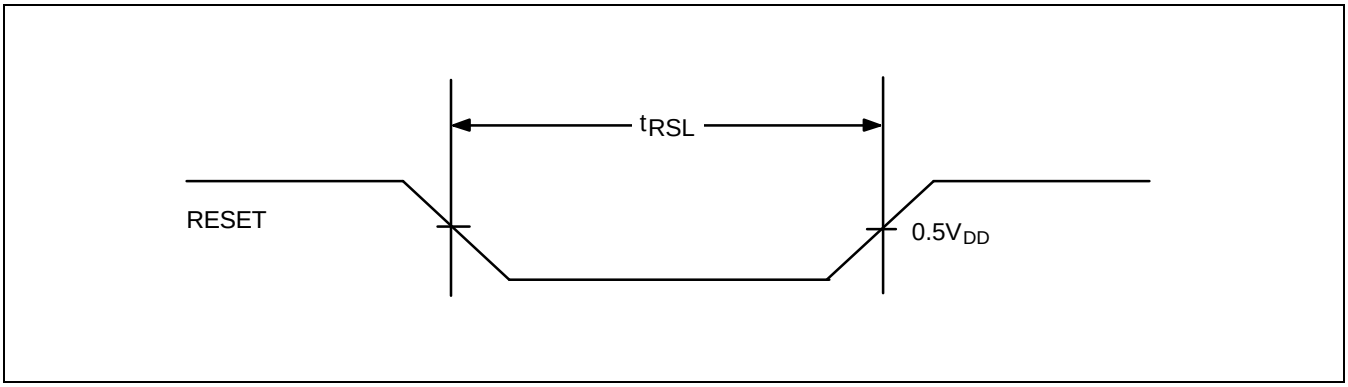


Figure 12-2. Input Timing for RESET

Table 12-5. Oscillator Characteristics

(T_A = – 40°C + 85°C, V_{DD} = 4.0 V to 5.25 V)

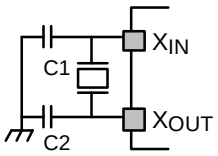
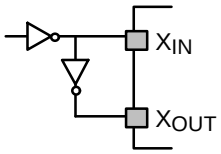
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal Main ceramic (f_{OSC})		Oscillation frequency	–	6.0	–	MHz
External clock		Oscillation frequency	–	6.0	–	

Table 12-6. Oscillation Stabilization Time

(T_A = – 40°C + 85°C, V_{DD} = 4.0 V to 5.25 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main Crystal	f_{OSC} = 6.0 MHz	–	–	10	ms
Main Ceramic	(Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.)				
Oscillator Stabilization Wait Time	t_{WAIT} stop mode release time by a reset	–	$2^{16}/f_{OSC}$	–	
	t_{WAIT} stop mode release time by an interrupt	–	(note)	–	

NOTE: The oscillator stabilization wait time, t_{WAIT}, is determined by the setting in the basic timer control register, BTCON.

Table 12-7. Data Retention Supply Voltage in Stop Mode

(T_A = – 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	2.0	–	6	V
Data Retention Supply Current	I_{DDDR}	Stop mode; V_{DDDR} = 2.0 V	–	–	300	µA

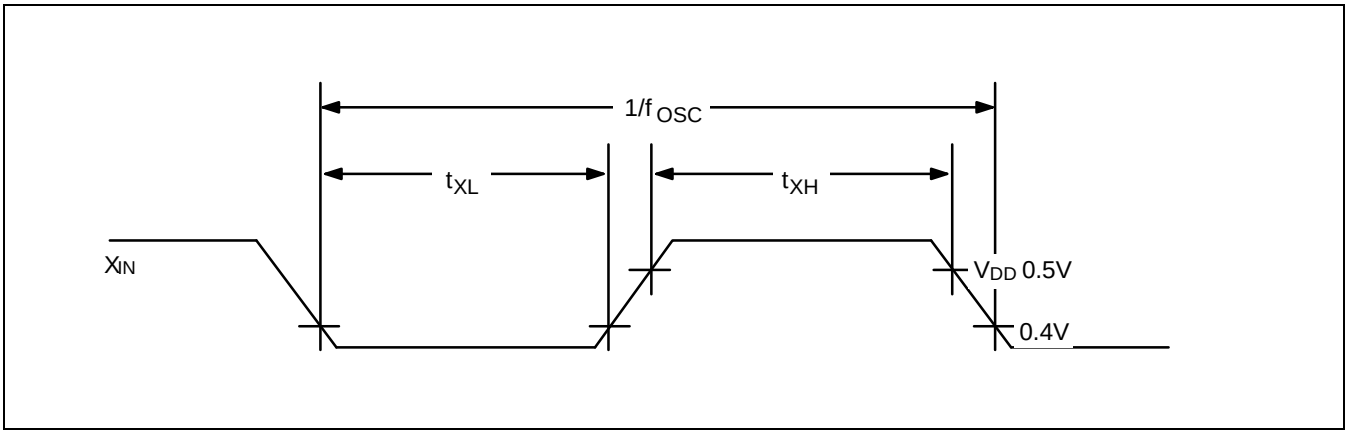


Figure 12-3. Clock Timing Measurement Points at X_{IN}

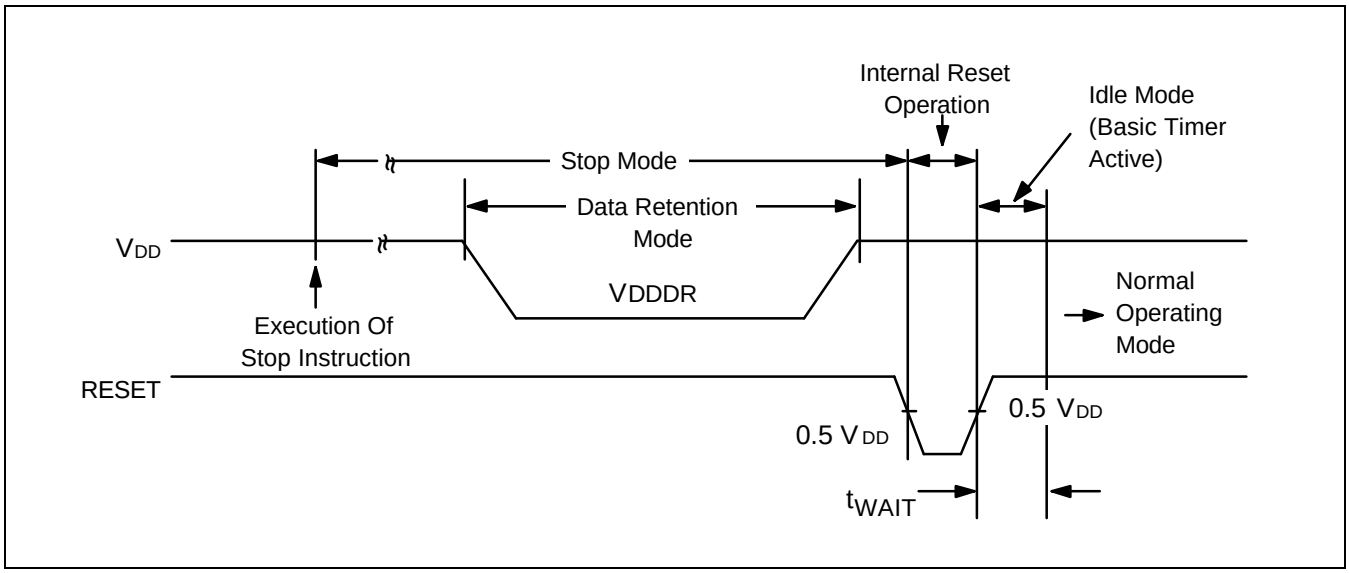


Figure 12-4. Stop Mode Release Timing When Initiated by a Reset

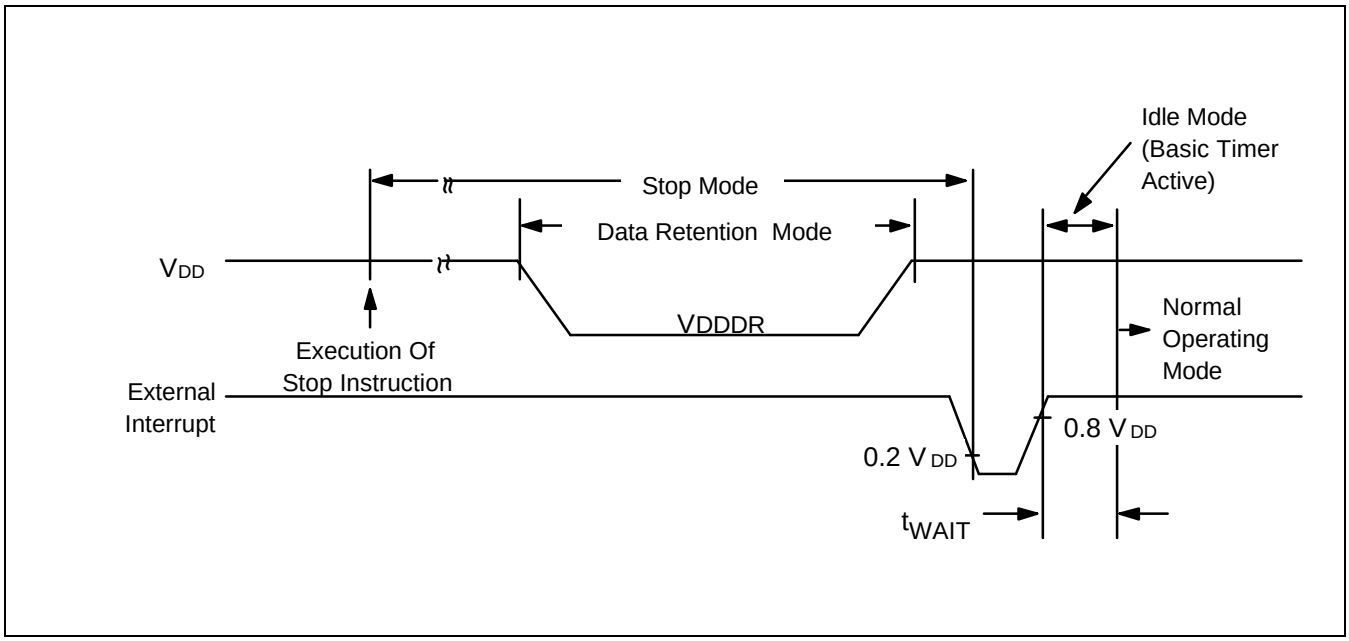


Figure 12-5. Stop Mode Release Timing When Initiated by an External Interrupt

Table 12-8. Low Speed USB Electrical Characteristics

(T_A = – 40°C to + 85°C, Voltage Regulator Output V_{33out} = 2.8 V to 3.5 V, typ 3,3 V)

Parameter	Symbol	Conditions	Min	Max	Unit
Transition Time:					
Rise Time	Tr	CL = 50 pF	75	–	ns
		CL = 350 pF	–	300	
Fall Time	Tf	CL = 50 pF	75	–	
		CL = 350 pF	–	300	
Rise/Fall Time Matching	Trfm	(Tr/Tf) CL = 50 pF	80	120	%
Output Signal Crossover Voltage	Vcrs	CL = 50 pF	1.3	2.0	V
Voltage Regulator Output Voltage	V33OUT	with V33OUT to GND 0.1 µF capacitor	2.8	3.5	V

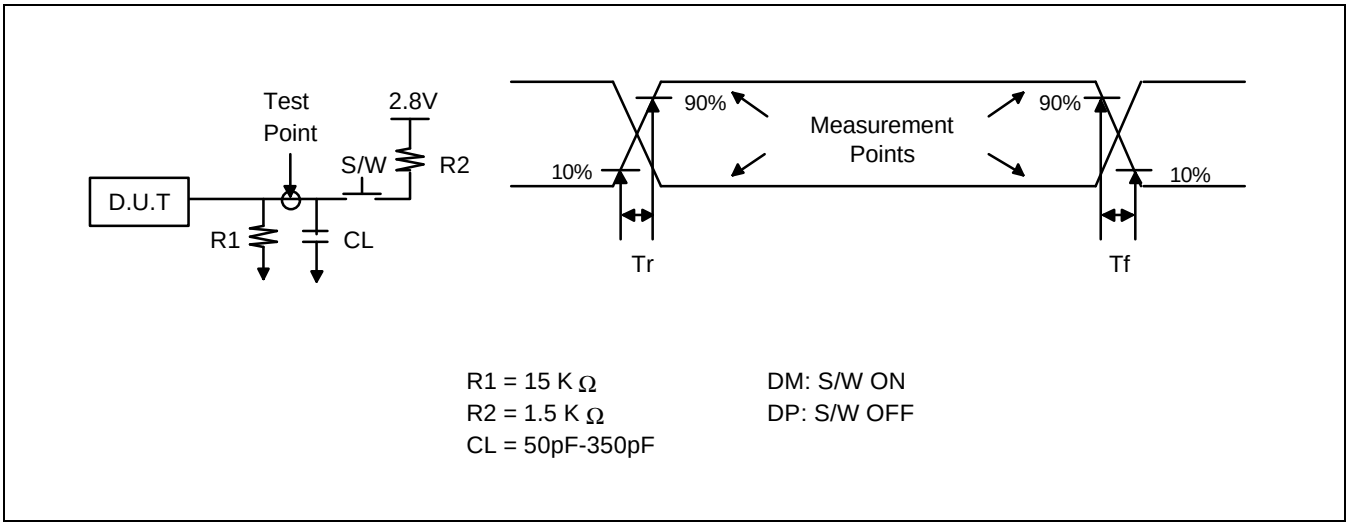


Figure 12-6. USB Data Signal Rise and Fall Time

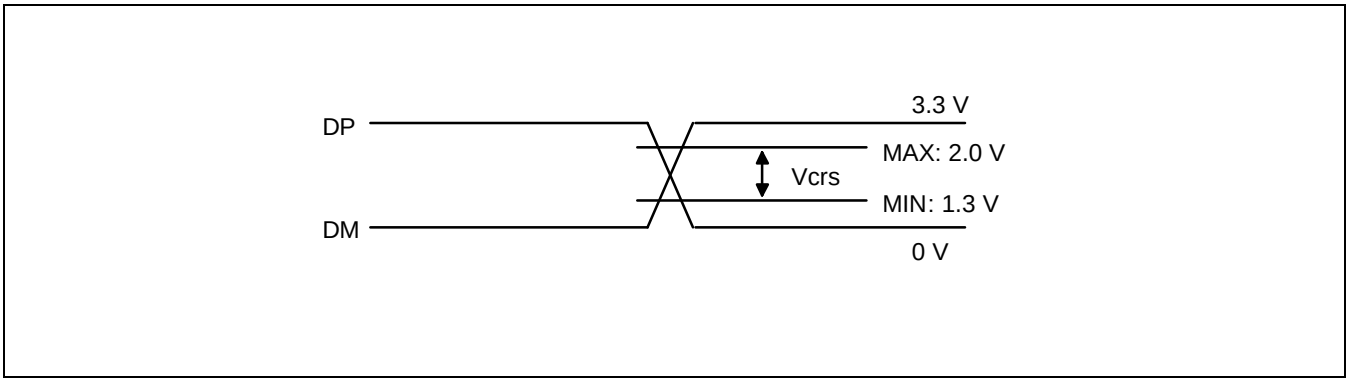


Figure 12-7. USB Output Signal Crossover Point Voltage

13 MECHANICAL DATA

OVERVIEW

The S3C9644/C9648/P9648 is available in a 42-pin SDIP package (Samsung: 42-SDIP-600) and a 44-pin QFP package (44-QFP-1010B). Package dimensions are shown in Figures 13-1 and 13-2.

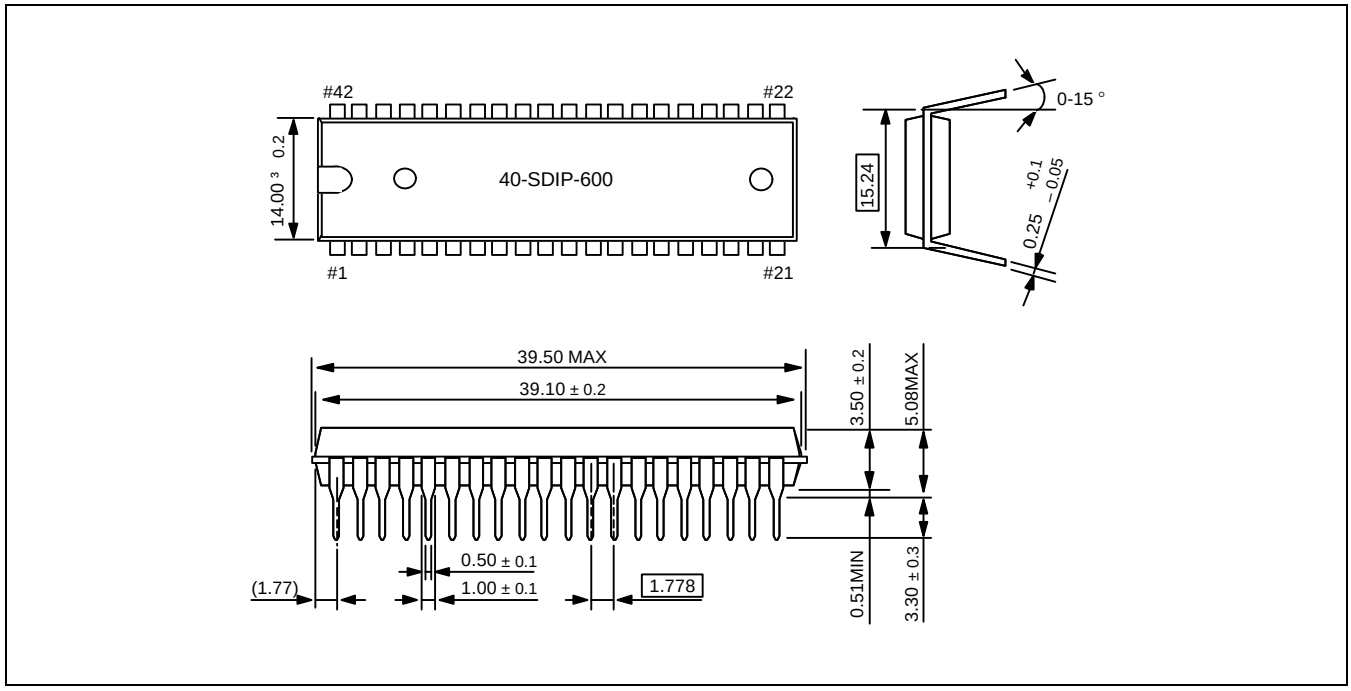
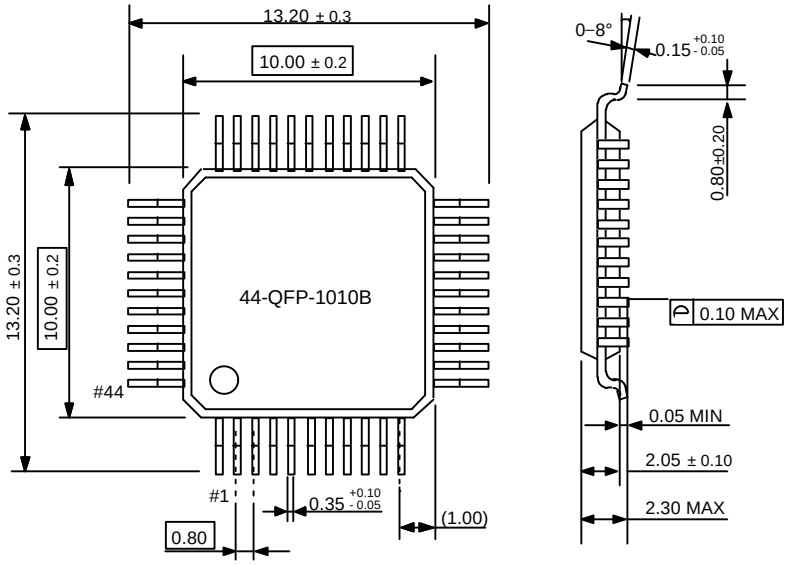


Figure 13-1. 42-Pin SDIP Package Mechanical Data (42-SDIP-600)



NOTE: Dimensions are in millimeters.

Figure 13-2. 44-Pin QFP Package Mechanical Data (44-QFP-1010B)

14 S3P9648 OTP

OVERVIEW

The S3P9648 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C9644/C9648 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P9648 is fully compatible with the S3C9644/C9648, both in function and in pin configuration. Because of its simple programming requirements, the S3P9648 is ideal for use as an evaluation chip for the S3C9644/C9648.

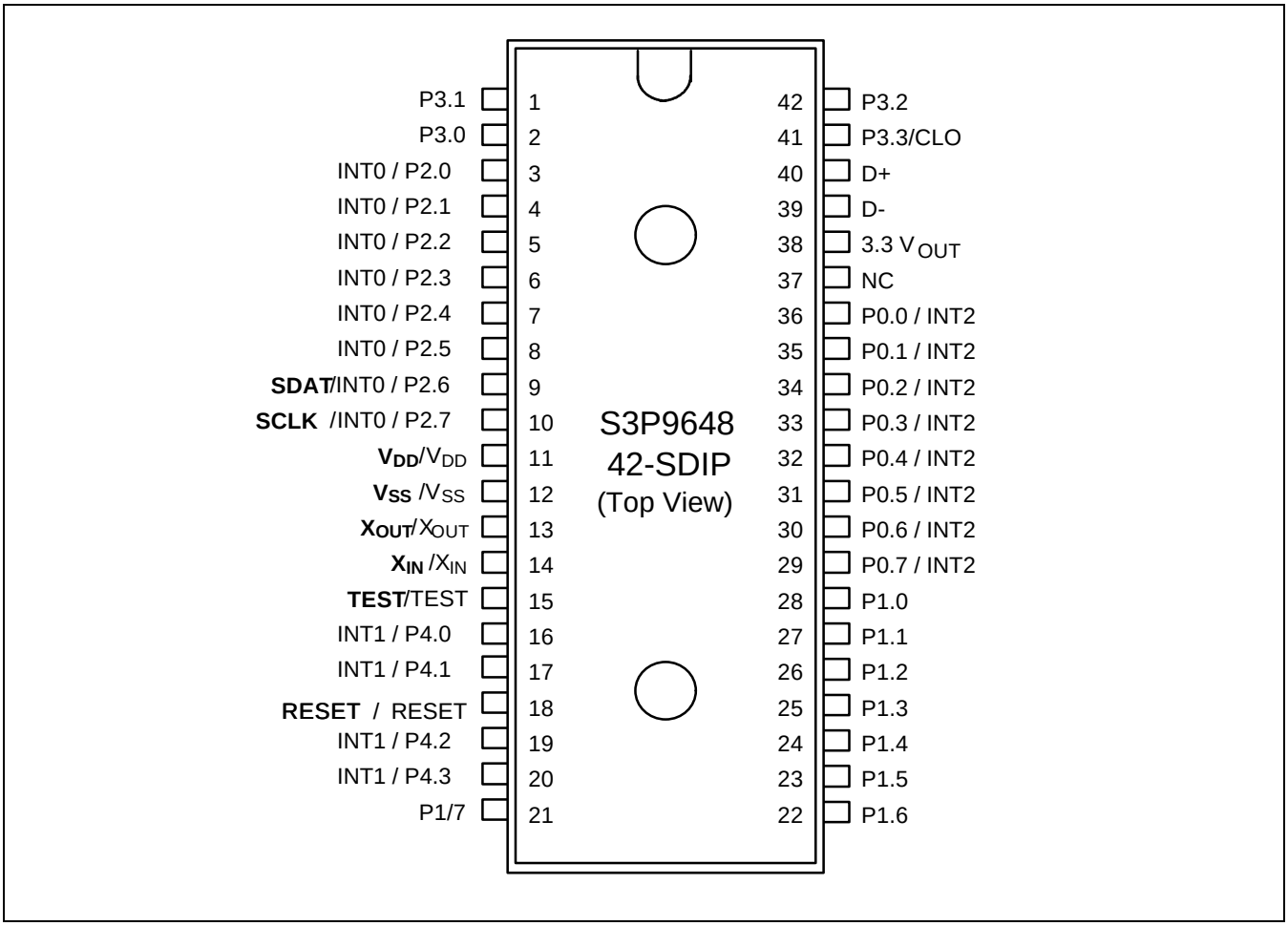


Figure 14-1. S3P9648 Pin Assignments (42-SDIP Package)

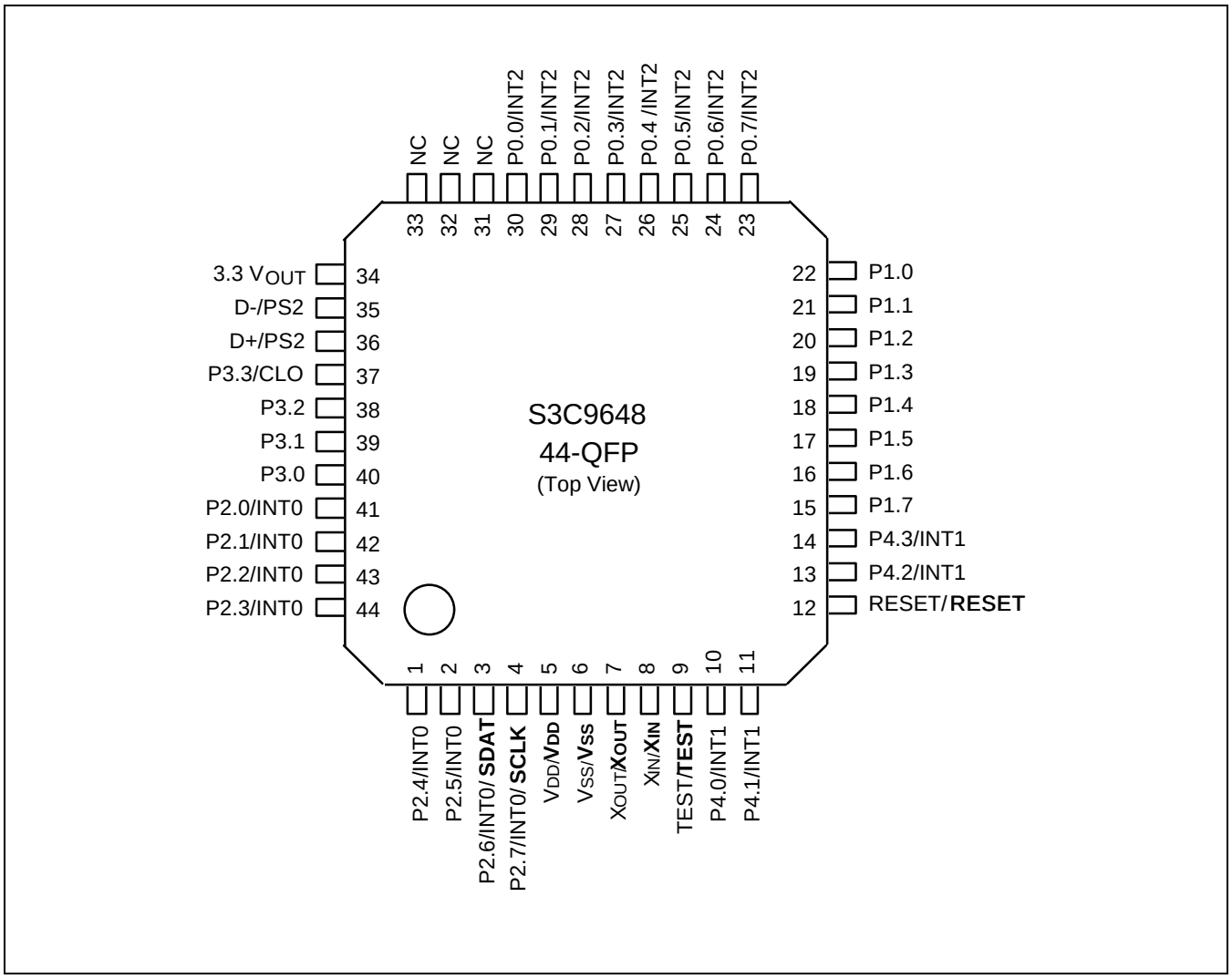


Figure 14-2. S3P9648 Pin Assignments (44-QFP Package)

Table 14-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P2.6	SDAT	9 (3)	I/O	Serial DATa Pin (Output when reading, Input when writing) Input and Push-pull Output Port can be assigned
P2.7	SCLK	10 (4)	I/O	Serial CLocK Pin (Input Only Pin)
TEST	TEST	15 (9)	I	Chip Initialization and EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5 V is applied and when reading.
RESET	RESET	18 (12)	I	0 V: OTP write and test mode 5 V: Operating mode
V_{DD} / V_{SS}	V_{DD} / V_{SS}	11(5)/12(6)	–	Logic Power Supply Pin.

NOTE: ( ) means 44 QFP package.

Table 14-2. Comparison of S3P9648 and S3C9644/C9648 Features

Characteristic	S3P9648	S3C9644/C9648
Program Memory	8-Kbyte EPROM	8-Kbyte mask ROM
Operating Voltage (V_{DD})	4.0 V to 5.25 V	4.0 V to 5.25 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (RESET) = 12.5 V	
Pin Configuration	42 SDIP/44 QFP	42 SDIP/44 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (RESET) pin of the S3P9648, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 14-3 below.

Table 14-3. Operating Mode Selection Criteria

V_{DD}	VPP (RESET)	REG/ MEM	ADDRESS (A15-A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

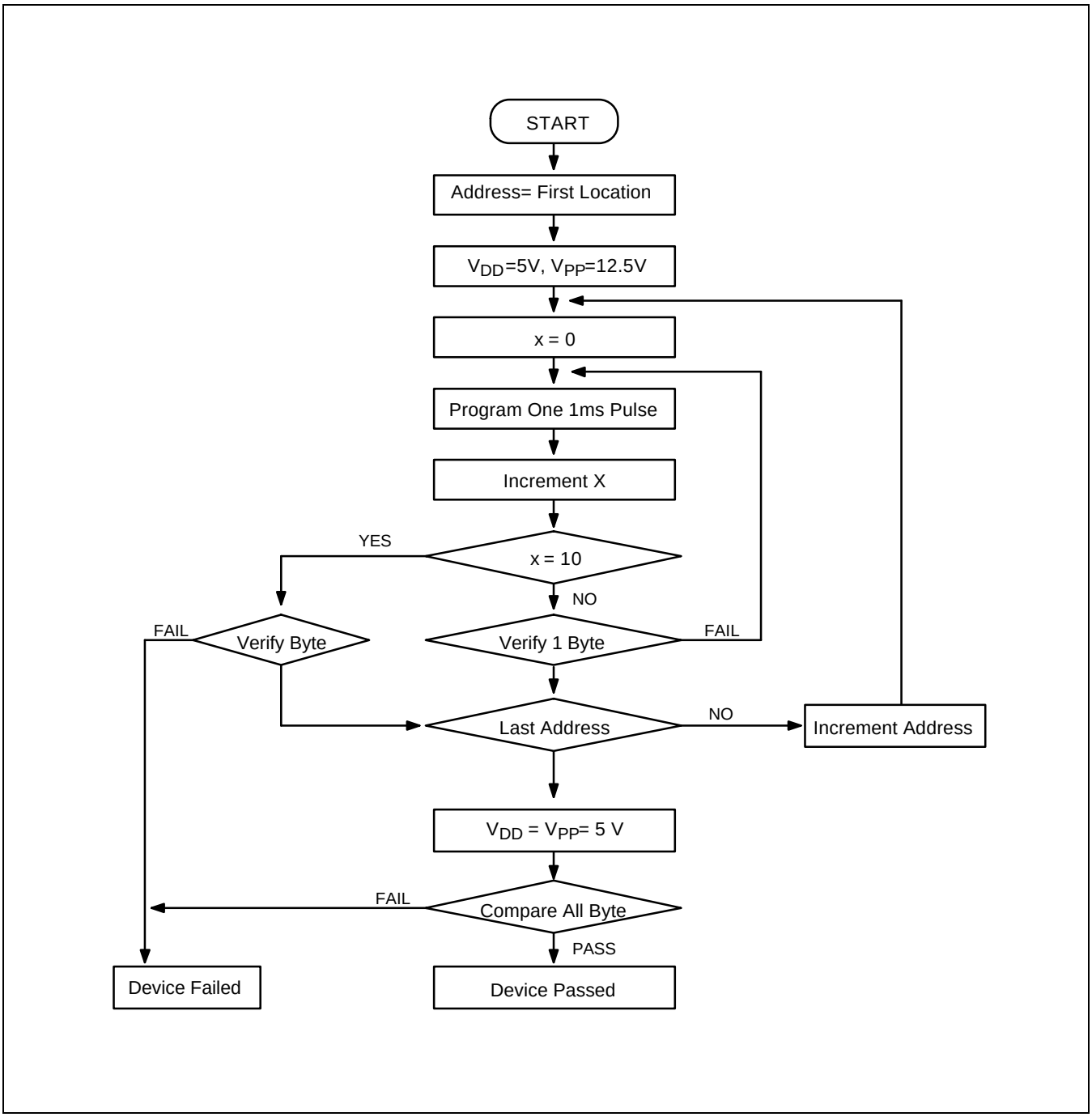


Figure 14-3. OTP Programming Algorithm

Table 14-4. D.C. Electrical Characteristics

(T_A = – 40_C to + 85_C, V_{DD} = 4.0 V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current (note)	I_{DD1}	Normal mode; 6 MHz CPU clock	–	5.5	12	mA
	I_{DD2}	Idle mode; 6 MHz CPU clock		2.2	5	
	I_{DD3}	Stop mode		180	300	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.