HY51V4100B Series

4M × 1bit CMOS DRAM

DESCRIPTION

The HY51V4100B is the new generation and fast dynamic RAM organized 4,194,304x1-bit. The HY51V4100B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY51V4100B to be packaged in a standard 20/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 3.3V ±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 1.08mW (L-part)
  Max. CMOS standby 0.72mW (L-part)
  3.6mW
  Max. TTL standby 7.2mW
  Max. Self refresh 0.72mW(SL-part)
  Max. operating

Speed	Power
60	324.0mW
70	288.0mW
80	252.0mW

- **Single power supply of 3.3V±10%**
- **TTL compatible inputs and outputs**
- **Fast access and cycle time**

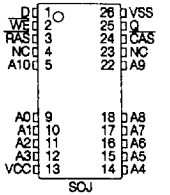
Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

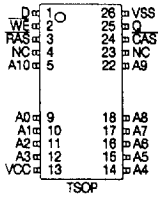
- **Fast page mode operation**
- **Multi-bit test capability**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden & Self refresh capability**
- **1024 refresh cycles / 128ms (L-part)**
  1024 refresh cycles / 16ms

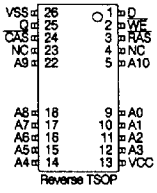
PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A10	Address input
D	Data input
Q	Data Output
Vcc	Power (+3.3V)
Vss	Ground

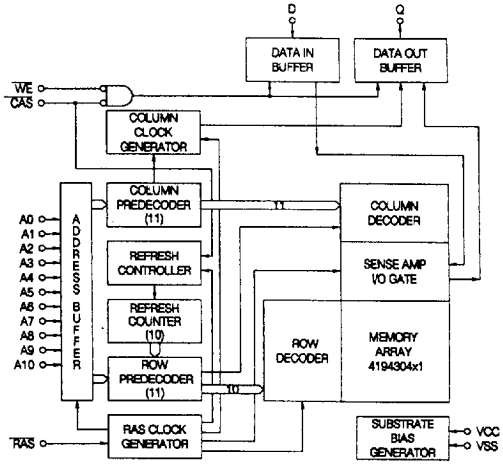
PIN CONNECTION







BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
V_{CC}	Voltage on Vcc Relative to Vss	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	20	mA
P_D	Power Dissipation	0.90	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

NOTE:Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

NOTE: All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}$+0.3V, All other pins not under test = V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	Vcc Supply Current, Operating	t_{RC} = t_{RC} (min.)	60 70 80	- - -	90 80 70	mA	1,2,3
I_{CC2}	Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}		-	2	mA	
I_{CC3}	Vcc Supply Current, $\overline{RAS}$-only refresh	t_{RC} = t_{RC} (min.)	60 70 80	- - -	90 80 70	mA	1,3
I_{CC4}	Vcc Supply Current, Fast Page mode	t_{PC} = t_{PC} (min.)	60 70 80	- - -	60 50 40	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ Vcc-0.2V	 L-part	- -	1 200	mA µA	 5
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before- $\overline{RAS}$ refresh	t_{RC} = t_{RC} (min.)	60 70 80	- - -	90 80 70	mA	1,3
I_{CC7}	Vcc Supply Current, Battery Back up (L-part only)	t_{RC} = 125µs, $t_{RAS} \le$ 1µs $\overline{CAS}$ = CBR cycling or 0.2V $\overline{WE}$ = Vcc-0.2V or 0.2V A0-A10 = Vcc-0.2V or 0.2V D = Vcc-0.2V, 0.2V or open Q = open		-	300	µ A	1,4,5
I_{CC8}	Vcc Supply Current, Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V other pins same as I_{CC7}		-	200	µA	6
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2.0mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rates.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$ =V_{IL}. I_{CC4}, Address can be changed maximum once while and $\overline{CAS}$=V_{IH}.
4. Only t_{RAS}(max.) =1µs is applied to refresh of battery backup but t_{RAS}(max.) =10µs is applied to normal functional operation .
5. I_{CC5}(max.) =200µA and I_{CC7} are applied to L-parts (HY51V4100BLJ, HY51V4100BLT, HY51V4100BLR, HY51V4100BSLJ, HY51V4100BSLT, HY51V4100BSLR)
6. I_{CC8} is applied to SL-parts only (HY51V4100BSLJ, HY51V4100BSLT and HY51V4100BSLR).

AC CHARACTERISTICS

(TA=0C to 70C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.) NOTE :1,2,3,13

#	SYMBOL	PARAMETER	HY51V4100BJ/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	130	-	155	-	175	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	60	-	70	-	80	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge		35		40		45	ns	4,15
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	20	0	25	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
17	tCAS	$\overline{CAS}$ Pulse width	15	10K	20	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	20	40	ns	.10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	20	-	ns	14
32	tWCR	Write Command Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	20	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	20	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	45	-	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	12
		L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V4100BJ/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	-	20	-	20	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	-	70	-	80	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	30	-	35	-	40	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	20	-	25	-	30	-	ns	17
48	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	8
49	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
50	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	-	10	-	10	-	ns	
51	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
52	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
53	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
54	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
55	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh)	130	-	150	-	180	-	ns	
56	tCHS	$\overline{CAS}$ Hold Time from $\overline{RAS}$ (Self Refresh)	-50	-	-50	-	-50	-	ns	

AC CHARACTERISTICS IN TEST MODE

NOTE 18

#	SYMBOL	PARAMETER	HY51V4100BJ/BT/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	115	-	135	-	155	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	135	-	160	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	55	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	65	-	75	-	85	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	65	-	75	-	85	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	20	-	25	-	30	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	50	ns	4
13	tRAS	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	65	200K	75	200K	85	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	20	-	25	-	25	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	-	25	-	25	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	65	-	75	-	85	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	35	-	40	-	45	-	ns	8

NOTE:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. If $\overline{RAS}$=Vss during power-up, the HY51V4100B could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 1 TTL loads and 100pF.
5. t_{OFF}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.)=128ms is applied to L-Parts(HY51V4100BLJ/BSLJ, HY51V4100BLT/BSLT and HY51V4100BLR/BSLR).
12. A burst of 1024$\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 16ms(128ms for L-part) after exiting self refresh.
13. When $\overline{CAS}$ goes low, 1-bits data are written into the device.
14. These parameters are determined by the earlier falling edge of $\overline{CAS}$.
15. These parameters are determined by the later rising edge of $\overline{CAS}$.
16. t_{CWL} must be satisfied by $\overline{CAS}$ for 1-bits access cycles.
17. t_{CP} and t_{CPT} are measured when $\overline{CAS}$ is high state.
18. These specificaitons are applied to the test Mode.

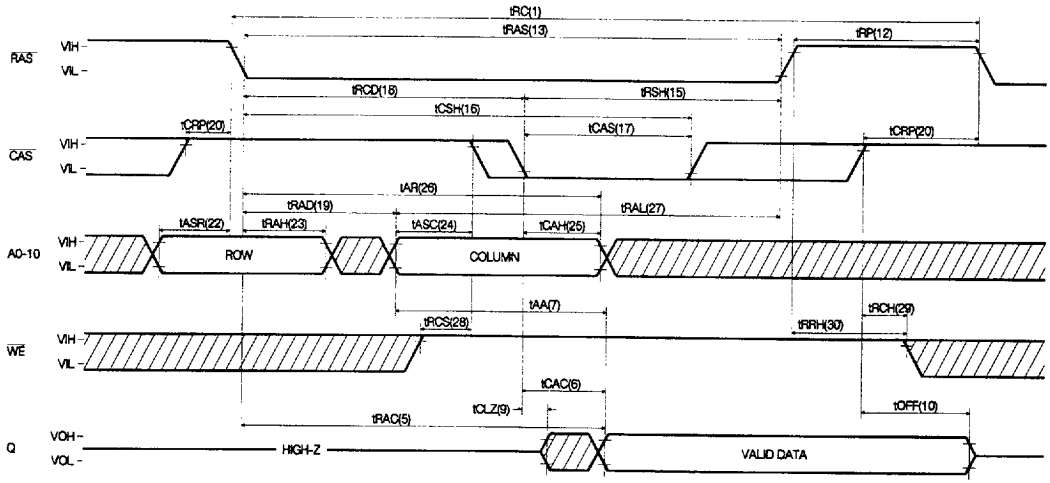
CAPACITANCE

(T_A=25°C, Vcc=3.3V±10%, Vss=0V, f=1MHz, unless otherwise noted.)

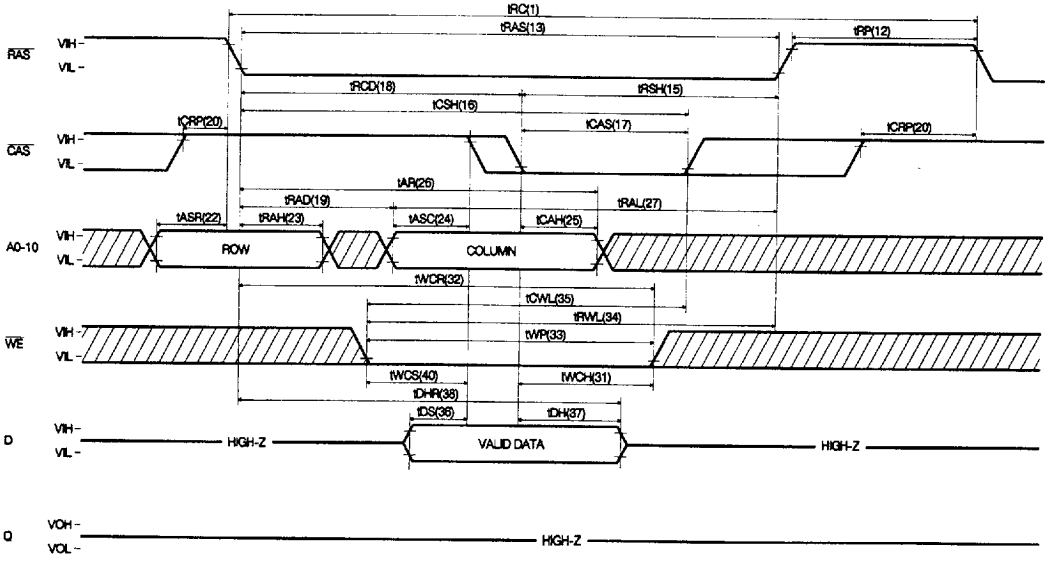
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (Q)	-	7	pF

TIMING DIAGRAM

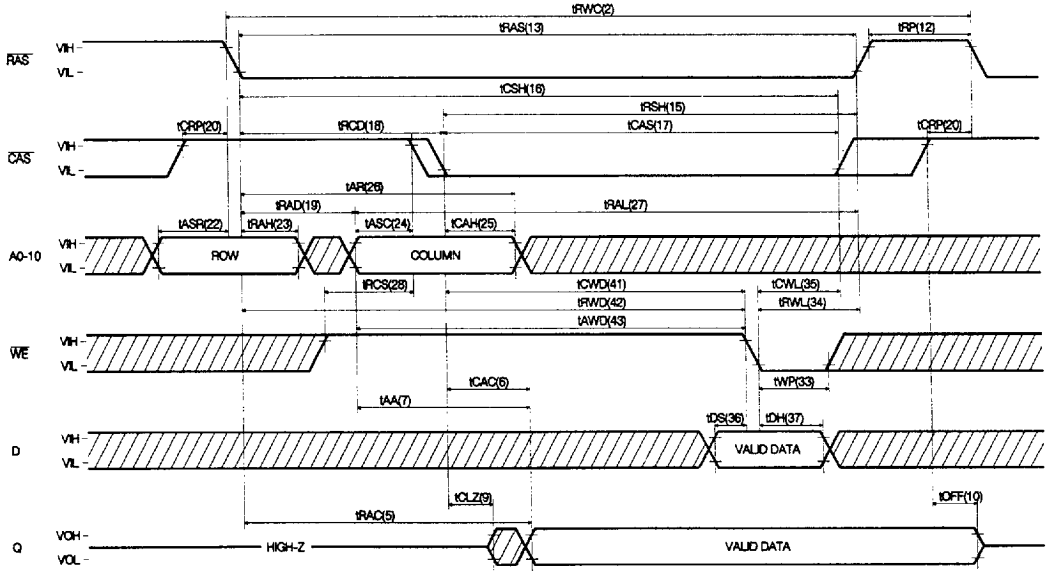
READ CYCLE



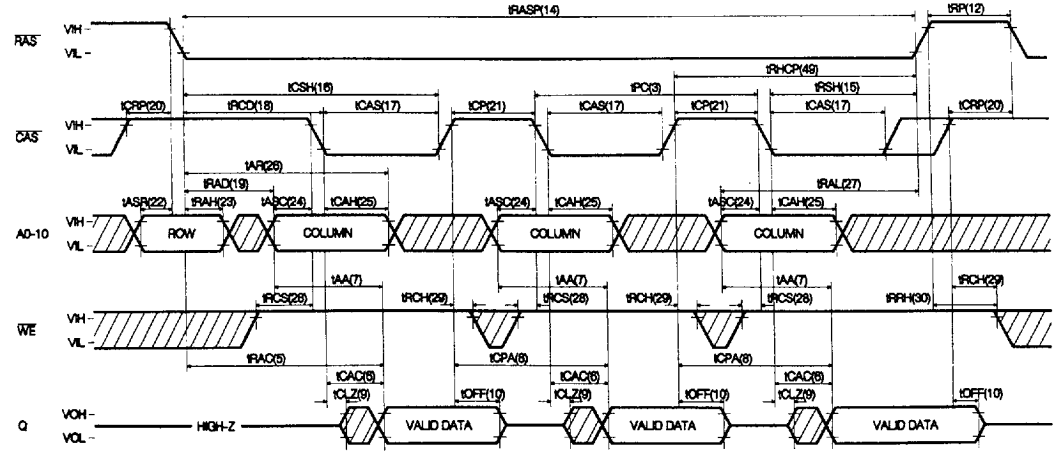
EARLY WRITE CYCLE



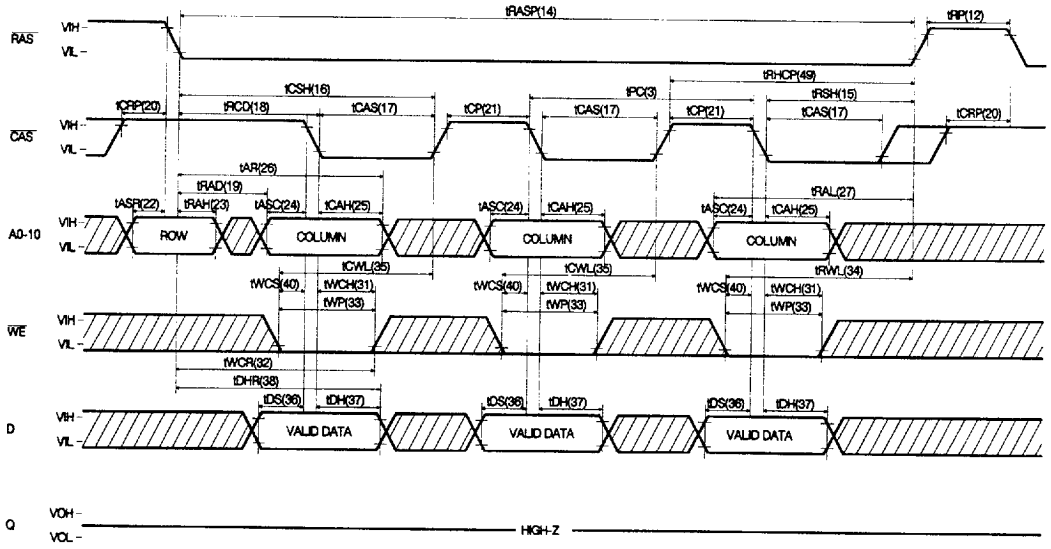
READ-MODIFY-WRITE CYCLE



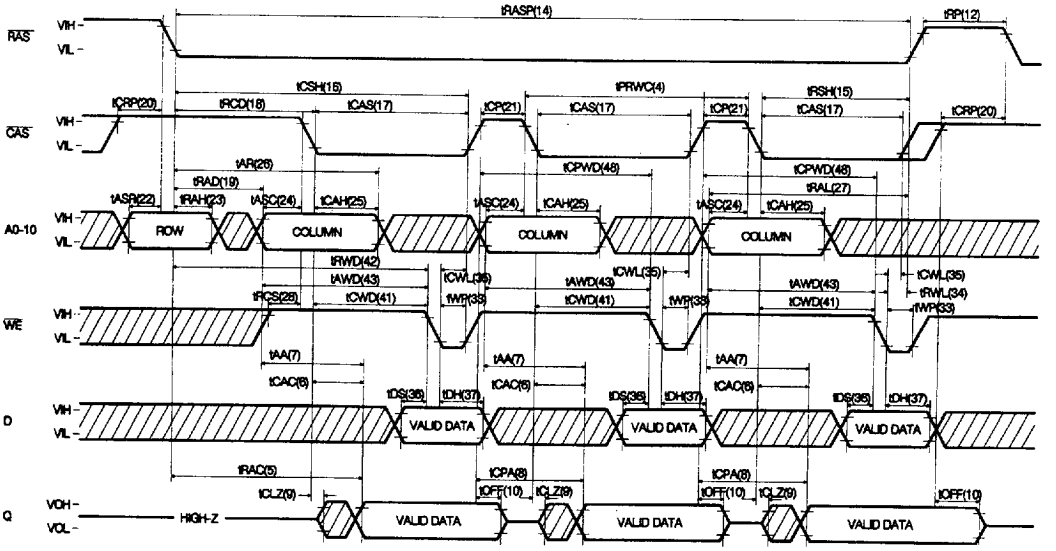
FAST PAGE MODE READ CYCLE



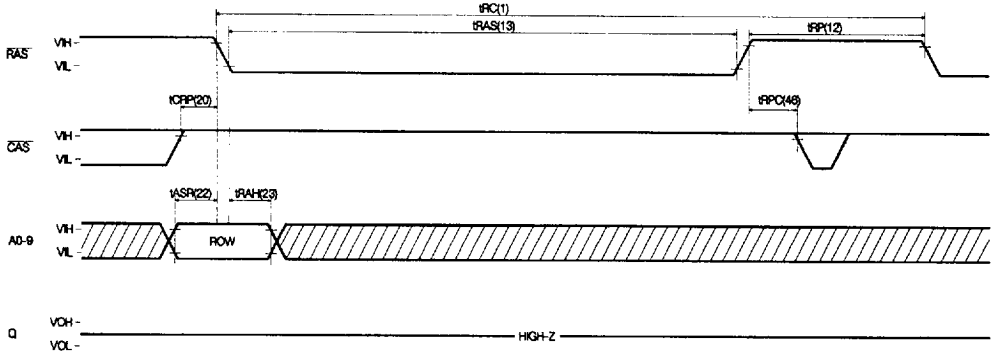
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

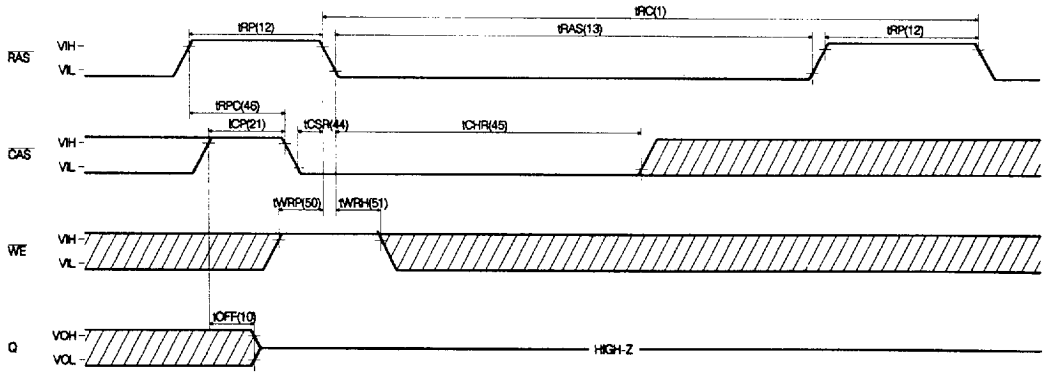


$\overline{RAS}$-ONLY REFRESH CYCLE



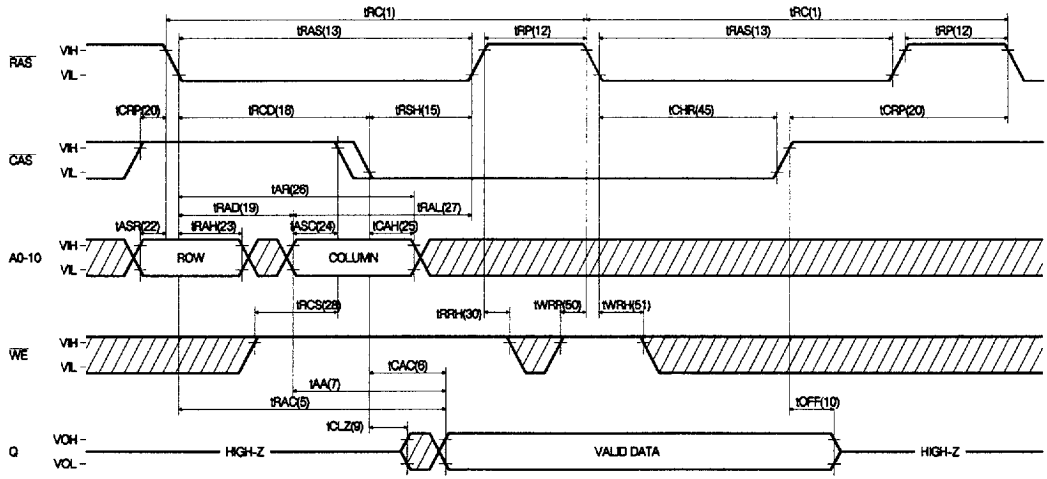
NOTE : $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

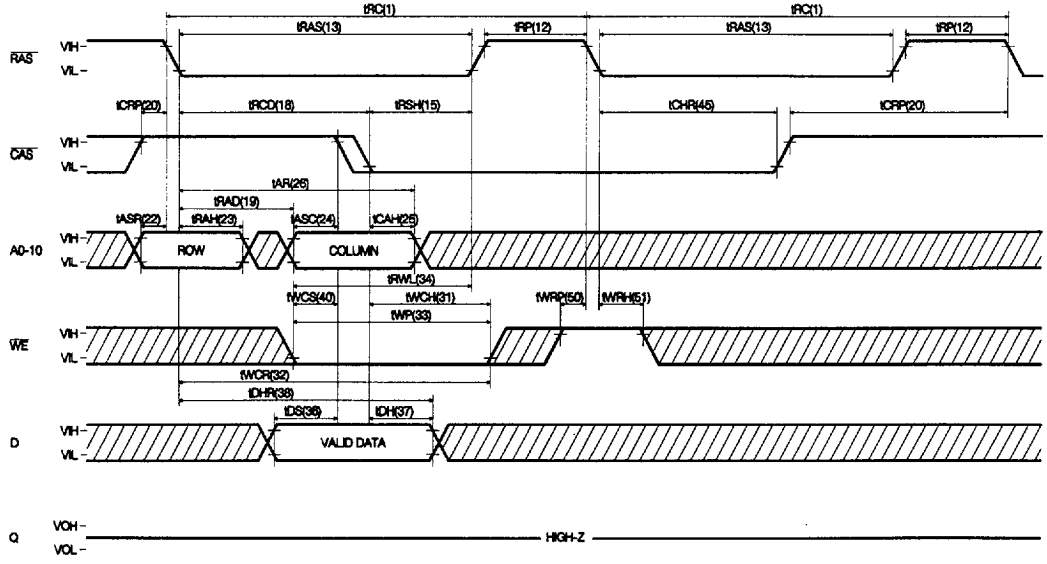


NOTE : A0-10 = "H" or "L"

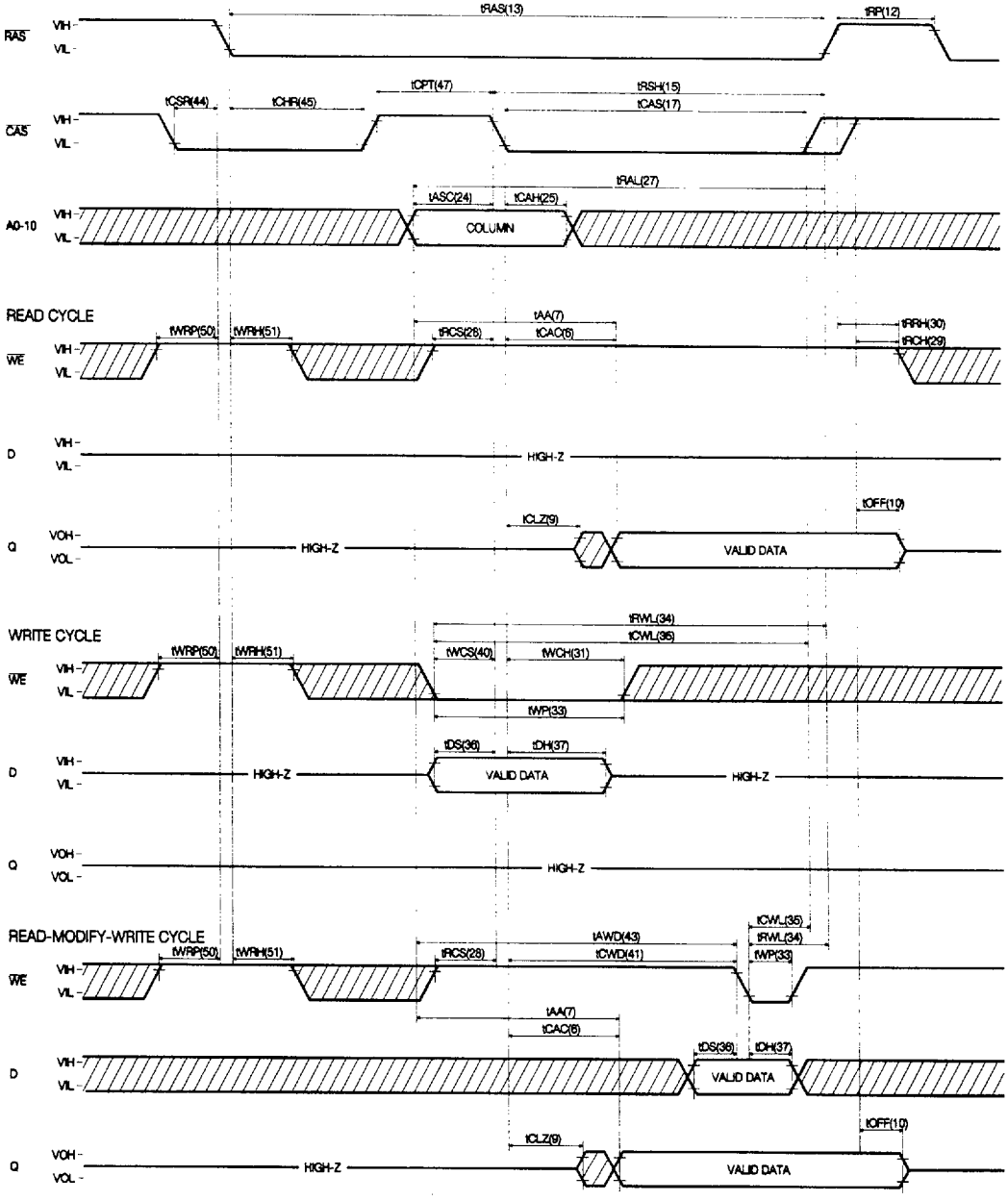
HIDDEN REFRESH CYCLE (READ)



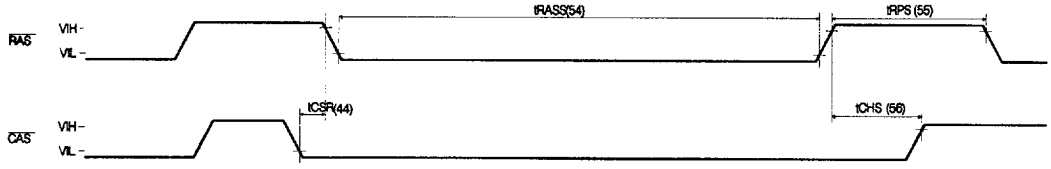
HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



CAS-BEFORE-RAS SELF REFRESH CYCLE

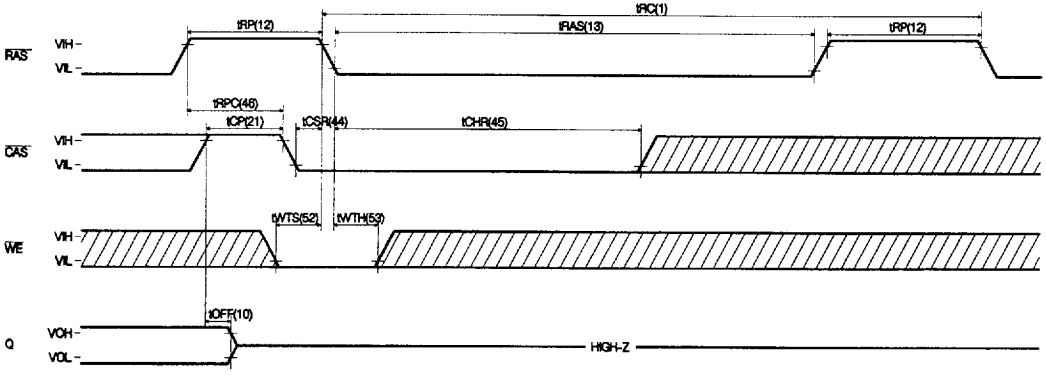


NOTE:A0-10, WE = 'H' or 'L"

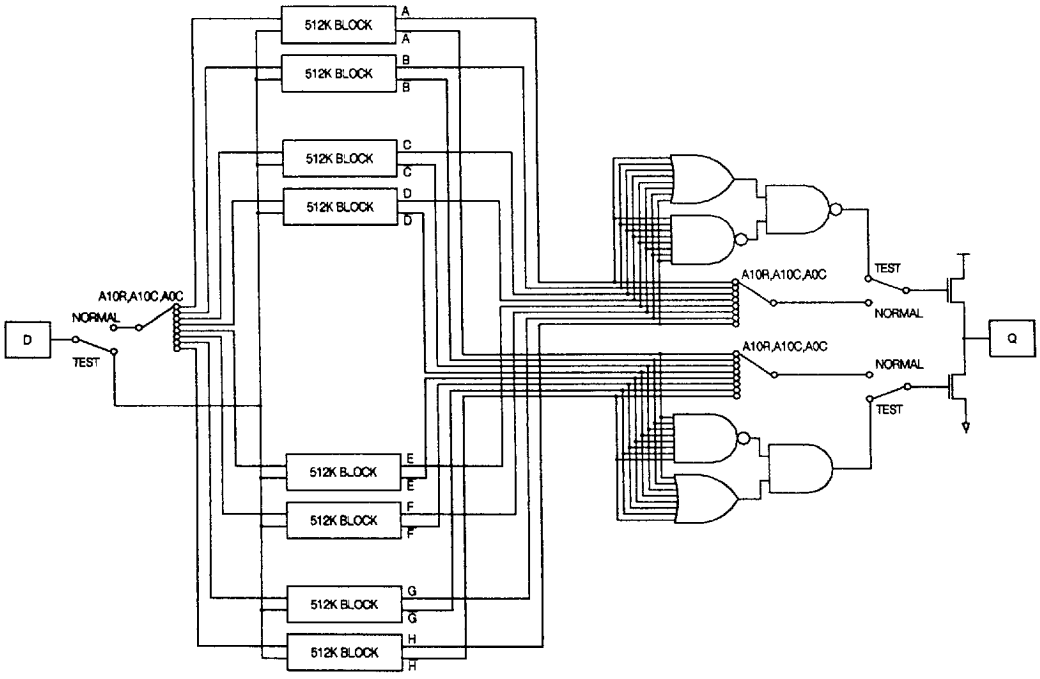
TEST MODE

The HY51V4100B is a DRAM organized 4,194,304 x 1-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved in the same way. Row address A10 and column address A0 and A10 are not used. If, upon reading, all bit are equal (all "1"s or "0"s), the Q pin indicates a "1". If they are not equal, the Q pin indicates a "0". The diagram below shows the timing of the HY51V4100B to enter Test Mode. In Test Mode, the 4Mx1 DRAM can be tested as if it were a 512Kx1 DRAM. WE, CAS-before-RAS cycle (Test Mode In Cycle) puts the HY51V4100B into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time. (1/8 in case of N test pattern).

TEST MODE IN CYCLE

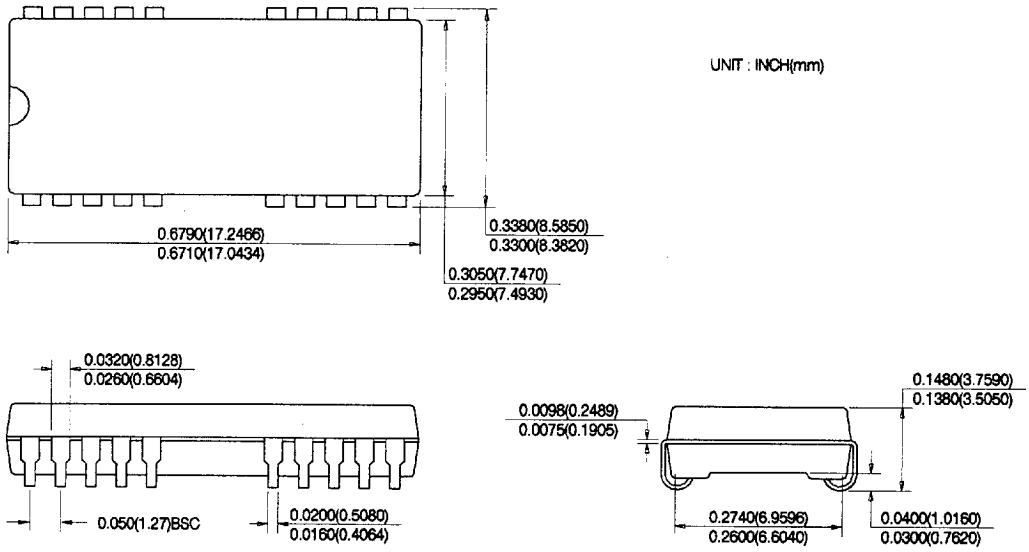


BLOCK DIAGRAM IN TEST MODE

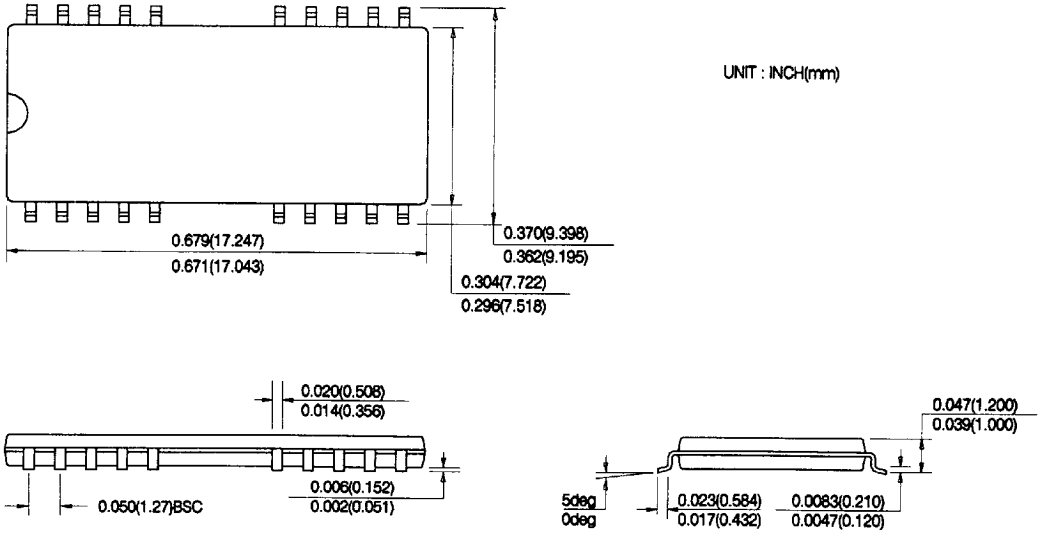


PACKAGE INFORMATION

300 mil 20/26 pin Small Out line J-form Package (J)



300 mil 20/26 pin Thin Small Outline Package (T) (R)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY51V4100BJ	60/70/80		SOJ
HY51V4100BLJ	60/70/80	L-part	SOJ
HY51V4100BSLJ	60/70/80	SL-part	SOJ
HY51V4100BT	60/70/80		TSOP-II
HY51V4100BLT	60/70/80	L-part	TSOP-II
HY51V4100BSLT	60/70/80	SL-part	TSOP-II
HY51V4100BR	60/70/80		TSOP-II(R)
HY51V4100BLR	60/70/80	L-part	TSOP-II(R)
HY51V4100BSLR	60/70/80	SL-part	TSOP-II(R)