NEC Electronics Inc.

μPD431016
65,536 x 16-Bit Static CMOS RAM

T-46-23-14

Description

The μPD431016 is a 65,536-word by 16-bit static RAM fabricated with advanced silicon-gate technology, unique CMOS peripheral circuits, and N-channel memory cells. It is suitable for cache memory and buffer memory applications where high speed, high density, and wide I/O SRAMs are required.

The μPD431016 operates with low power from a single +5-volt supply. No clock or refreshing is required. The plastic package is a standard 44-pin SOJ or TSOP.

Features

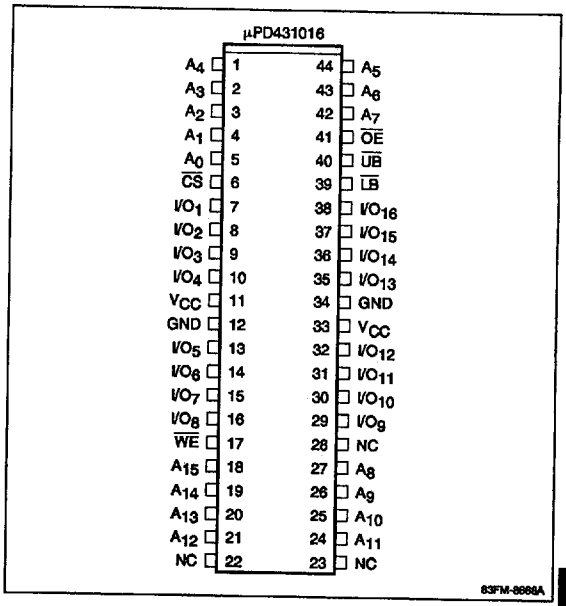
- 65,536-word x 16-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Output buffer control: $\overline{OE}$
- Data byte control: $\overline{LB}$, $\overline{UB}$
- Low power dissipation
  - 240 mA max (active)
  - 10 mA max (standby)
- Standard 44-pin, 400-mil plastic SOJ or TSOP package

Ordering Information

Part Number	Access Time (max)	Package
μPD431016LE-15	15 ns	44-pin plastic SOJ
LE-17	17 ns	
LE-20	20 ns	
μPD431016G5-15	15 ns	44-pin plastic TSOP
G5-17	17 ns	
G5-20	20 ns	

Pin Configurations

44-Pin Plastic SOJ



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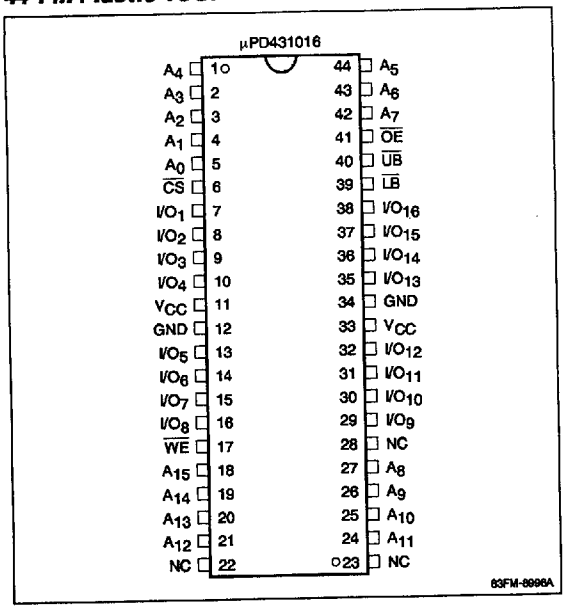
Pin Configurations (cont)

44-Pin Plastic TSOP



Pin Identification

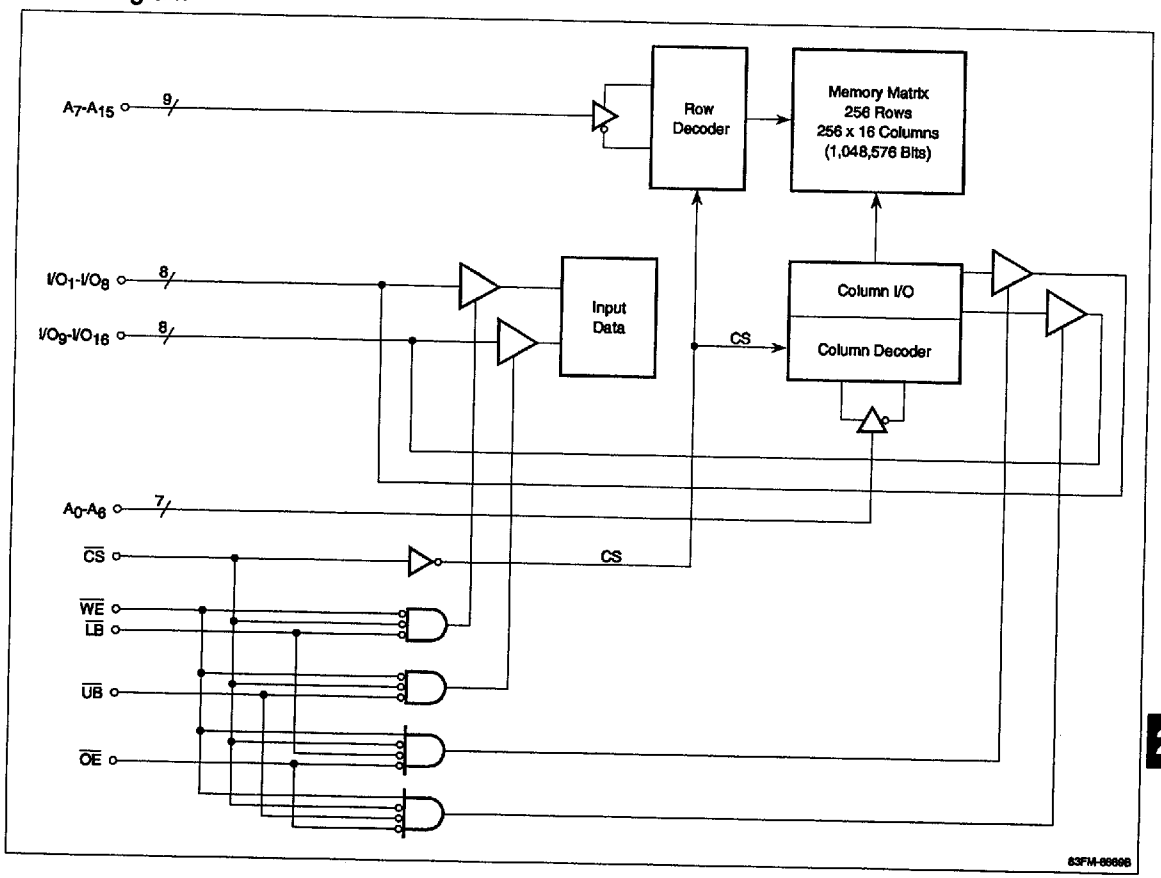
Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{LB}$	Lower byte select (I/O_1 - I/O_8)
$\overline{OE}$	Output enable
$\overline{UB}$	Upper byte select (I/O_9 - I/O_{16})
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O_1 - I/O_8	I/O_9 - I/O_{16}	Power
H	X	X	X	X	Not selected	Hi-Z	Hi-Z	Standby
L	L	H	L	L	Read	D_{OUT}	D_{OUT}	Active
			L	H	Read	D_{OUT}	Hi-Z	
			H	L	Read	Hi-Z	D_{OUT}	
L	X	L	L	L	Write	D_{IN}	D_{IN}	
			L	H	Write	D_{IN}	Hi-Z	
			H	L	Write	Hi-Z	D_{IN}	
L	H	H	X	X	—	Hi-Z	Hi-Z	
L	X	X	H	H	—	Hi-Z	Hi-Z	

X = Don't care.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) V_{IN} (min) = −3.0 V for 10-ns pulse.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Note:

(1) V_{IL} = −3.0 V for 10-ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

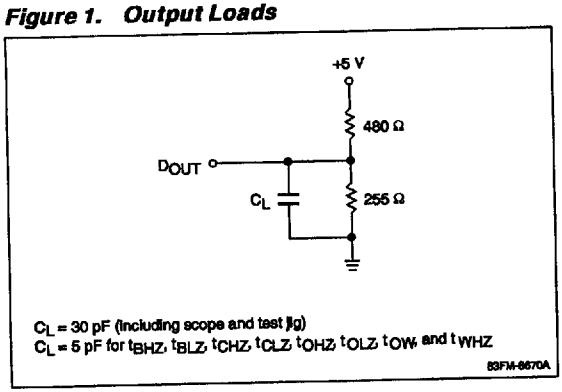
Capacitance is sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, or UB = V_{IH} or $\overline{WE}$ = V_{IL}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Figure 1. Output Loads



C_L = 30 pF (including scope and test jig)
C_L = 5 pF for t_{BHZ}, t_{BLZ}, t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD431016-15 Min	μPD431016-15 Max	μPD431016-17 Min	μPD431016-17 Max	μPD431016-20 Min	μPD431016-20 Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		240		230		220	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA (Note 5)
Address access time	t_{AA}		15		17		20	ns	
Chip select access time	t_{ACS}		15		17		20	ns	
Data byte select access time	t_{ADB}		8		9		10	ns	
Data byte select to output in high-Z	t_{BHZ}		7		7		7	ns	
Data byte select to output in low-Z	t_{BLZ}	1		1		1		ns	
Chip deselection to output in high-Z	t_{CHZ}	0	7	0	7	0	7	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Output enable access time	t_{OE}		8		9		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Output enable to output in high-Z	t_{OHZ}		7		7		7	ns	
Output enable to output in low-Z	t_{OLZ}	1		1		1		ns	
Read cycle time	t_{RC}	15		17		20		ns	(Note 2)
Write Operation									
Address setup time	t_{AS}	0		0		0		ns	
Address valid to end of write	t_{AW}	9		11		12		ns	
Data byte select to end of write	t_{BW}	9		11		12		ns	
Chip select to end of write	t_{CW}	10		11		12		ns	
Data hold time	t_{DH}	0		0		0		ns	
Data valid to end of write	t_{DW}	8		9		10		ns	
Output active from end of write	t_{OW}	3		3		3		ns	(Note 3)
Write enable to output in high-Z	t_{WHZ}	0	7	0	7	0	7	ns	(Note 4)
Write cycle time	t_{WC}	15		17		20		ns	(Note 2)
Write pulse width	t_{WP}	9		10		10		ns	
Write recovery time	t_{WR}	0		0		0		ns	

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figure 1 for output loads.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

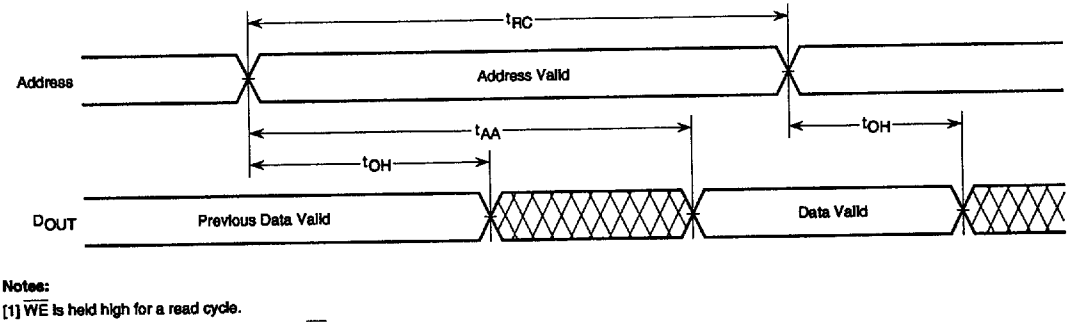
(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 1.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} – 200 mV with the load shown in figure 1.

(5) I_{CC} = 180 mA max at t_{AA} = 50 ns.

Timing Waveforms

Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

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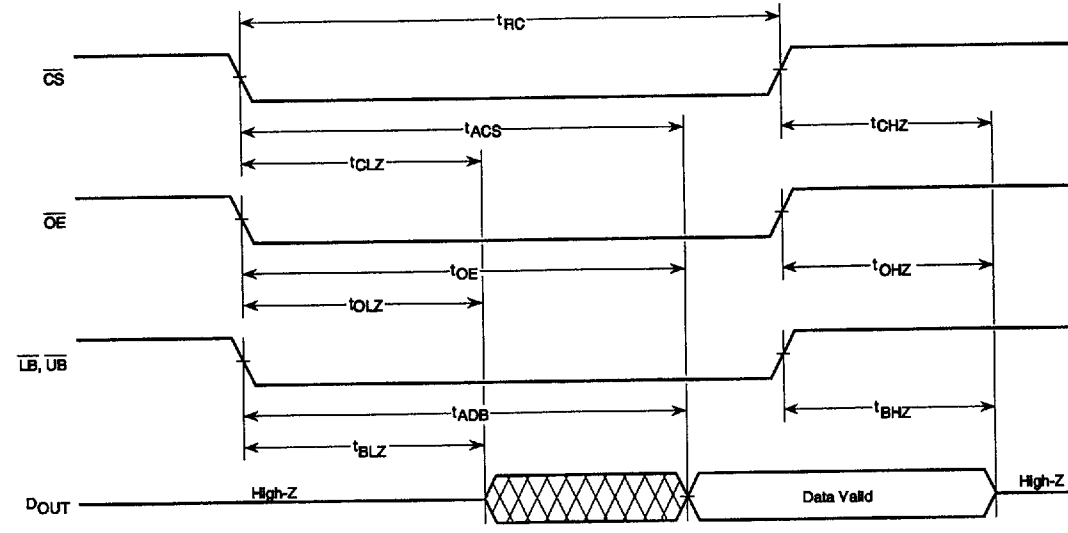
Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Device is continuously selected:
$\overline{CS} = \overline{OE} = \overline{LB} = Low$
$\overline{CS} = \overline{OE} = \overline{UB} = Low$
[3] Address valid prior to or coincident with $\overline{CS}$ transition low.

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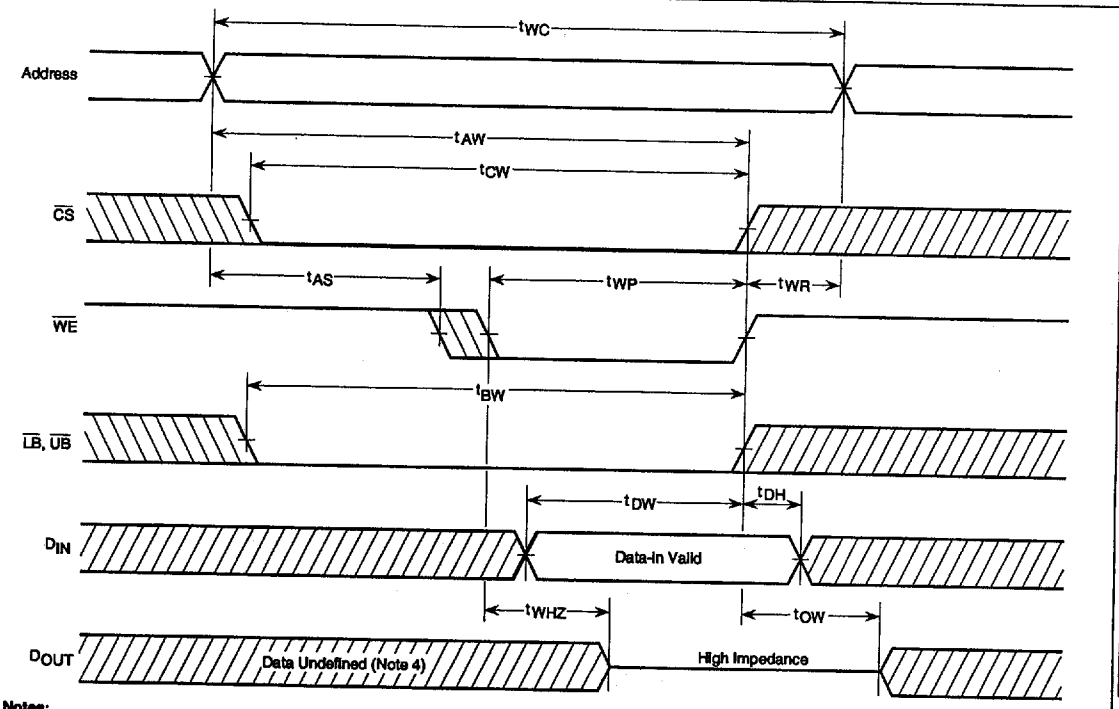
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.

[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

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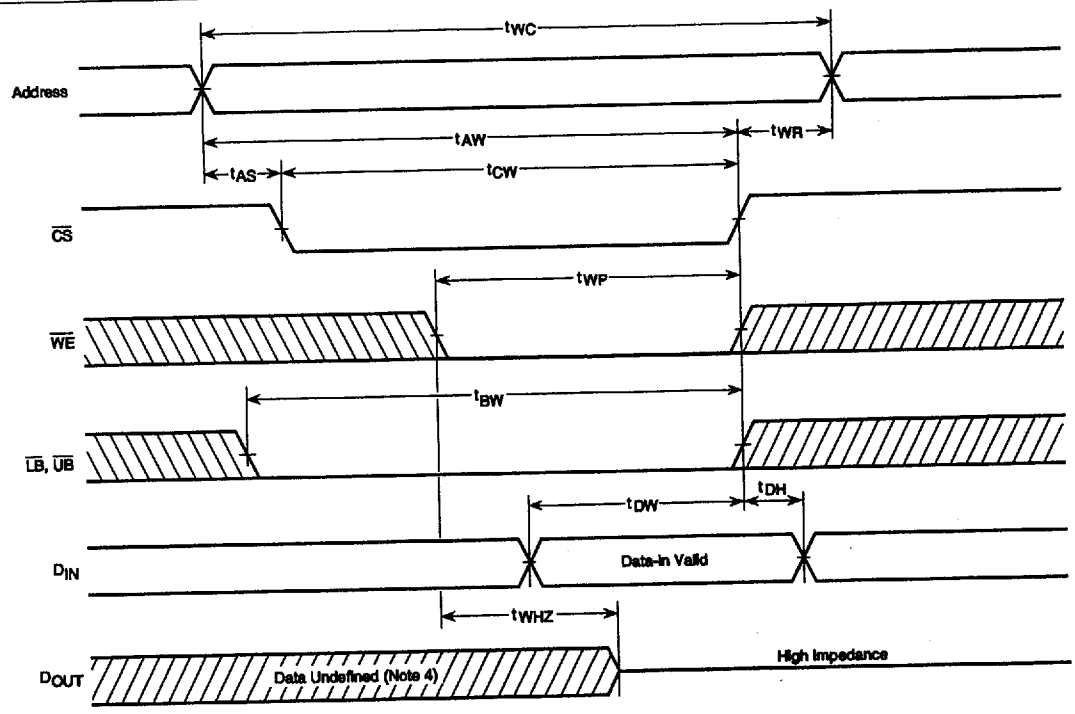
Timing Waveforms (cont)

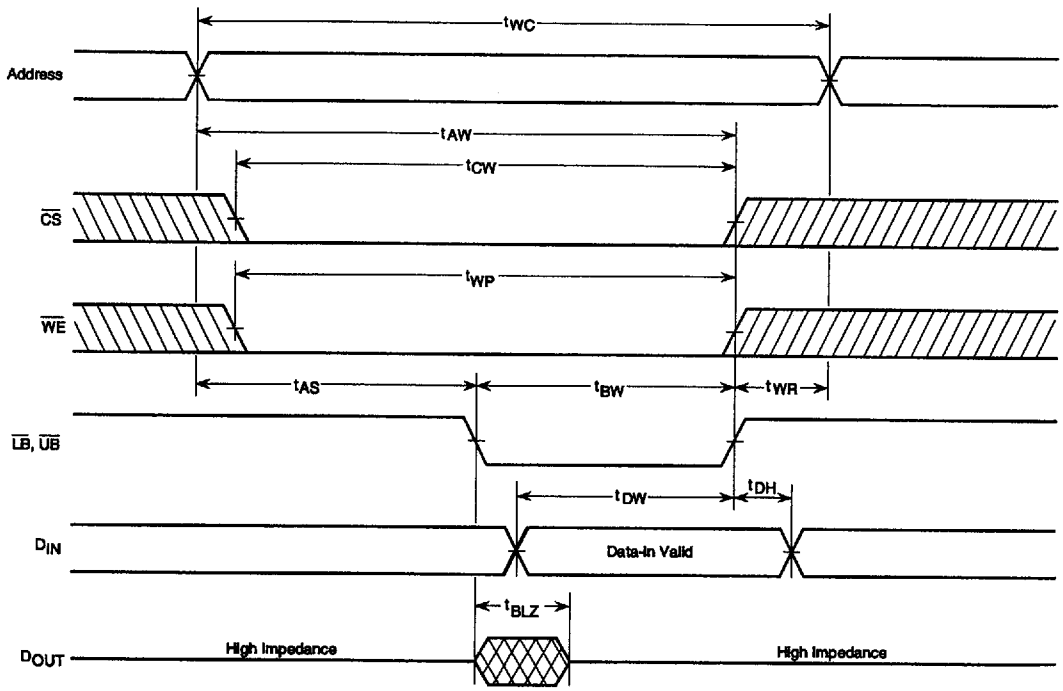
$\overline{CS}$-Controlled Write Cycle



Notes:
[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.
[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.
[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

Timing Waveforms (cont)

$\overline{LB}$/ $\overline{UB}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.

[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

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