

MOS INTEGRATED CIRCUIT

μ PD42S16170L, 42S17170L, 42S18170L

16 M BIT DYNAMIC RAM
(3.3V FAST PAGE MODE & BYTE WRITE MODE)

PRELIMINARY

DESCRIPTION

The NEC μ PD42S16170L, μ PD42S17170L and μ PD42S18170L are 1 048 576 words by 16 bits dynamic CMOS RAM with optional fast page mode. CMOS sense amplifier, peripheral circuits and 1 transistor memory cell technique realize high speed access, cycle time and low power dissipation.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh cycles or normal read or write cycles on the 4096 address combinations of A0 to A11 (for μ PD42S16170L) or 2048 address combinations of A0 to A10 (for μ PD42S17170L) or 1024 address combinations of A0 to A9 (for μ PD42S18170L) during a 256 ms period.

The μ PD42S16170L, μ PD42S17170L and μ PD42S18170L are packaged in 42-pin plastic SOJ and 50-pin plastic TSOP.

FEATURES

- 1 048 576 words by 16 bits organization
- Single +3.3V \pm 0.3V power supply
- On-chip substrate bias generator
- Non latched I/O, TTL-compatible
- Multiplexed address inputs
- Read-modify-write, Fast Page Mode and Byte Write Mode capability
- $\overline{\text{RAS}}$ only refresh, hidden refresh and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal address refresh
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

| DEVICE | Row Address | Column Address | Refresh cycle |
|-------------------|-------------|----------------|--------------------|
| μ PD42S16170L | A0 to A11 | A0 to A7 | 4096 cycles/256 ms |
| μ PD42S17170L | A0 to A10 | A0 to A8 | 2048 cycles/256 ms |
| μ PD42S18170L | A0 to A9 | A0 to A9 | 1024 cycles/256 ms |

- 4 performance ranges

| DEVICE | ACCESS TIME (MAX.) | R/W CYCLE (MIN.) | PAGE MODE CYCLE (MIN.) | Low power dissipation | |
|-----------------------|--------------------|------------------|------------------------|-----------------------|--------------------------------|
| | | | | Active (MAX.) | Standby |
| μ PD42S16170L-A60 | 60 ns | 110 ns | 40 ns | 324 mW | 0.36 mW (MAX.) (CMOS level) |
| μ PD42S17170L-A60 | | | | 396 mW | |
| μ PD42S18170L-A60 | | | | 540 mW | |
| μ PD42S16170L-A70 | 70 ns | 130 ns | 45 ns | 288 mW | |
| μ PD42S17170L-A70 | | | | 360 mW | |
| μ PD42S18170L-A70 | | | | 504 mW | |
| μ PD42S16170L-A80 | 80 ns | 150 ns | 50 ns | 252 mW | |
| μ PD42S17170L-A80 | | | | 324 mW | |
| μ PD42S18170L-A80 | | | | 468 mW | |

μPD42S16170L, 42S17170L, 42S18170L

ORDERING INFORMATION

| PART NUMBER | ACCESS TIME (MAX.) | PACKAGE | QUALITY GRADE |
|-------------------------|--------------------|------------------------------------|---------------|
| μ PD42S16170LLE-A60 | 60ns | 42-pin Plastic SOJ | STANDARD |
| μ PD42S17170LLE-A60 | | | |
| μ PD42S18170LLE-A60 | | | |
| μ PD42S16170LLE-A70 | 70ns | | |
| μ PD42S17170LLE-A70 | | | |
| μ PD42S18170LLE-A70 | | | |
| μ PD42S16170LLE-A80 | 80ns | | |
| μ PD42S17170LLE-A80 | | | |
| μ PD42S18170LLE-A80 | | | |
| μ PD42S16170LG5-A60-7JF | 60ns | 50-pin Plastic TSOP | STANDARD |
| μ PD42S17170LG5-A60-7JF | | | |
| μ PD42S18170LG5-A60-7JF | | | |
| μ PD42S16170LG5-A70-7JF | 70ns | | |
| μ PD42S17170LG5-A70-7JF | | | |
| μ PD42S18170LG5-A70-7JF | | | |
| μ PD42S16170LG5-A80-7JF | 80ns | | |
| μ PD42S17170LG5-A80-7JF | | | |
| μ PD42S18170LG5-A80-7JF | | | |
| μ PD42S16170LG5-A60-7KF | 60ns | 50-pin Plastic TSOP (Reverse bent) | STANDARD |
| μ PD42S17170LG5-A60-7KF | | | |
| μ PD42S18170LG5-A60-7KF | | | |
| μ PD42S16170LG5-A70-7KF | 70ns | | |
| μ PD42S17170LG5-A70-7KF | | | |
| μ PD42S18170LG5-A70-7KF | | | |
| μ PD42S16170LG5-A80-7KF | 80ns | | |
| μ PD42S17170LG5-A80-7KF | | | |
| μ PD42S18170LG5-A80-7KF | | | |

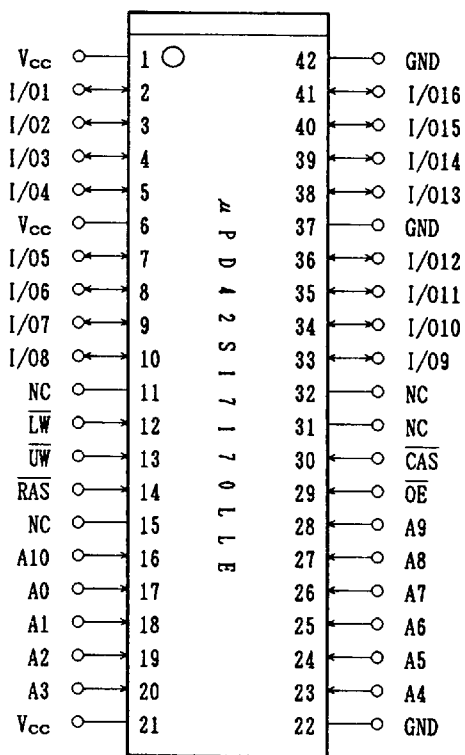
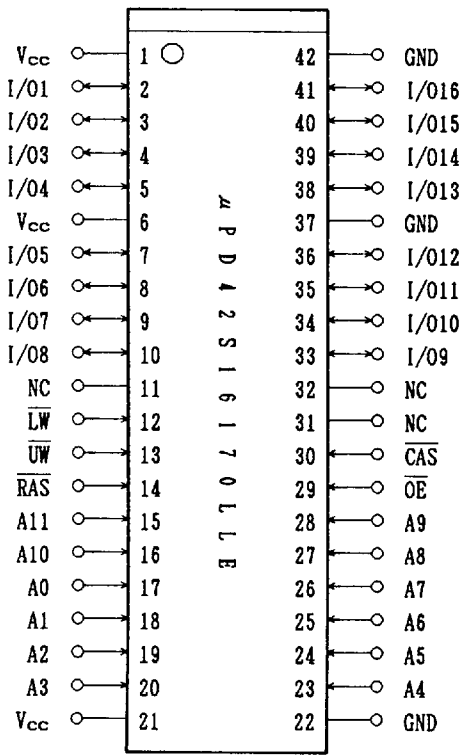
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

μPD42S16170L, 42S17170L, 42S18170L

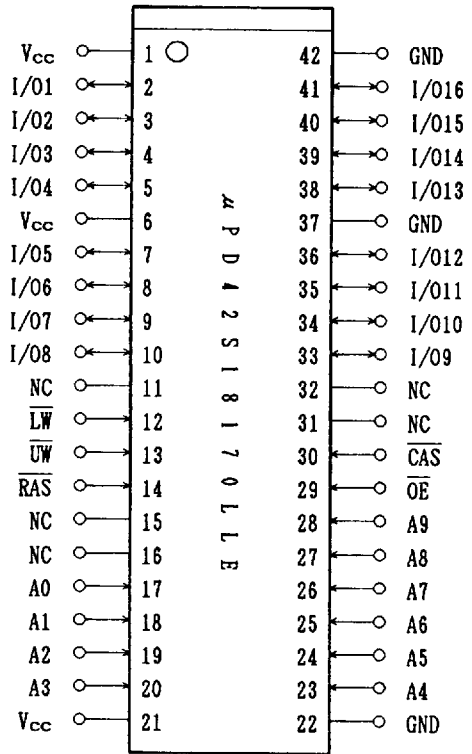
PIN CONFIGURATION (Marking Side)

- A0 to A9/A10/A11 : Address Inputs
- I/01 to I/016 : Data Inputs/Outputs
- $\overline{\text{RAS}}$: Row Address Strobe
- $\overline{\text{CAS}}$: Column Address Strobe
- $\overline{\text{UW}}$: Upper Byte Write Enable
- $\overline{\text{LW}}$: Lower Byte Write Enable
- OE : Output Enable
- V_{cc} : Supply Voltage
- GND : Ground
- NC : No Connection

42-pin Plastic SOJ (400 mil)



42-pin Plastic SOJ (400 mil)

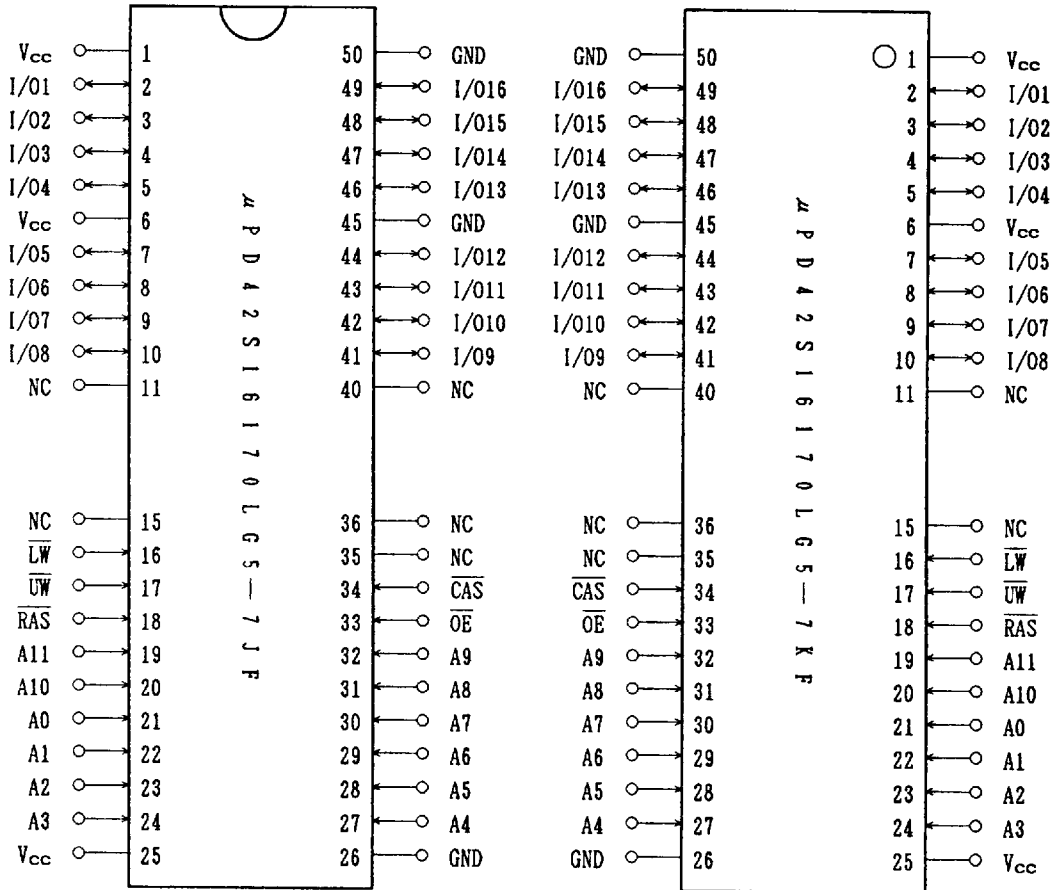


μ PD42S16170L, 42S17170L, 42S18170L

50-pin Plastic TSOP (400 mil)

【 μ PD42S16170L】

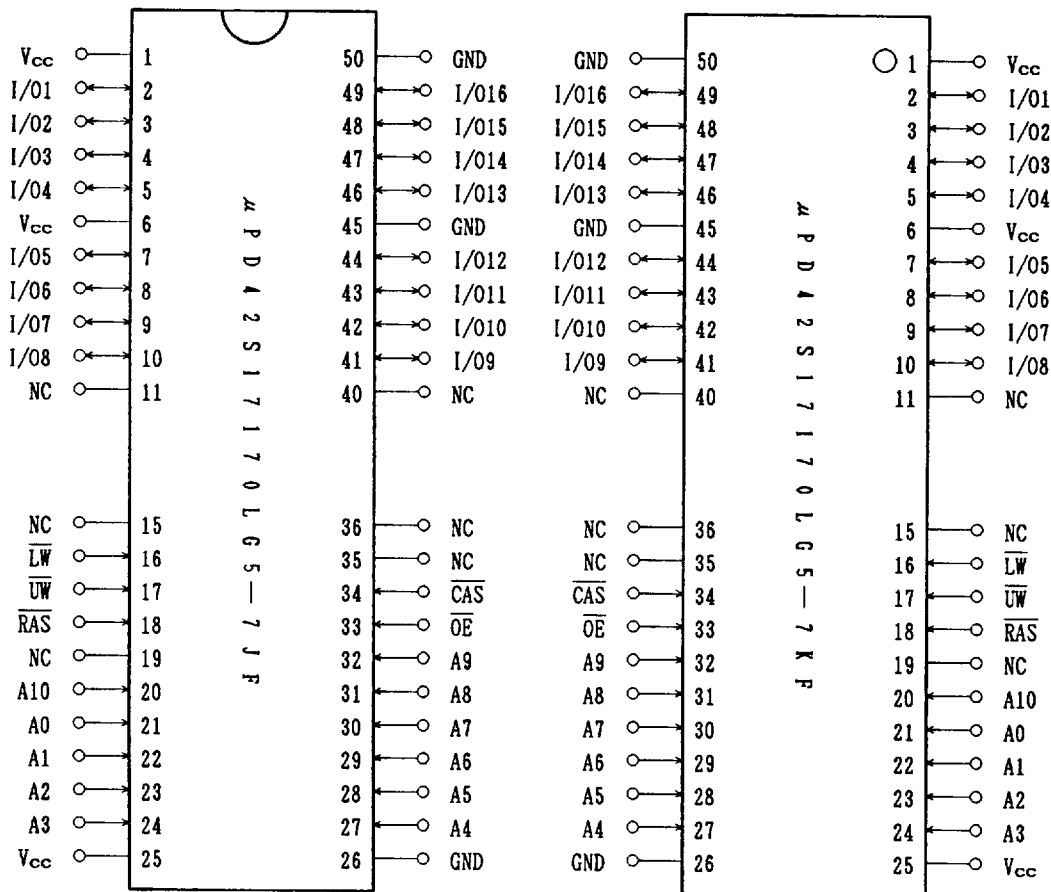
Reverse bent



μ PD42S16170L, 42S17170L, 42S18170L

【 μ PD42S17170L】

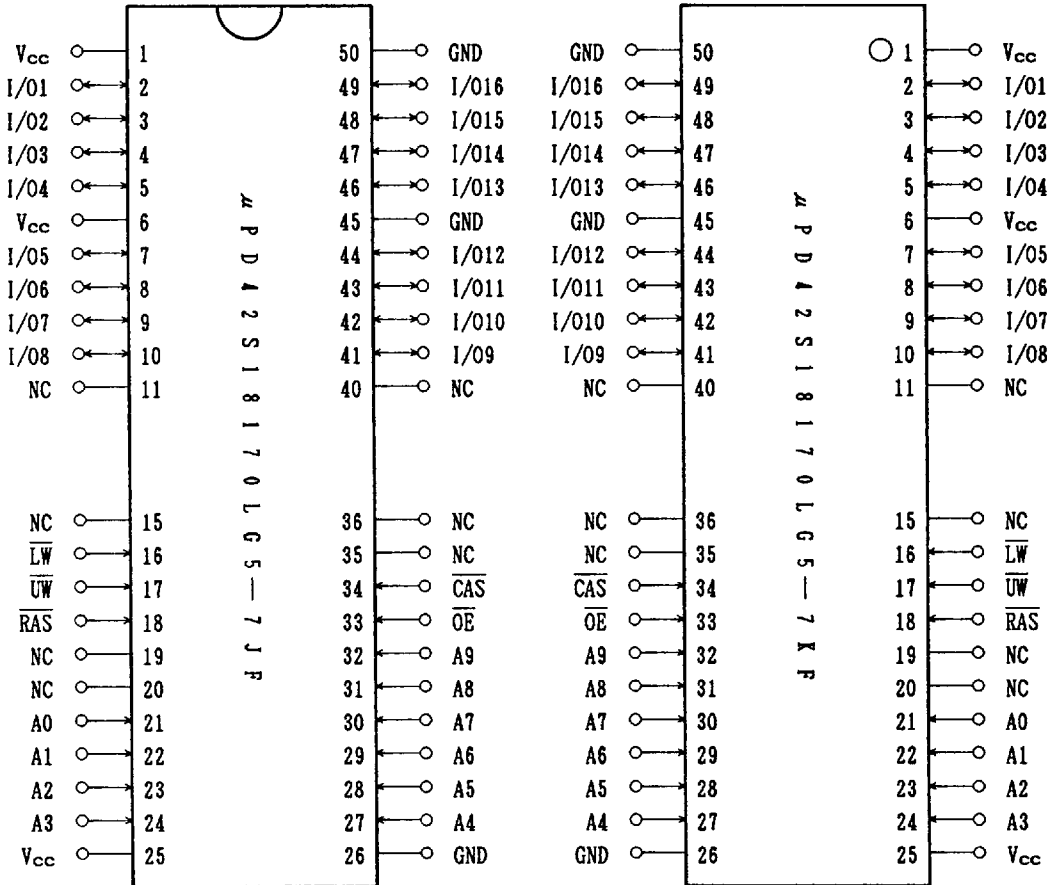
Reverse bent



μPD42S16170L, 42S17170L, 42S18170L

【μPD42S18170L】

Reverse bent



μPD42S16170L,42S17170L,42S18170L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | TEST CONDITION | RATING | UNIT |
|------------------------------------|-----------|----------------|--------------|------|
| Voltage on Any Pin Relative to GND | V_T | | -0.5 to +4.6 | V |
| Short Circuit Output Current | I_o | | 20 | mA |
| Power Dissipation | P_D | | 1 | W |
| Operating Temperature | T_{opt} | | 0 to 70 | °C |
| Storage Temperature | T_{stg} | | -55 to +125 | °C |

*COMMENT : Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS NOTES:1,2

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|--------------------------|----------|----------------|------|------|--------------|------|
| Supply Voltage | V_{cc} | | 3.0 | 3.3 | 3.6 | V |
| High Level Input Voltage | V_{IH} | | 2.0 | | $V_{cc}+0.3$ | V |
| Low Level Input Voltage | V_{IL} | | -0.3 | | 0.8 | V |
| Ambient Temperature | T_a | | 0 | | 70 | °C |

CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{ MHz}$)

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------------------|----------|---|------|------|------|------|
| Input Capacitance | C_{i1} | A0 to A9/A10/A11 | | | 5 | pF |
| | C_{i2} | RAS, CAS, \overline{UW} , \overline{LW} , \overline{OE} | | | 7 | pF |
| Data Input/Output Capacitance | C_D | I/01 to I/016 | | | 7 | pF |

DC CHARACTERISTICS (Recommended Operating Conditions unless Otherwise noted)

【 μ PD42S16170L】

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|------------|---|-----------------------|------|------|---------|-------|
| Operating Current | I_{CC1} | $\overline{RAS}, \overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}, I_O=0mA$ | μ PD42S16170L-A60 | | 90 | mA | 3 |
| | | | μ PD42S16170L-A70 | | 80 | | |
| | | | μ PD42S16170L-A80 | | 70 | | |
| Standby Current | I_{CC2} | $\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}, I_O=0mA$ | | | 0.5 | mA | |
| | | $\overline{RAS}, \overline{CAS} \geq V_{CC}-0.2V, I_O=0mA$ | | | 0.1 | | |
| Refresh Current (\overline{RAS} Only Refresh) | I_{CC3} | \overline{RAS} Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC}=t_{RC(MIN.)}, I_O=0mA$ | μ PD42S16170L-A60 | | 90 | mA | 3 |
| | | | μ PD42S16170L-A70 | | 80 | | |
| | | | μ PD42S16170L-A80 | | 70 | | |
| Operating Current (Fast Page Mode) | I_{CC4} | \overline{CAS} Cycling, $\overline{RAS} \leq V_{IL(MAX.)}$ $t_{PC}=t_{PC(MIN.)}, I_O=0mA$ | μ PD42S16170L-A60 | | 90 | mA | 3 |
| | | | μ PD42S16170L-A70 | | 80 | | |
| | | | μ PD42S16170L-A80 | | 70 | | |
| Refresh Current (\overline{CAS} before \overline{RAS} Refresh) | I_{CC5} | \overline{RAS} Cycling, $t_{RC}=t_{RC(MIN.)}, I_O=0mA$ | μ PD42S16170L-A60 | | 90 | mA | 3 |
| | | | μ PD42S16170L-A70 | | 80 | | |
| | | | μ PD42S16170L-A80 | | 70 | | |
| Battery back-up Current (Standby with \overline{CAS} before \overline{RAS} Refresh) | I_{CC6} | Standby: $V_{CC}-0.2V \leq \overline{RAS}$, \overline{CAS} before \overline{RAS} Refresh: 4096 Cycle/256 ms $\overline{RAS}, \overline{CAS}: 0V \leq V_{IL} \leq 0.2V$ $V_{CC}-0.2V \leq V_{IH} \leq V_{IH MAX.}$ $\overline{WE}, \overline{OE}: V_{IH}$ Address: Don't care Output: OPEN | $t_{RAS} \leq 300ns$ | | 140 | μA | |
| | | | $t_{RAS} \leq 1\mu s$ | | 140 | | |
| Self Refresh Current (\overline{CAS} before \overline{RAS} Self Refresh) | I_{CC7} | $\overline{RAS}, \overline{CAS}: 0V \leq V_{IL} \leq 0.2V$ $V_{CC}-0.2V \leq V_{IH} \leq V_{IH MAX.}, I_O=0mA$ | | | 80 | μA | |
| Input Leakage Current | $I_{I(L)}$ | $V_I=0$ to 3.6V, all other pins= 0V | | -5 | 5 | μA | |
| Output Leakage Current | $I_{O(L)}$ | D_{OUT} is disabled, $V_O=0$ to 3.6V | | -5 | 5 | μA | |
| Output High Voltage | V_{OH} | $I_O=-2mA$ | | 2.4 | | V | |
| Output Low Voltage | V_{OL} | $I_O=2mA$ | | | 0.4 | V | |

μ PD42S16170L, 42S17170L, 42S18170L

【 μ PD42S17170L】

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|------------|---|-----------------------|------|------|---------|-------|
| Operating Current | I_{CC1} | $\overline{RAS}, \overline{CAS}$ Cycling $t_{RC}=t_{RC(MIN.)}, I_o=0mA$ | μ PD42S17170L-A60 | | 110 | mA | 3 |
| | | | μ PD42S17170L-A70 | | 100 | | |
| | | | μ PD42S17170L-A80 | | 90 | | |
| Standby Current | I_{CC2} | $\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}, I_o=0mA$ | | | 0.5 | mA | |
| | | $\overline{RAS}, \overline{CAS} \geq V_{CC}-0.2V, I_o=0mA$ | | | 0.1 | | |
| Refresh Current (\overline{RAS} Only Refresh) | I_{CC3} | \overline{RAS} Cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC}=t_{RC(MIN.)}, I_o=0mA$ | μ PD42S17170L-A60 | | 110 | mA | 3 |
| | | | μ PD42S17170L-A70 | | 100 | | |
| | | | μ PD42S17170L-A80 | | 90 | | |
| Operating Current (Fast Page Mode) | I_{CC4} | \overline{CAS} Cycling, $\overline{RAS} \leq V_{IL(MAX.)}$ $t_{PC}=t_{PC(MIN.)}, I_o=0mA$ | μ PD42S17170L-A60 | | 90 | mA | 3 |
| | | | μ PD42S17170L-A70 | | 80 | | |
| | | | μ PD42S17170L-A80 | | 70 | | |
| Refresh Current (\overline{CAS} before \overline{RAS} Refresh) | I_{CC5} | \overline{RAS} Cycling, $t_{RC}=t_{RC(MIN.)}, I_o=0mA$ | μ PD42S17170L-A60 | | 110 | mA | 3 |
| | | | μ PD42S17170L-A70 | | 100 | | |
| | | | μ PD42S17170L-A80 | | 90 | | |
| Battery back-up Current (Standby with \overline{CAS} before \overline{RAS} Refresh) | I_{CC6} | Standby: $V_{CC}-0.2V \leq \overline{RAS}$, \overline{CAS} before \overline{RAS} Refresh: 2048 Cycle/256 ms $\overline{RAS}, \overline{CAS}: 0V \leq V_{IL} \leq 0.2V$ $V_{CC}-0.2V \leq V_{IH} \leq V_{IH MAX.}$ $\overline{WE}, \overline{OE}: V_{IH}$ Address: Don't care Output: OPEN | $t_{RAS} \leq 300ns$ | | 120 | μA | |
| | | | $t_{RAS} \leq 1\mu s$ | | 120 | | |
| Self Refresh Current (\overline{CAS} before \overline{RAS} Self Refresh) | I_{CC7} | $\overline{RAS}, \overline{CAS}: 0V \leq V_{IL} \leq 0.2V$ $V_{CC}-0.2V \leq V_{IH} \leq V_{IH MAX.}, I_o=0mA$ | | | 80 | μA | |
| Input Leakage Current | $I_{I(L)}$ | $V_i=0$ to 3.6V, all other pins= 0V | -5 | | 5 | μA | |
| Output Leakage Current | $I_{O(L)}$ | D_{OUT} is disabled, $V_o=0$ to 3.6V | -5 | | 5 | μA | |
| Output High Voltage | V_{OH} | $I_o=-2mA$ | 2.4 | | | V | |
| Output Low Voltage | V_{OL} | $I_o=2mA$ | | | 0.4 | V | |

μPD42S16170L, 42S17170L, 42S18170L

【μPD42S18170L】

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT | NOTES |
|---|-------------------|---|------------------------------------|------|------|------|-------|
| Operating Current | I _{CC1} | $\overline{\text{RAS}}, \overline{\text{CAS}}$ Cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}, I_{\text{O}} = 0\text{mA}$ | μPD42S18170L-A60 | | 150 | mA | 3 |
| | | | μPD42S18170L-A70 | | 140 | | |
| | | | μPD42S18170L-A80 | | 130 | | |
| Standby Current | I _{CC2} | $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}, I_{\text{O}} = 0\text{mA}$ | | | 0.5 | mA | |
| | | $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2\text{V}, I_{\text{O}} = 0\text{mA}$ | | | 0.1 | | |
| Refresh Current (RAS Only Refresh) | I _{CC3} | $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN.})}$ $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}, I_{\text{O}} = 0\text{mA}$ | μPD42S18170L-A60 | | 150 | mA | 3 |
| | | | μPD42S18170L-A70 | | 140 | | |
| | | | μPD42S18170L-A80 | | 130 | | |
| Operating Current (Fast Page Mode) | I _{CC4} | $\overline{\text{CAS}}$ Cycling, $\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX.})}$ $t_{\text{PC}} = t_{\text{PC}(\text{MIN.})}, I_{\text{O}} = 0\text{mA}$ | μPD42S18170L-A60 | | 90 | mA | 3 |
| | | | μPD42S18170L-A70 | | 80 | | |
| | | | μPD42S18170L-A80 | | 70 | | |
| Refresh Current (CAS before RAS Refresh) | I _{CC5} | $\overline{\text{RAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC}(\text{MIN.})}, I_{\text{O}} = 0\text{mA}$ | μPD42S18170L-A60 | | 150 | mA | 3 |
| | | | μPD42S18170L-A70 | | 140 | | |
| | | | μPD42S18170L-A80 | | 130 | | |
| Battery back-up Current (Standby with $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh) | I _{CC6} | Standby: $V_{\text{CC}} - 0.2\text{V} \leq \overline{\text{RAS}},$ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh: 1024 Cycle/256 ms $\overline{\text{RAS}}, \overline{\text{CAS}}: 0\text{V} \leq V_{\text{IL}} \leq 0.2\text{V}$ $V_{\text{CC}} - 0.2\text{V} \leq V_{\text{IH}} \leq V_{\text{IH MAX.}}$ $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ Address: Don't care Output: OPEN | $t_{\text{RAS}} \leq 300\text{ns}$ | | 110 | μA | |
| | | | $t_{\text{RAS}} \leq 1\mu\text{s}$ | | 110 | | |
| Self Refresh Current (CAS before RAS Self Refresh) | I _{CC7} | $\overline{\text{RAS}}, \overline{\text{CAS}}: 0\text{V} \leq V_{\text{IL}} \leq 0.2\text{V}$ $V_{\text{CC}} - 0.2\text{V} \leq V_{\text{IH}} \leq V_{\text{IH MAX.}}, I_{\text{O}} = 0\text{mA}$ | | | 80 | μA | |
| Input Leakage Current | I _{I(L)} | V _I =0 to 3.6V, all other pins= 0V | -5 | | 5 | μA | |
| Output Leakage Current | I _{O(L)} | D _{OUT} is disabled, V _O =0 to 3.6V | -5 | | 5 | μA | |
| Output High Voltage | V _{OH} | I _O =-2mA | 2.4 | | | V | |
| Output Low Voltage | V _{OL} | I _O =2mA | | | 0.4 | V | |

μPD42S16170L,42S17170L,42S18170L

AC CHARACTERISTICS

(Recommended Operating Conditions unless Otherwise noted) NOTES:2,4,5

(1/2)

| PARAMETER | SYMBOL | μ PD42S16170L-A60 | μ PD42S16170L-A70 | μ PD42S16170L-A80 | μ PD42S17170L-A60 | μ PD42S17170L-A70 | μ PD42S17170L-A80 | UNIT | NOTES |
|--|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Random Read or Write Cycle Time | t _{RC} | 110 | | 130 | | 150 | | ns | 6 |
| Read Write Cycle Time | t _{RWC} | 160 | | 180 | | 200 | | ns | 6 |
| Fast Page Mode Cycle Time(Read or Write) | t _{PC} | 40 | | 45 | | 50 | | ns | 6 |
| Read Modify Write Cycle Time(Fast Page Mode) | t _{PRWC} | 85 | | 90 | | 105 | | ns | 6 |
| Access Time from $\overline{\text{RAS}}$ | t _{RAC} | | 60 | | 70 | | 80 | ns | 7, 8 |
| Access Time from $\overline{\text{CAS}}$ (Falling Edge) | t _{CAC} | | 15 | | 20 | | 20 | ns | 7, 8 |
| Access Time from Column Address | t _{AA} | | 30 | | 35 | | 40 | ns | 7, 8 |
| Access Time from $\overline{\text{CAS}}$ Precharge | t _{ACP} | | 35 | | 40 | | 45 | ns | 7 |
| Access Time from $\overline{\text{OE}}$ | t _{OEA} | | 15 | | 20 | | 20 | ns | |
| $\overline{\text{RAS}}$ to Column Address Delay Time | t _{RAD} | 15 | 30 | 15 | 35 | 17 | 40 | ns | 8 |
| $\overline{\text{CAS}}$ -Data Set-up Time | t _{CLZ} | 0 | | 0 | | 0 | | ns | 7 |
| $\overline{\text{OE}}$ -Data Set-up Time | t _{OLZ} | 0 | | 0 | | 0 | | ns | 7 |
| Output Buffer Turn-off Delay ($\overline{\text{CAS}}$) | t _{OPF} | 0 | 13 | 0 | 15 | 0 | 15 | ns | 9 |
| $\overline{\text{OE}}$ Data Delay Time | t _{OED} | 13 | | 15 | | 15 | | ns | |
| Output Buffer Turn-off Delay ($\overline{\text{OE}}$) | t _{OEZ} | 0 | 13 | 0 | 15 | 0 | 15 | ns | 9 |
| $\overline{\text{OE}}$ Command Hold Time | t _{OEH} | 0 | | 0 | | 0 | | ns | |
| $\overline{\text{OE}}$ to $\overline{\text{RAS}}$ inactive Set-up Time | t _{OES} | 0 | | 0 | | 0 | | ns | |
| Transition Time (Rise and Fall) | t _T | 3 | 50 | 3 | 50 | 3 | 50 | ns | |
| $\overline{\text{RAS}}$ Precharge Time | t _{RP} | 40 | | 50 | | 60 | | ns | |
| $\overline{\text{RAS}}$ Pulse Width (Random Read,Write Cycle) | t _{RAS} | 60 | 10000 | 70 | 10000 | 80 | 10000 | ns | |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode) | t _{RASP} | 60 | 125000 | 70 | 125000 | 80 | 125000 | ns | |
| $\overline{\text{RAS}}$ Hold Time | t _{RSH} | 15 | | 18 | | 20 | | ns | |
| $\overline{\text{CAS}}$ Pulse Width | t _{CAS} | 15 | 10000 | 20 | 10000 | 20 | 10000 | ns | |
| $\overline{\text{CAS}}$ Hold Time | t _{CSH} | 60 | | 70 | | 80 | | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | t _{RCD} | 20 | 45 | 20 | 50 | 25 | 60 | ns | 8 |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | t _{CRP} | 5 | | 5 | | 5 | | ns | 10 |
| $\overline{\text{CAS}}$ Precharge Time | t _{CPN} | 10 | | 10 | | 10 | | ns | |
| $\overline{\text{CAS}}$ Precharge Time (Fast Page Mode) | t _{CP} | 10 | | 10 | | 10 | | ns | |
| $\overline{\text{RAS}}$ Precharge $\overline{\text{CAS}}$ Hold Time | t _{RPC} | 5 | | 5 | | 5 | | ns | |
| $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | t _{RHCP} | 35 | | 40 | | 45 | | ns | |
| Row Address Set-up Time | t _{ASR} | 0 | | 0 | | 0 | | ns | |
| Row Address Hold Time | t _{RAH} | 10 | | 10 | | 12 | | ns | |

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(2/2)

| PARAMETER | SYMBOL | μ PD42S16170L-A60 | μ PD42S16170L-A70 | μ PD42S16170L-A80 | UNIT | NOTES |
|---|-------------------|-------------------|-------------------|-------------------|------|-------|
| | | μ PD42S17170L-A60 | μ PD42S17170L-A70 | μ PD42S17170L-A80 | | |
| | | MIN. | MIN. | MAX. | MAX. | |
| Column Address Set-up Time | t _{ASC} | 0 | | 0 | | ns |
| Column Address Hold Time | t _{CAH} | 15 | | 15 | | ns |
| Column Address Lead Time Referenced to $\overline{\text{RAS}}$ | t _{RAL} | 30 | | 35 | | ns |
| Read Command Set-up Time | t _{RCS} | 0 | | 0 | | ns |
| Read Command Hold Time Referenced to $\overline{\text{RAS}}$ | t _{RRH} | 0 | | 0 | | ns 11 |
| Read Command Hold Time Referenced to $\overline{\text{CAS}}$ | t _{RCH} | 0 | | 0 | | ns 11 |
| Write Command Hold Time Referenced to $\overline{\text{CAS}}$ | t _{WCH} | 10 | | 10 | | ns 12 |
| Write Command Pulse Width | t _{WP} | 10 | | 10 | | ns 12 |
| Data-in Set-up Time | t _{DS} | 0 | | 0 | | ns 13 |
| Data-in Hold Time | t _{DH} | 10 | | 15 | | ns 13 |
| $\overline{\text{WE}}$ Command Set-up Time | t _{WCS} | 0 | | 0 | | ns 14 |
| $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time(Fast Page) | t _{CPWD} | 60 | | 65 | | ns 15 |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay | t _{CWD} | 38 | | 40 | | ns 15 |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay | t _{RWD} | 83 | | 95 | | ns 15 |
| Column Address to $\overline{\text{WE}}$ Delay Time | t _{AWD} | 53 | | 60 | | ns 15 |
| Write Command to $\overline{\text{RAS}}$ Lead Time | t _{RWL} | 20 | | 20 | | ns |
| Write Command to $\overline{\text{CAS}}$ Lead Time | t _{CWL} | 15 | | 15 | | ns |
| $\overline{\text{CAS}}$ Set-up Time for CBR Refresh | t _{CSR} | 5 | | 5 | | ns |
| $\overline{\text{CAS}}$ Hold Time for CBR Refresh | t _{CHR} | 10 | | 10 | | ns |
| Masked Write Set-up Time | t _{MCS} | 0 | | 0 | | ns |
| Masked Write Hold Time Referenced to $\overline{\text{RAS}}$ | t _{MRH} | 0 | | 0 | | ns |
| Masked Write Hold Time Referenced to $\overline{\text{CAS}}$ | t _{MCH} | 0 | | 0 | | ns |
| $\overline{\text{RAS}}$ Pulse Width (Self Refresh Cycle) | t _{RASS} | 100 | | 100 | | μs |
| $\overline{\text{RAS}}$ Precharge Time (Self Refresh Cycle) | t _{RPS} | 110 | | 130 | | ns |
| $\overline{\text{CAS}}$ Hold Time (Self Refresh Cycle) | t _{CHS} | -50 | | -50 | | ns |
| Refresh Period | t _{REF} | | 256 | | 256 | ms 16 |

NOTES:

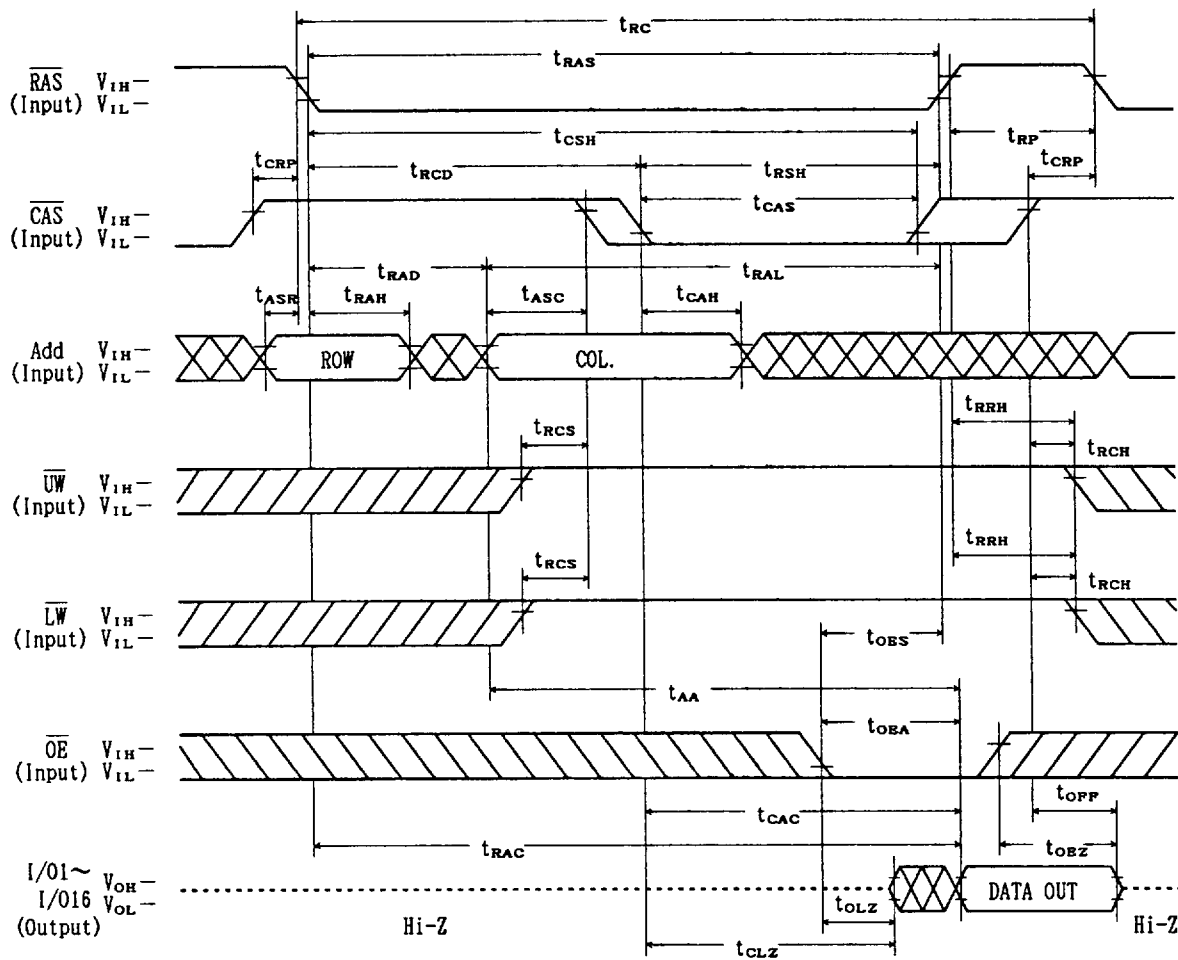
- All voltages referenced to GND.
- An initial pause of 100 μ s required after power-on followed by 8 refresh ($\overline{\text{RAS}}$ only refresh or CAS before RAS refresh) cycles before proper device operation is achieved.
- I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC3} is measured on condition that column addresses in RAS only cycle are held high or low level and I_{CC4} is measured on condition that column addresses in fast page mode are changed only one time during $t_{PC(MIN.)}$.
- AC measurements assume $t_T=5\text{ns}$
- $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_a=0$ to 70°C) is assured.
- Load = 1 TTL loads and 100pF ($V_{OH}=2.0\text{V}$, $V_{OL}=0.8\text{V}$)
- The access time is determined by RAS access time t_{RAC} , address access time t_{AA} , and $\overline{\text{CAS}}$ address time t_{CAC} . The relationship between these access time and t_{RCD} , t_{RAD} is as follows.

| CONDITION | ACCESS TIME |
|---|-----------------|
| $t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$ | $t_{RAC(MAX.)}$ |
| $t_{RAD} \geq t_{RAD(MAX.)}$ | $t_{AA(MAX.)}$ |
| $t_{RCD} \geq t_{RCD(MAX.)}$ | $t_{CAC(MAX.)}$ |

- $t_{OFF(MAX.)}$ and $t_{OBZ(MAX.)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
- t_{CRP} requirement should be applicable for RAS/CAS cycles preceded by any cycles.
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- t_{WP} is applicable for late write cycle. If the cycle is early write, it should be satisfied value of t_{WR} .
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{UW/LW}}$ leading edge in late write or read-modify-write cycles.
- If $t_{WCS} \geq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle.
- If $t_{CPWD} \geq t_{CPWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate.
- How to enter into $\overline{\text{CAS}}$ before RAS self refresh mode.
 - In case of using distributed $\overline{\text{CAS}}$ before RAS refresh
Refresh 4096 or 2048 or 1024 times during a 256ms (Before set into the $\overline{\text{CAS}}$ before RAS self refresh mode, and after reset).
 - In case of using burst CAS before RAS refresh
Refresh 4096 times during a 64ms (μ PD42S16170L) or 2048 times during a 32ms (μ PD42S17170L) or 1024 times during a 16ms (μ PD42S18170L) (Before set into the $\overline{\text{CAS}}$ before RAS self refresh mode, and after reset).
 - In case of use $\overline{\text{RAS}}$ only refresh
Refresh against all refresh address during 64ms (μ PD42S16170L) or 32ms (μ PD42S17170L) or 16ms (μ PD42S18170L) (Before set into the $\overline{\text{CAS}}$ before RAS self refresh mode, and after reset).

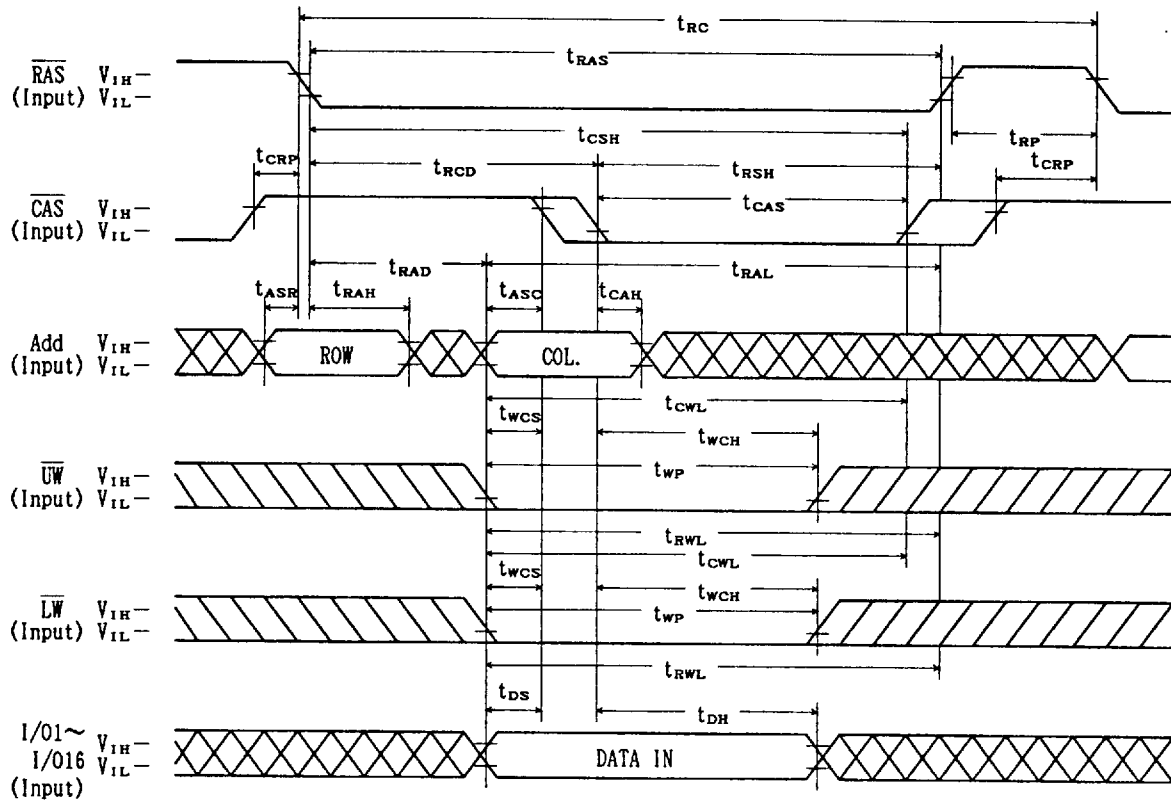
TIMING DIAGRAMS

READ CYCLE



μ PD42S16170L, 42S17170L, 42S18170L

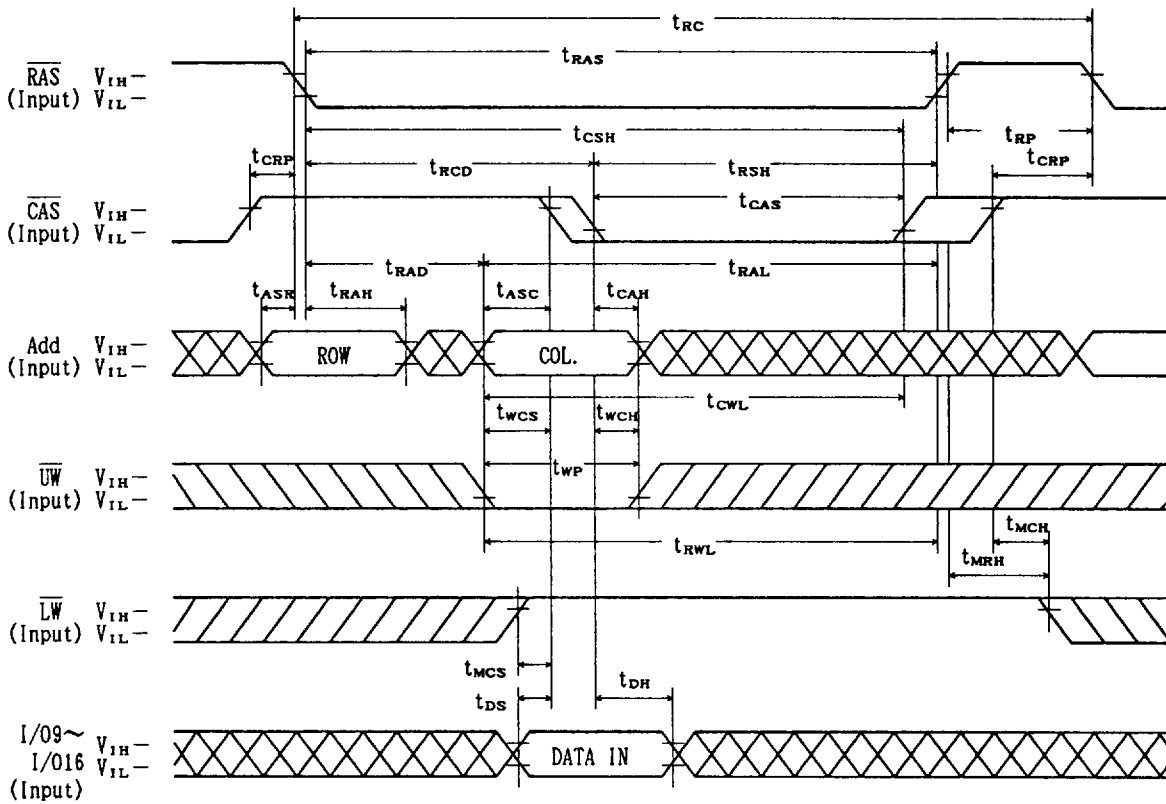
EARLY WRITE CYCLE



Note: $\overline{\text{OE}}$ = Don't care

μ PD42S16170L, 42S17170L, 42S18170L

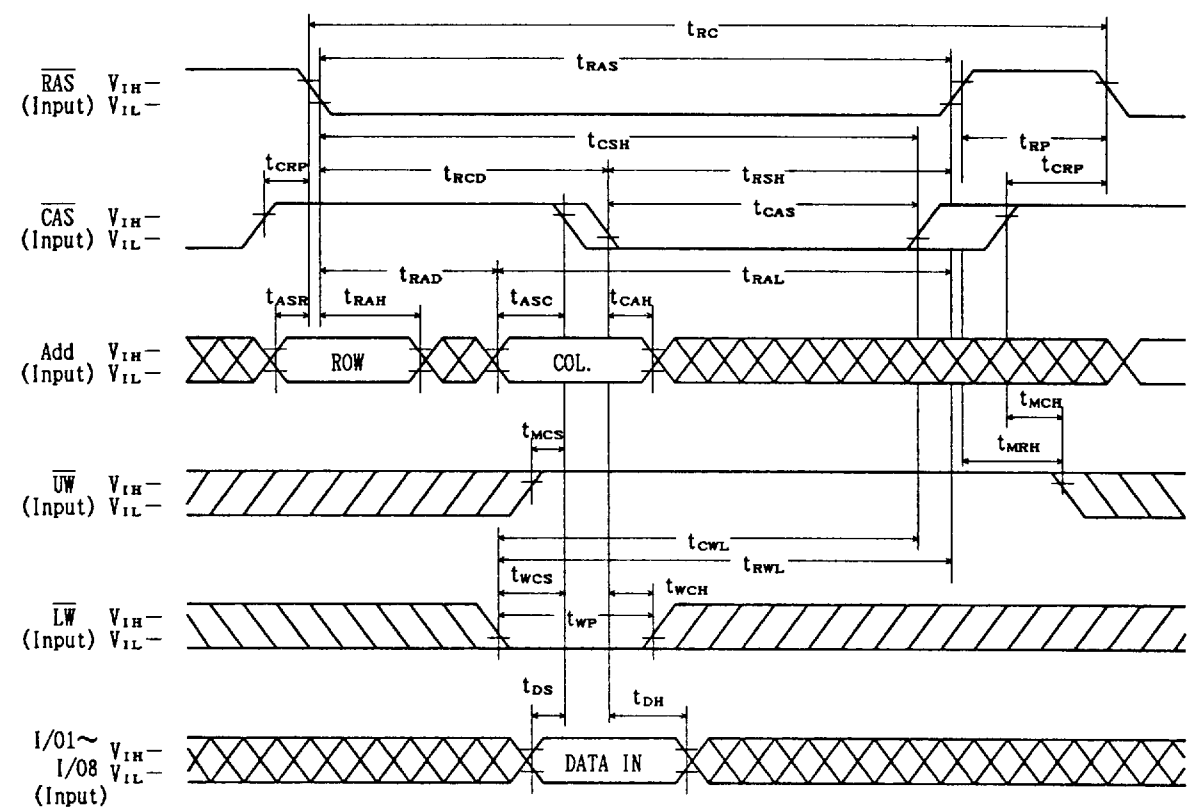
UPPER BYTE EARLY WRITE CYCLE



Note: \overline{OE} , I/O1~I/O8 = Don't care

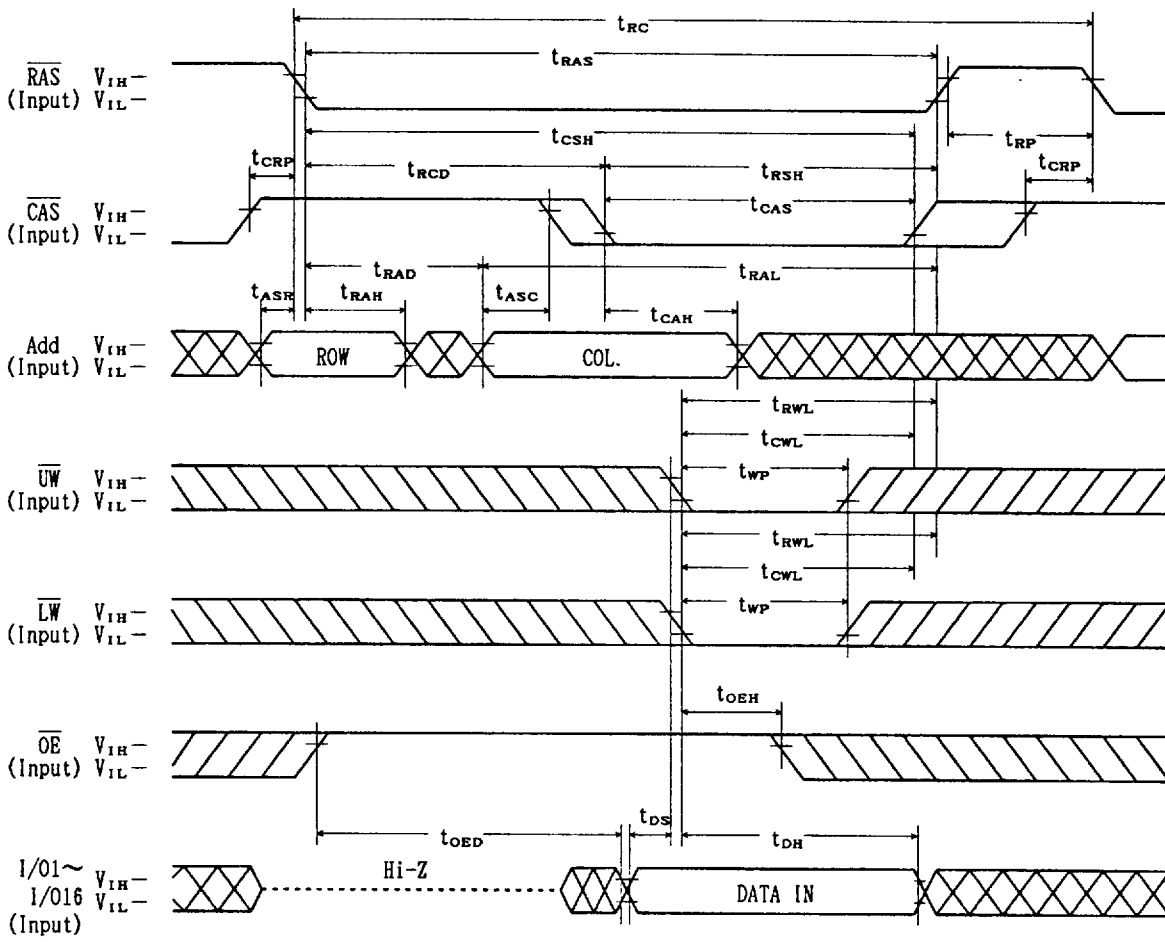
μ PD42S16170L, 42S17170L, 42S18170L

LOWER BYTE EARLY WRITE CYCLE

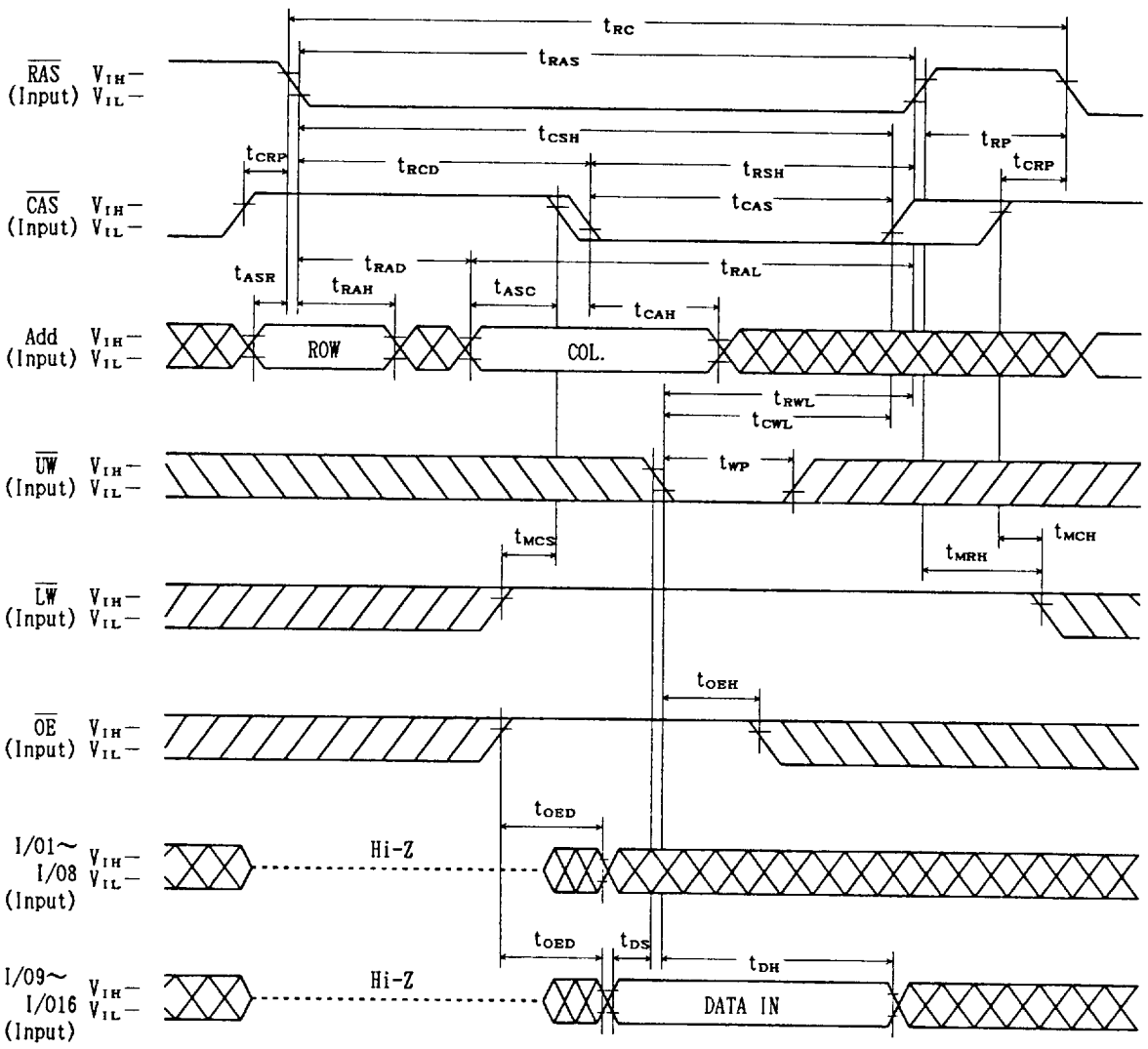


Note: \overline{OE} , I/09~I/016=Don't care

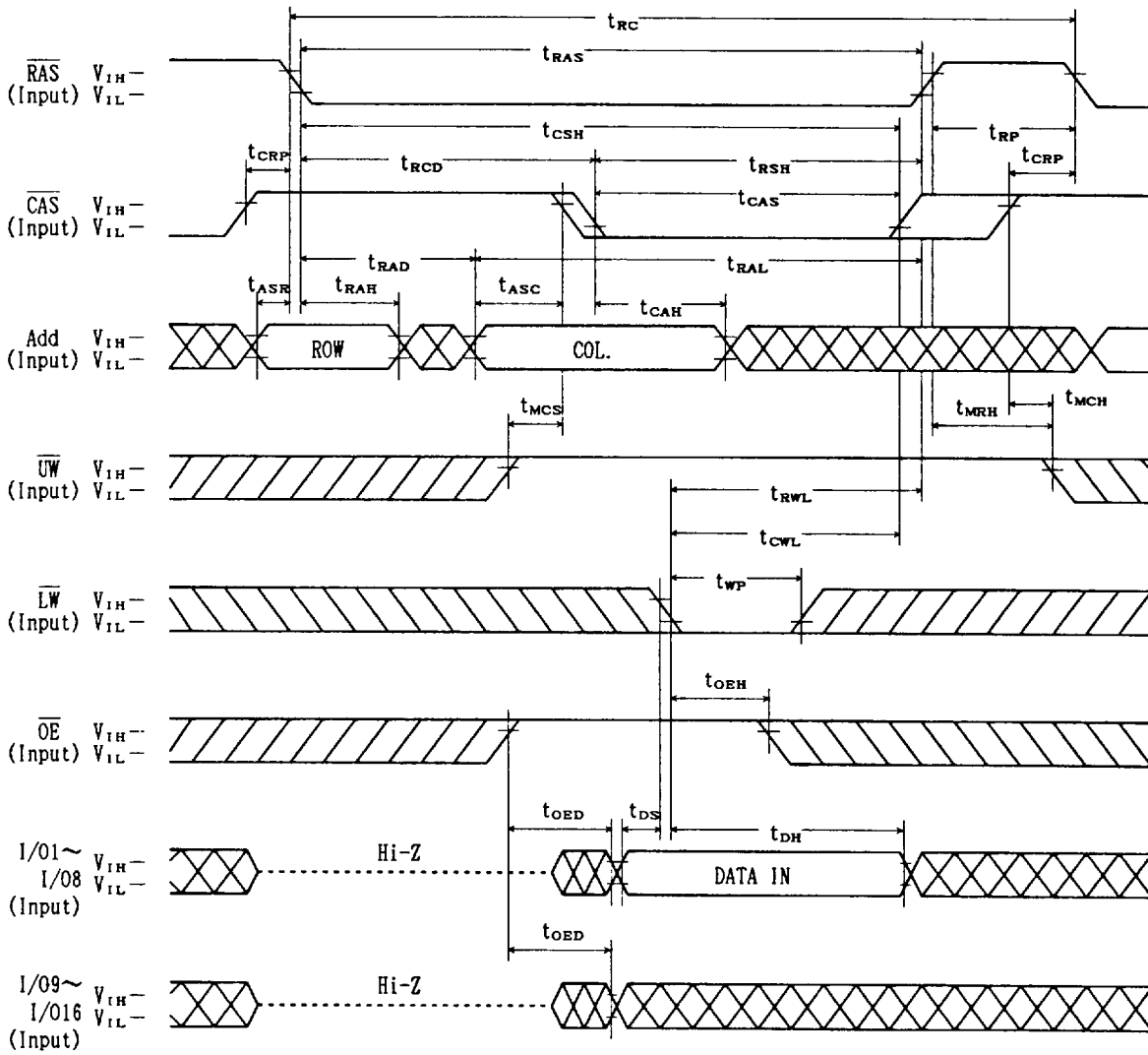
LATE WRITE CYCLE



UPPER BYTE LATE WRITE CYCLE

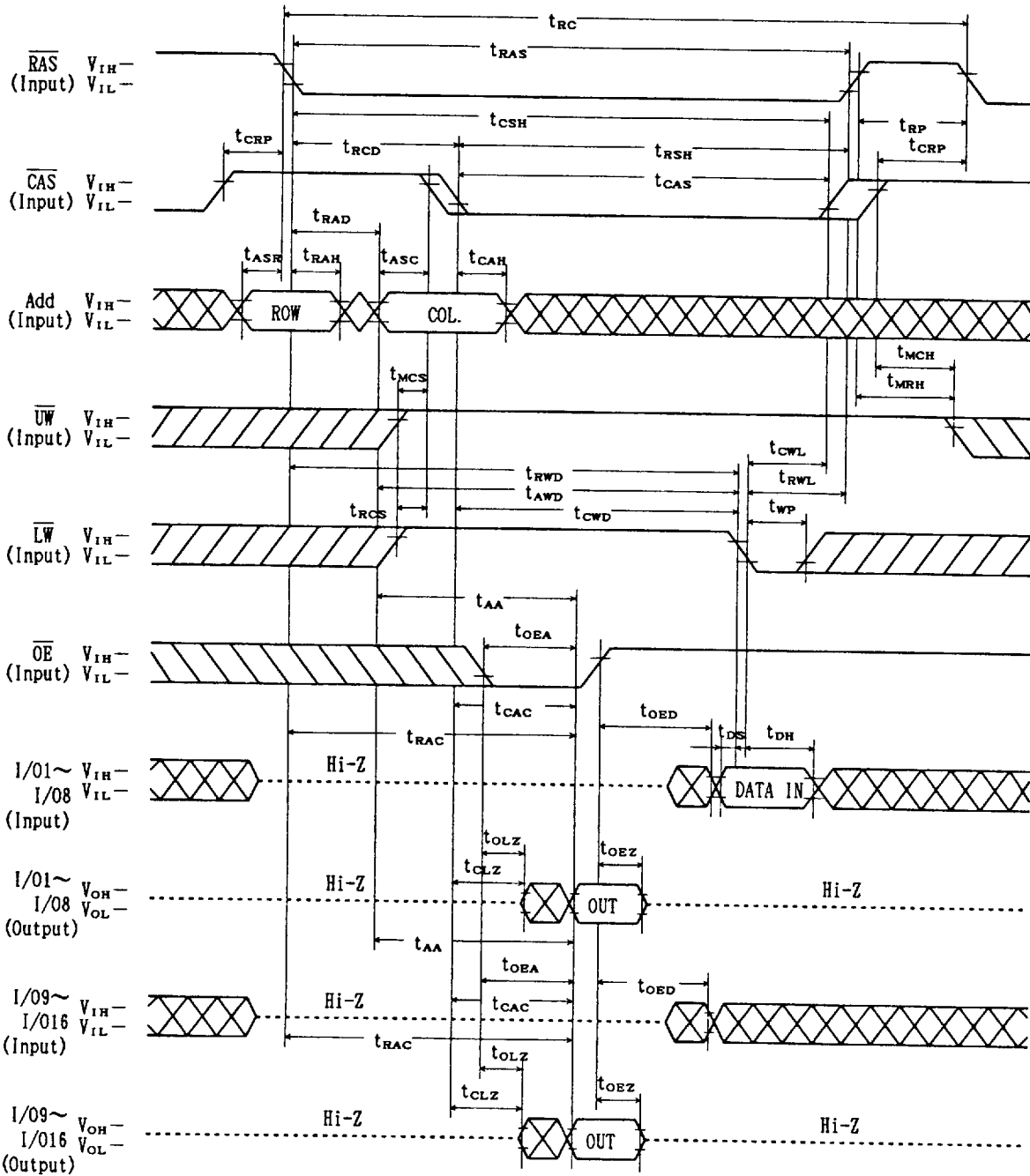


LOWER BYTE LATE WRITE CYCLE

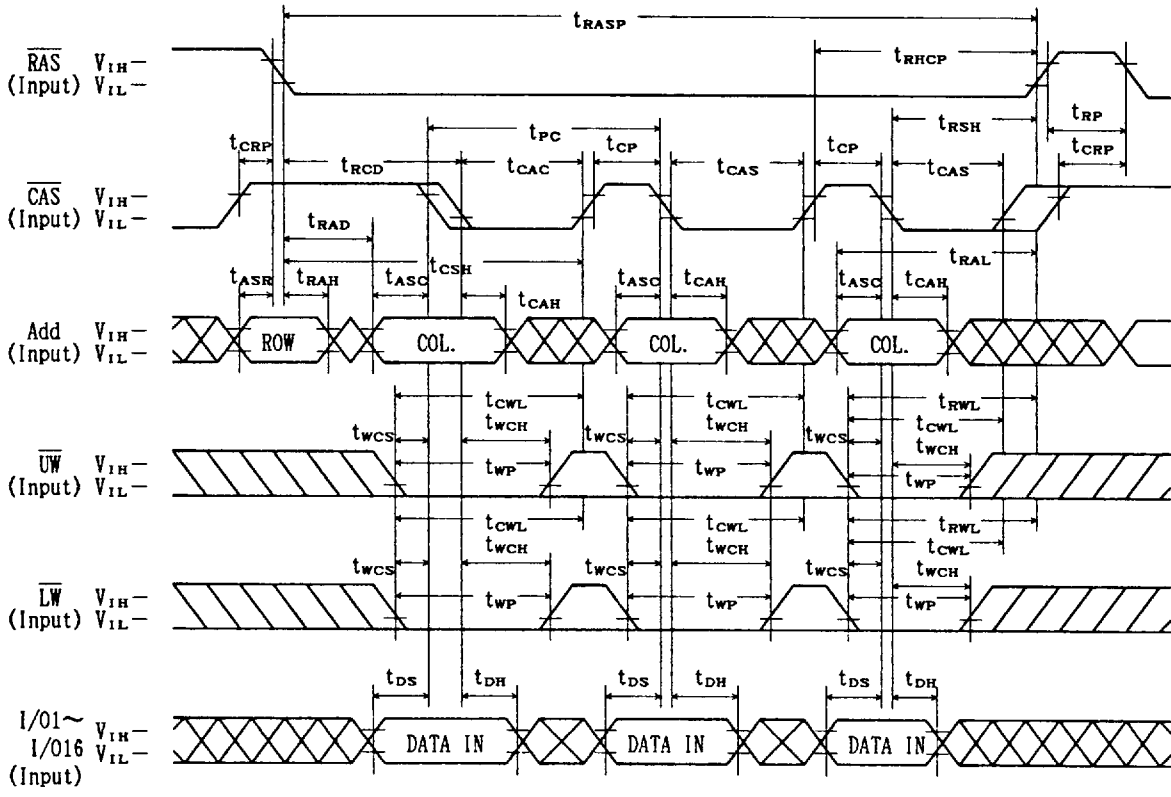


μ PD42S16170L, 42S17170L, 42S18170L

LOWER BYTE READ MODIFY WRITE CYCLE



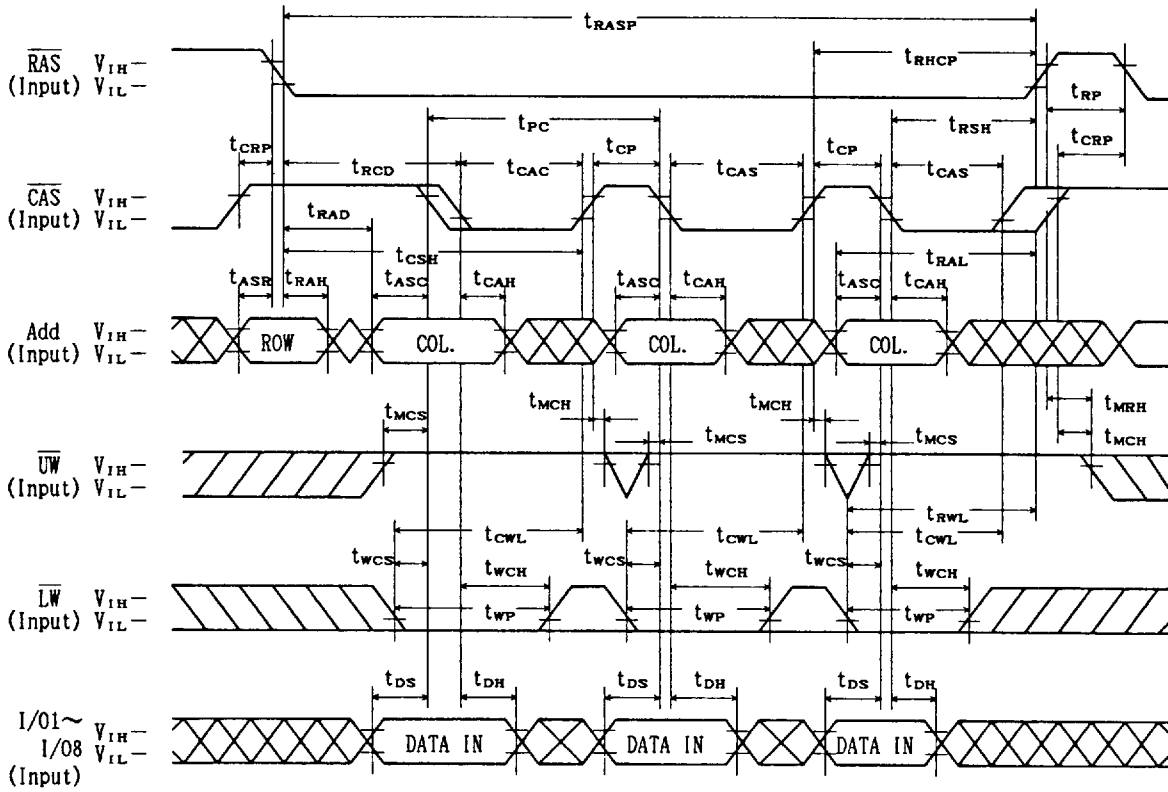
FAST PAGE MODE EARLY WRITE CYCLE



Note: \overline{OE} = Don't care

μ PD42S16170L, 42S17170L, 42S18170L

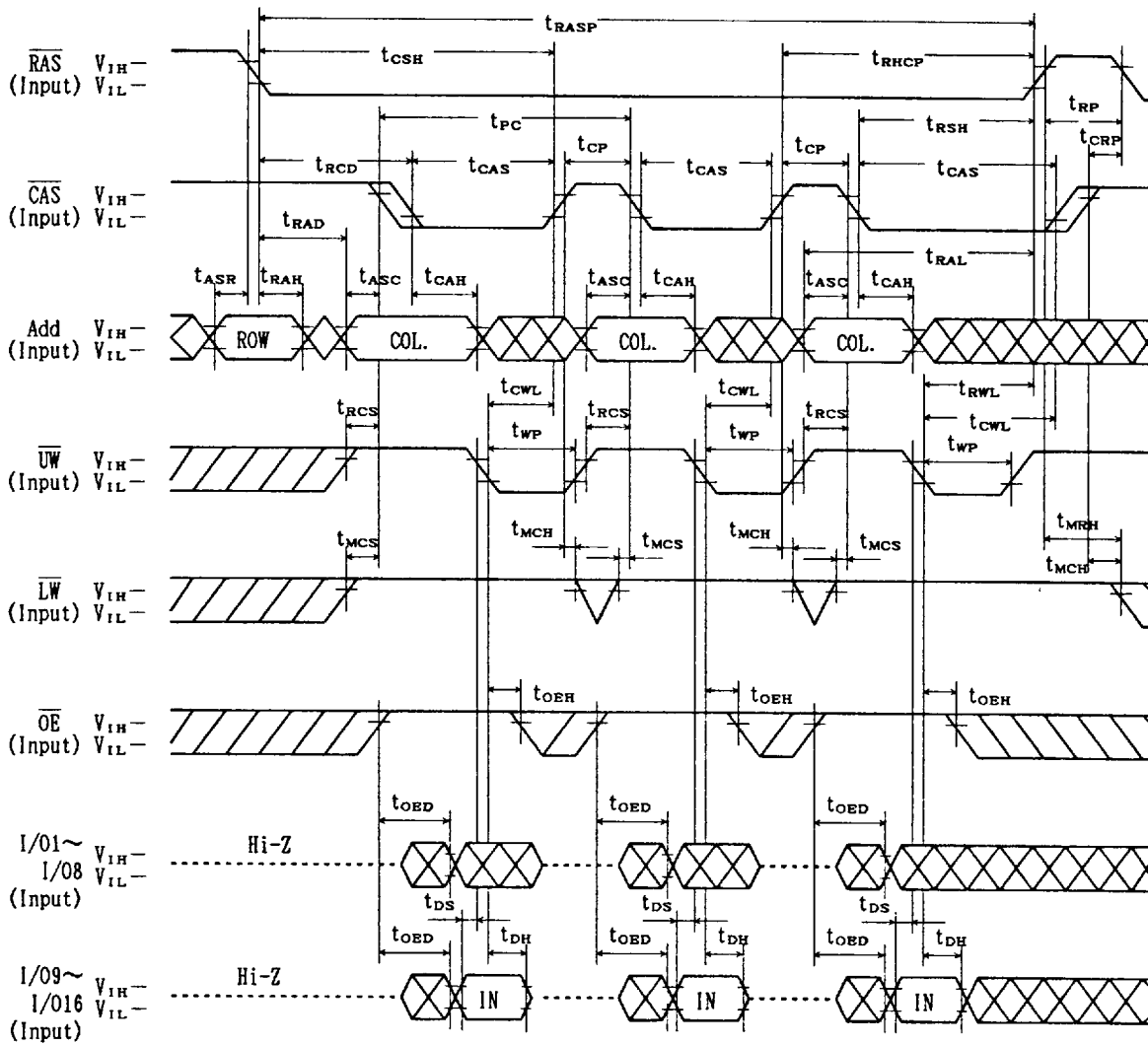
FAST PAGE MODE LOWER BYTE EARLY WRITE CYCLE



Note: \overline{OE} , I/09~I/016=Don't care

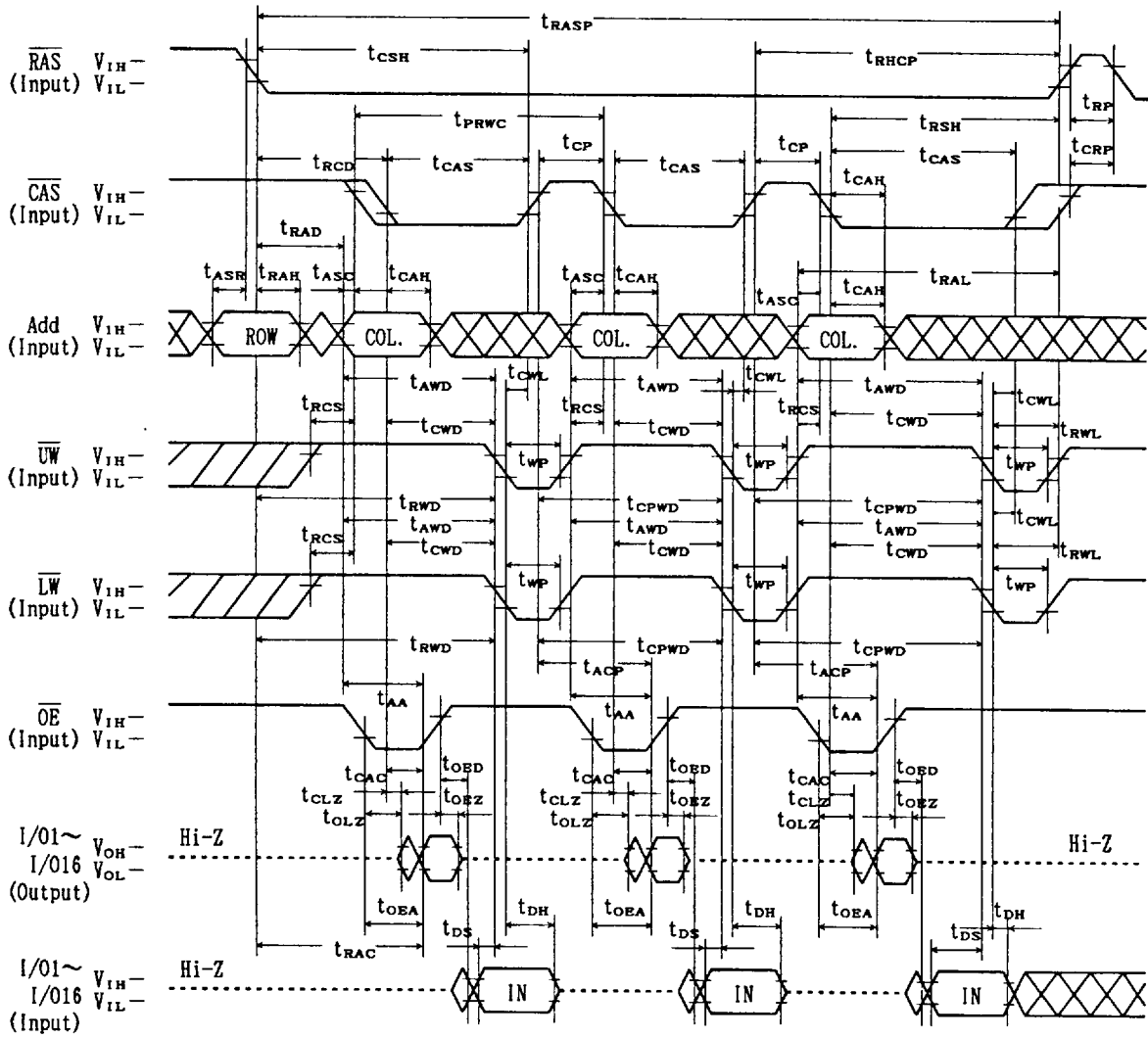
μPD42S16170L, 42S17170L, 42S18170L

FAST PAGE MODE (UPPER BYTE LATE WRITE)



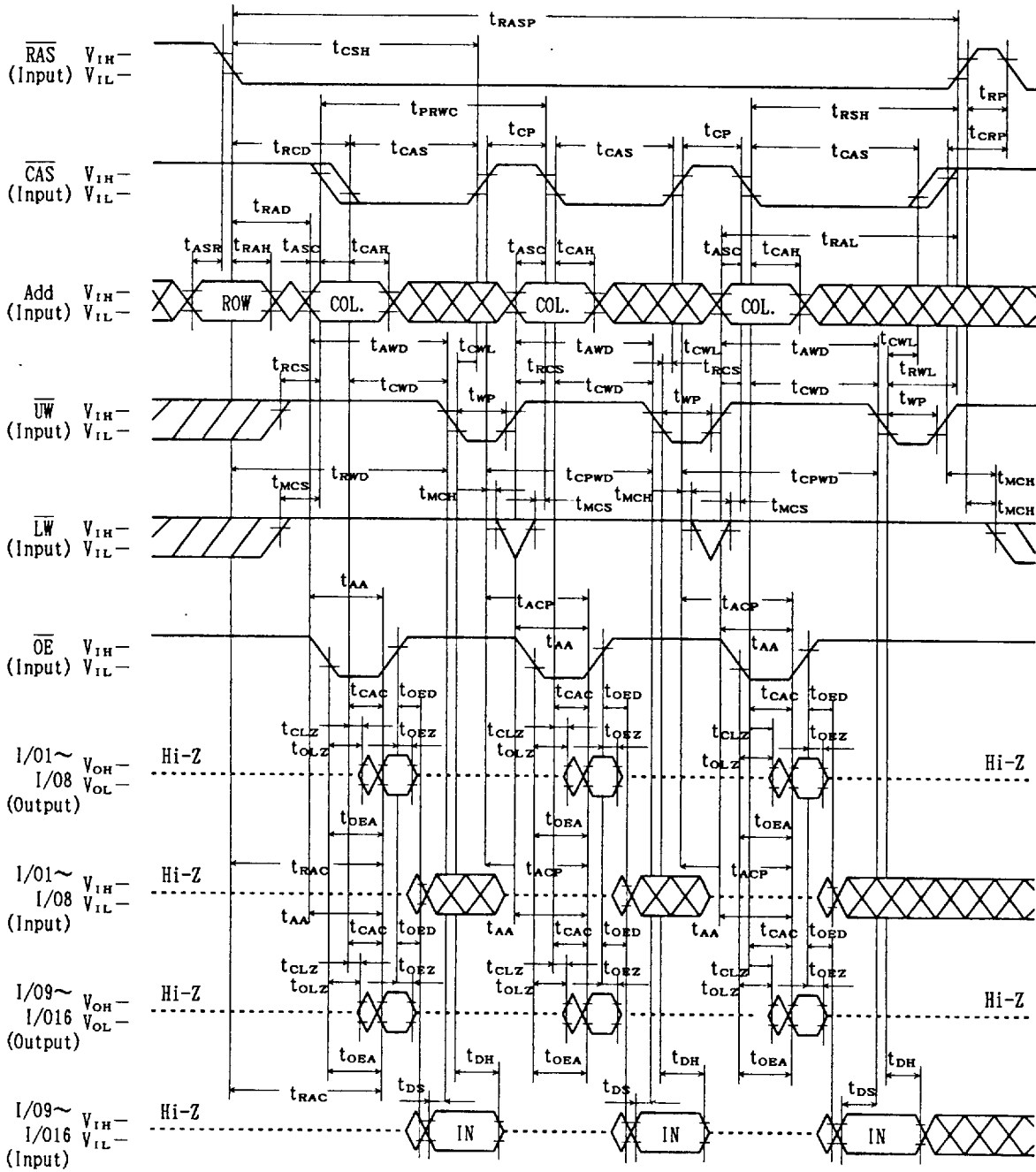
μPD42S16170L, 42S17170L, 42S18170L

FAST PAGE MODE READ MODIFY WRITE CYCLE

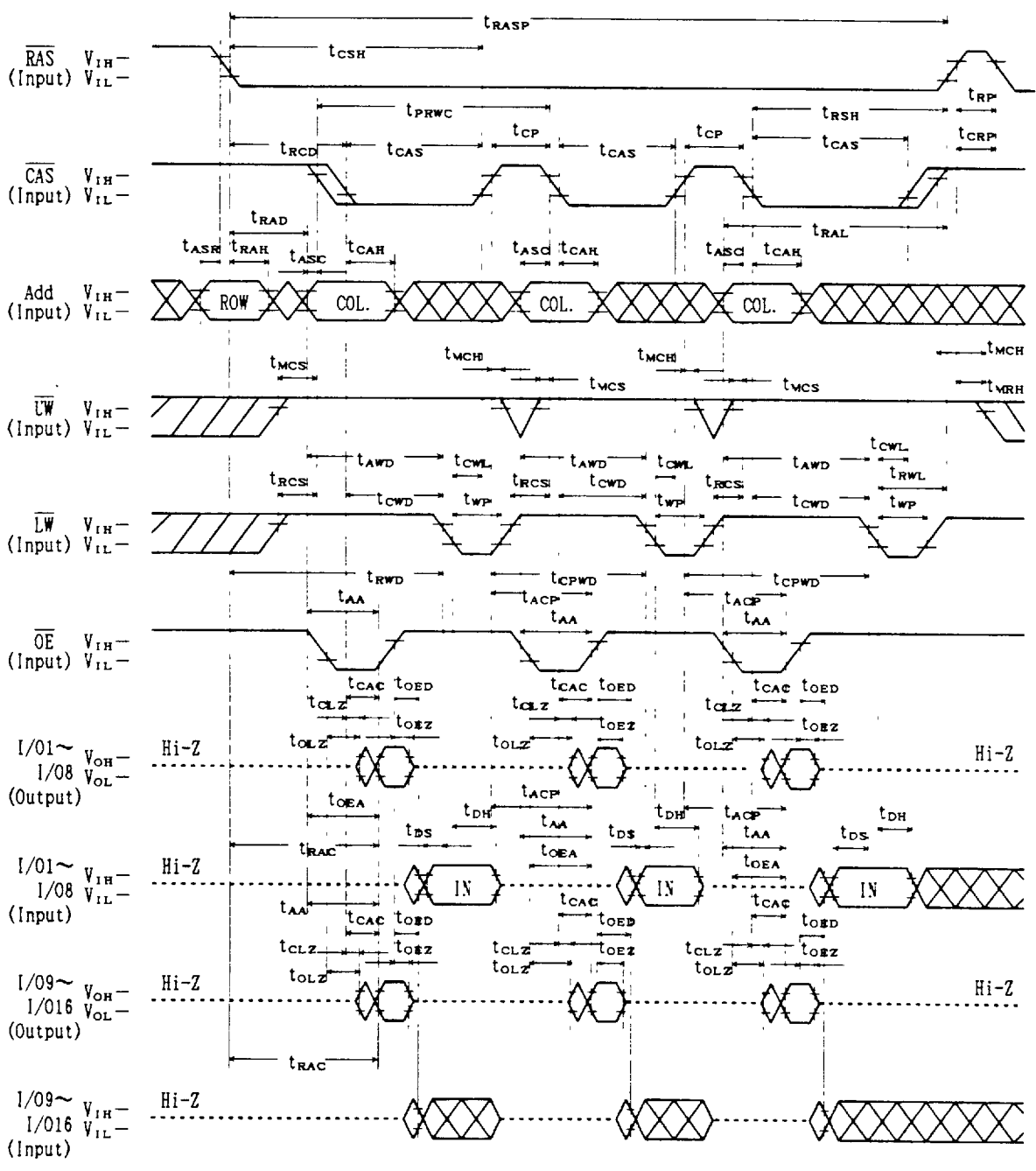


μ PD42S16170L, 42S17170L, 42S18170L

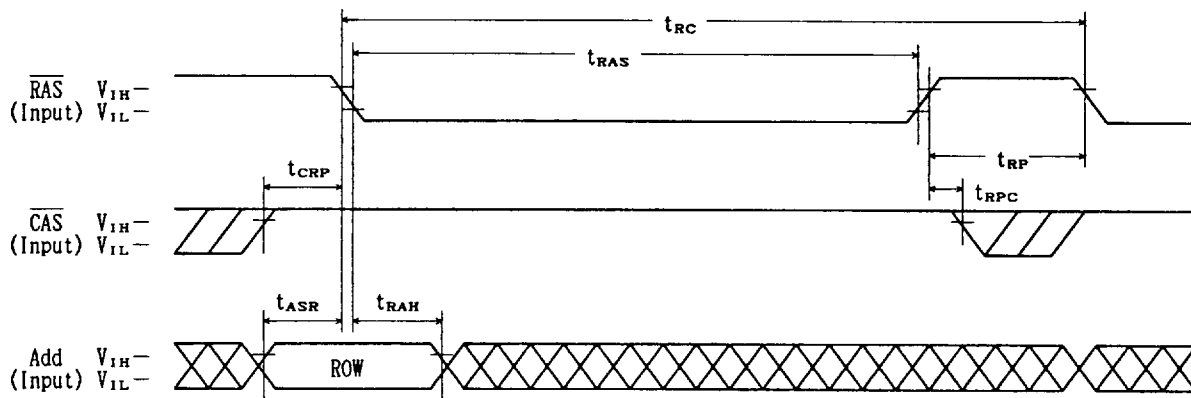
FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE



FAST PAGE MODE LOWER BYTE READ MODIFY WRITE CYCLE

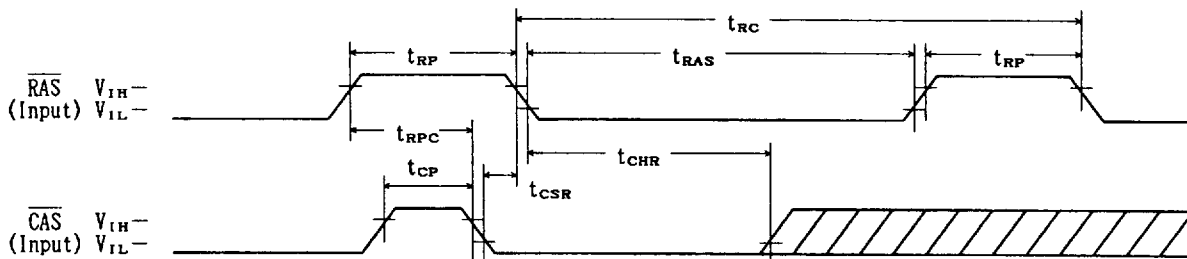


RAS ONLY REFRESH CYCLE



Note : I/01~I/016=Hi-Z

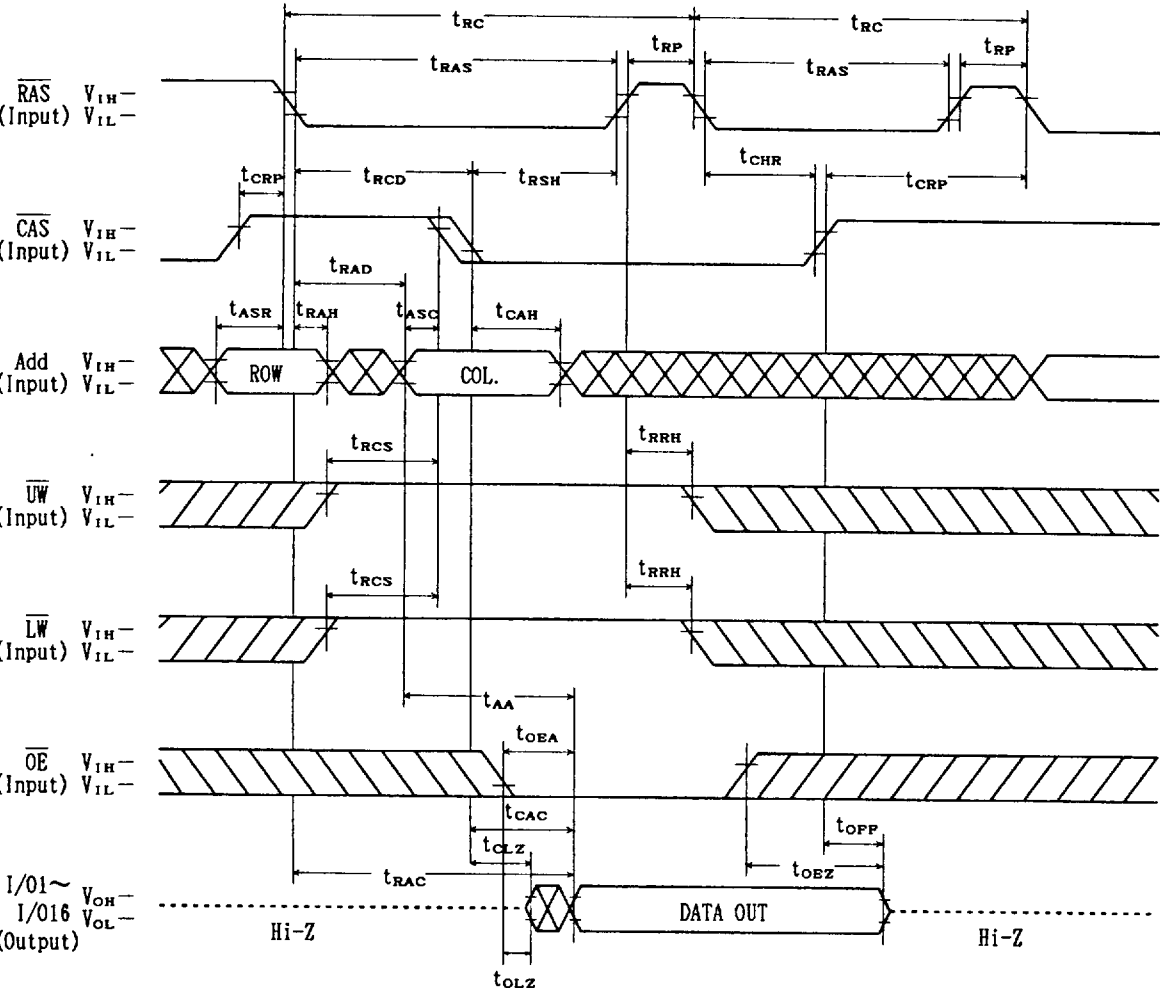
CAS BEFORE RAS REFRESH CYCLE



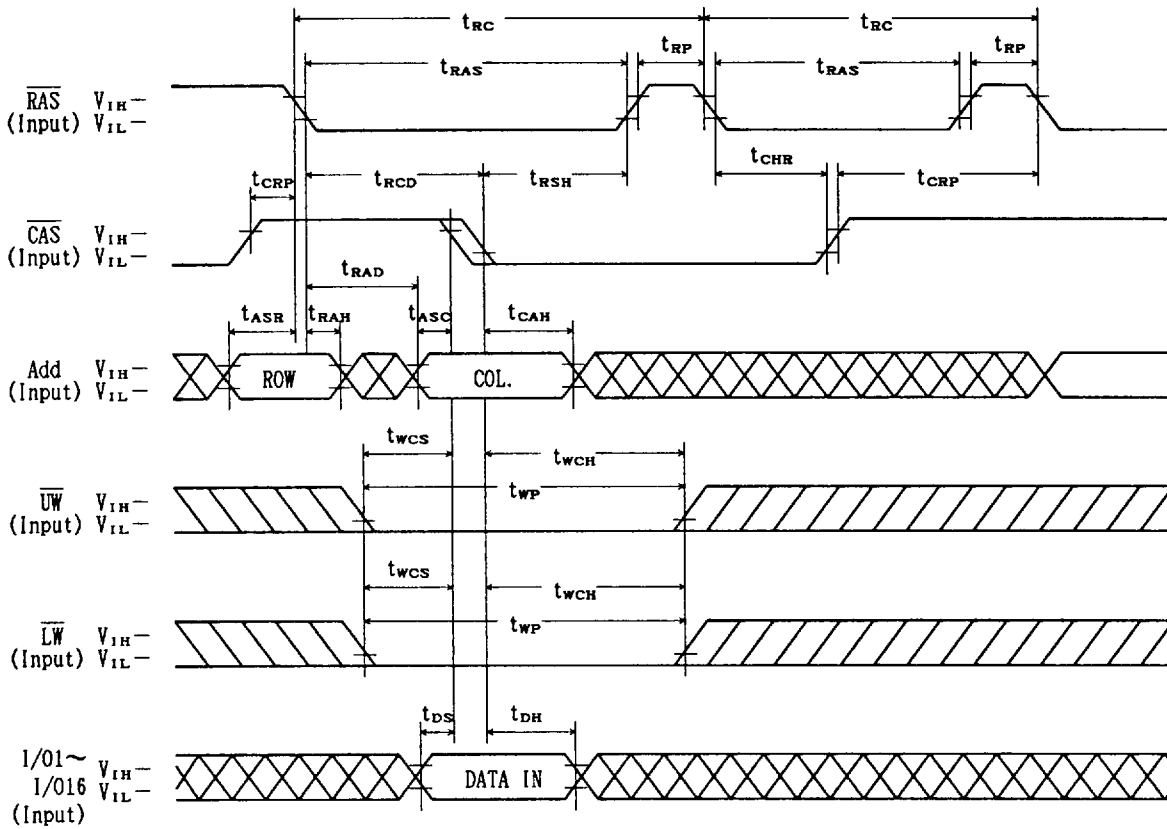
Note : Add=Don't care, I/01~I/016=Hi-Z

μ PD42S16170L, 42S17170L, 42S18170L

HIDDEN REFRESH CYCLE (READ)

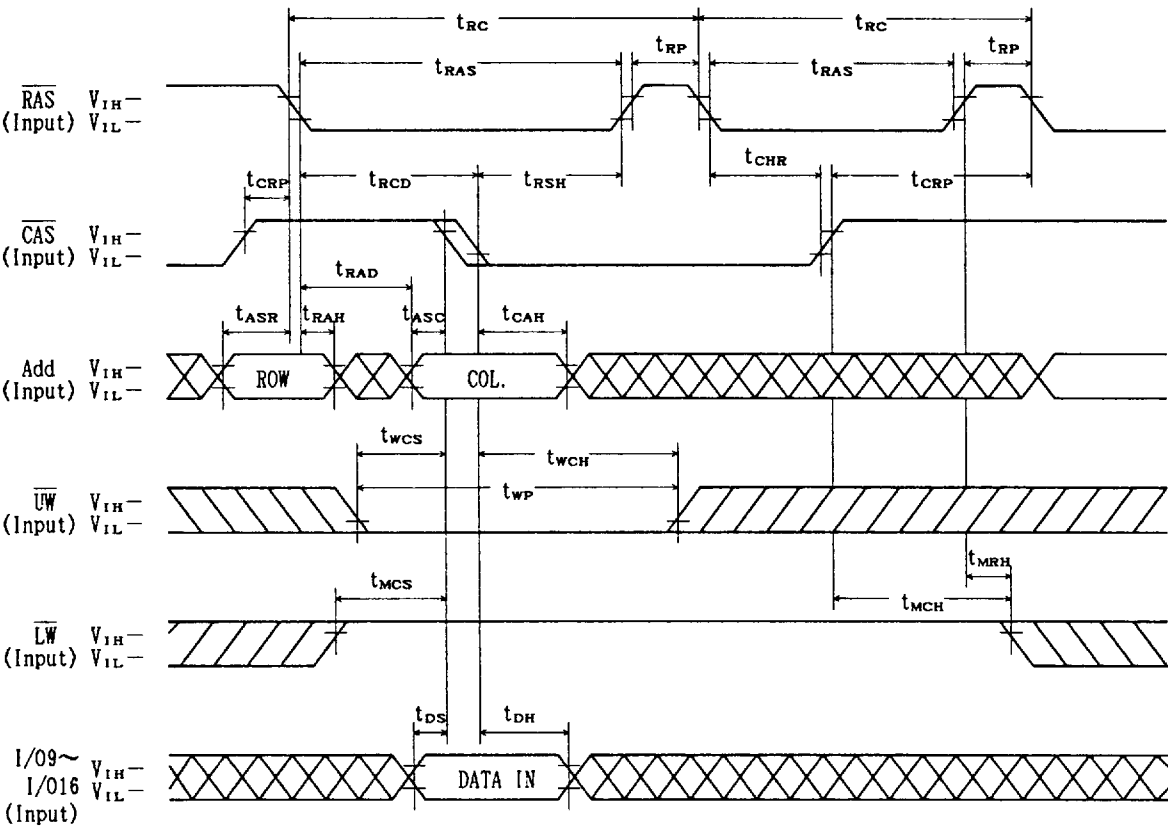


HIDDEN REFRESH CYCLE (WRITE)



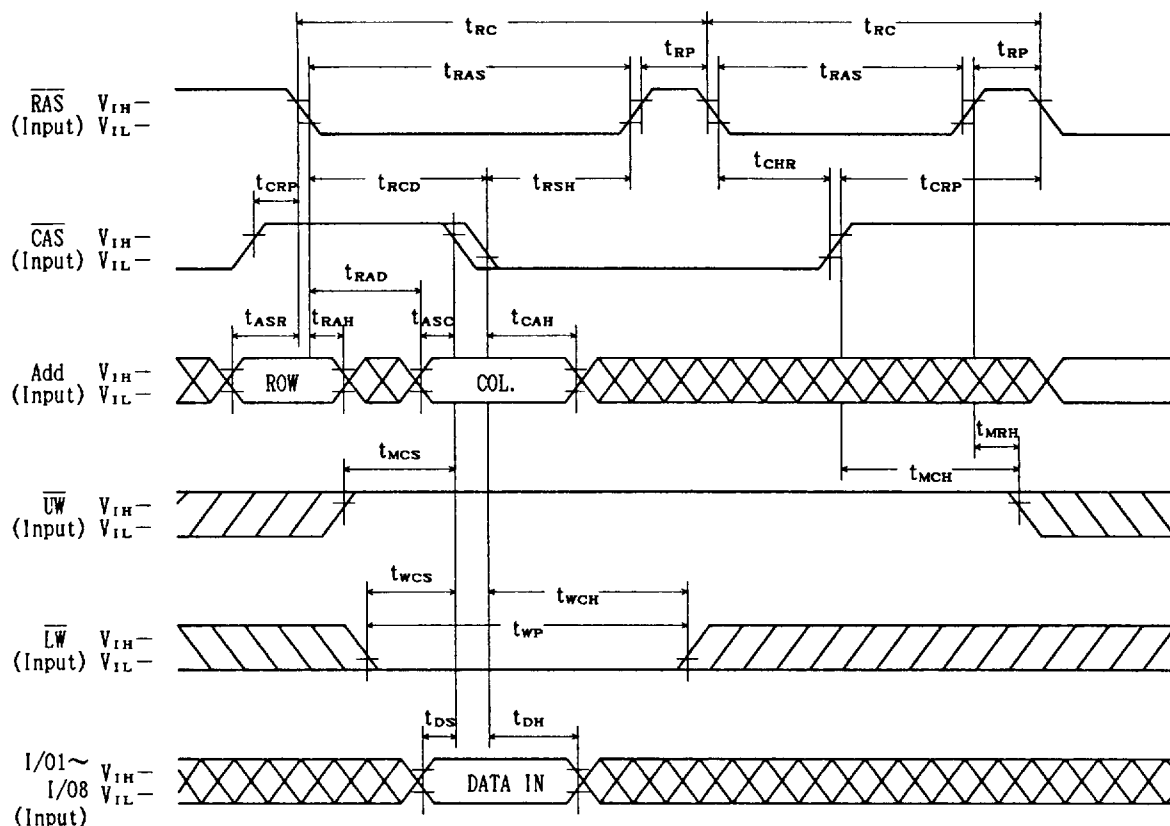
Note: \overline{OE} = Don't care

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



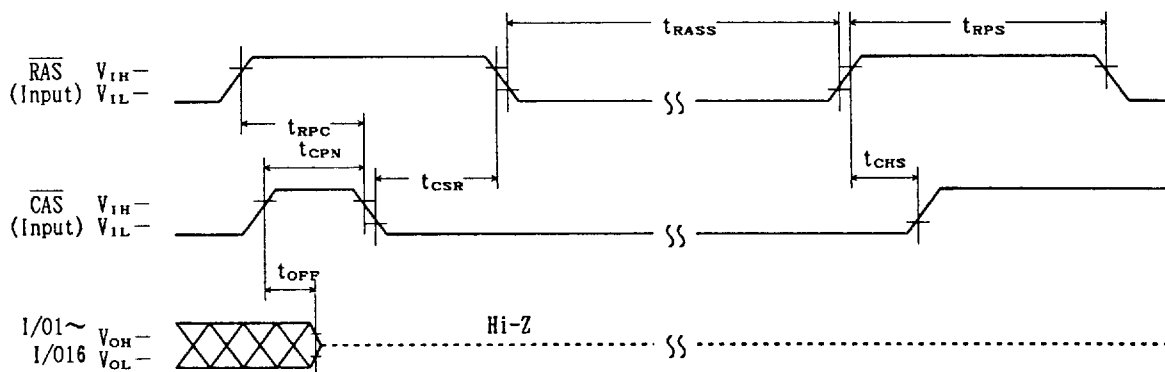
Note: \overline{OE} , I/01~I/08=Don't care

HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Note: \overline{OE} , I/09~I/016=Don't care

CAS BEFORE RAS SELF REFRESH CYCLE



3. PACKAGE DRAWINGS

| | | |
|--------------------------------|-----------------------|-----|
| 26 PIN PLASTIC SOJ (300mil) | 24 Leads | 495 |
| 28 PIN PLASTIC SOJ (400mil) | 24 Leads | 496 |
| 28 PIN PLASTIC SOJ (400mil) | 28 Leads | 497 |
| 32 PIN PLASTIC SOJ (400mil) | | 498 |
| 42 PIN PLASTIC SOJ (400mil) | | 499 |
| 26 PIN PLASTIC TSOP (300mil) * | 24 Leads | 500 |
| 26 PIN PLASTIC TSOP (300mil) * | 24 Leads Reverse bent | 501 |
| 28 PIN PLASTIC TSOP (400mil) | 24 Leads | 502 |
| 28 PIN PLASTIC TSOP (400mil) | 24 Leads Reverse bent | 503 |
| 28 PIN PLASTIC TSOP (400mil) | 28 Leads | 504 |
| 28 PIN PLASTIC TSOP (400mil) | 28 Leads Reverse bent | 505 |
| 32 PIN PLASTIC TSOP (400mil) | | 506 |
| 32 PIN PLASTIC TSOP (400mil) | Reverse bent | 507 |
| 50 PIN PLASTIC TSOP (400mil) | 44 Leads | 508 |
| 50 PIN PLASTIC TSOP (400mil) | 44 Leads Reverse bent | 509 |
| 24 PIN PLASTIC ZIP (475mil) | | 510 |
| 28 PIN PLASTIC ZIP (475mil) | | 511 |
| 32 PIN PLASTIC ZIP (475mil) | | 512 |

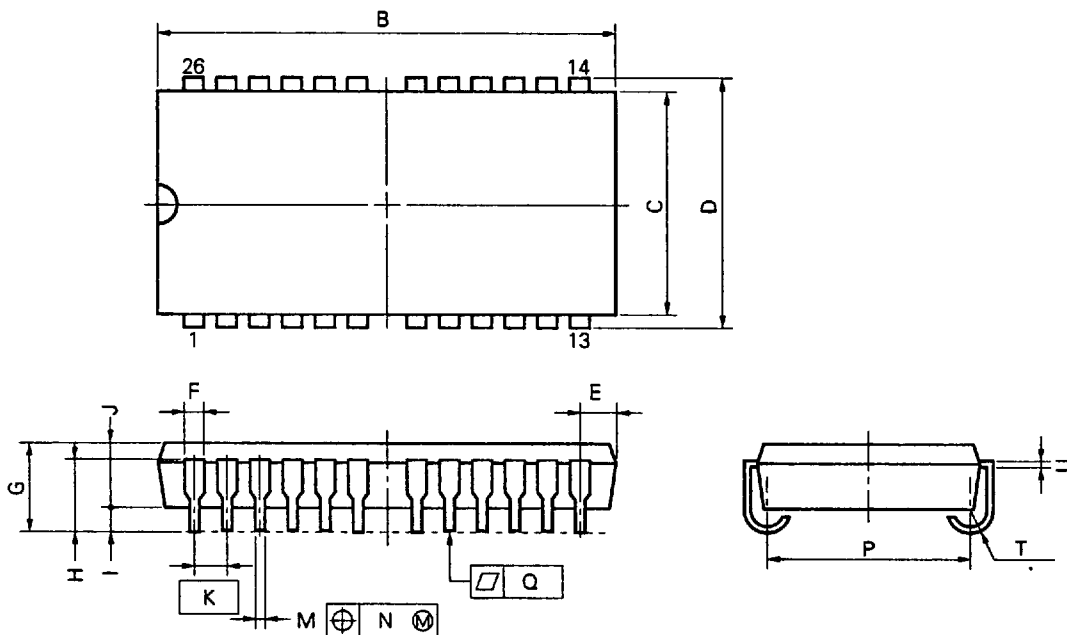
* : under development

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26 PIN PLASTIC SOJ (300mil)
24 Leads

NEC Cord:S26LA-300A



S26LA-300A

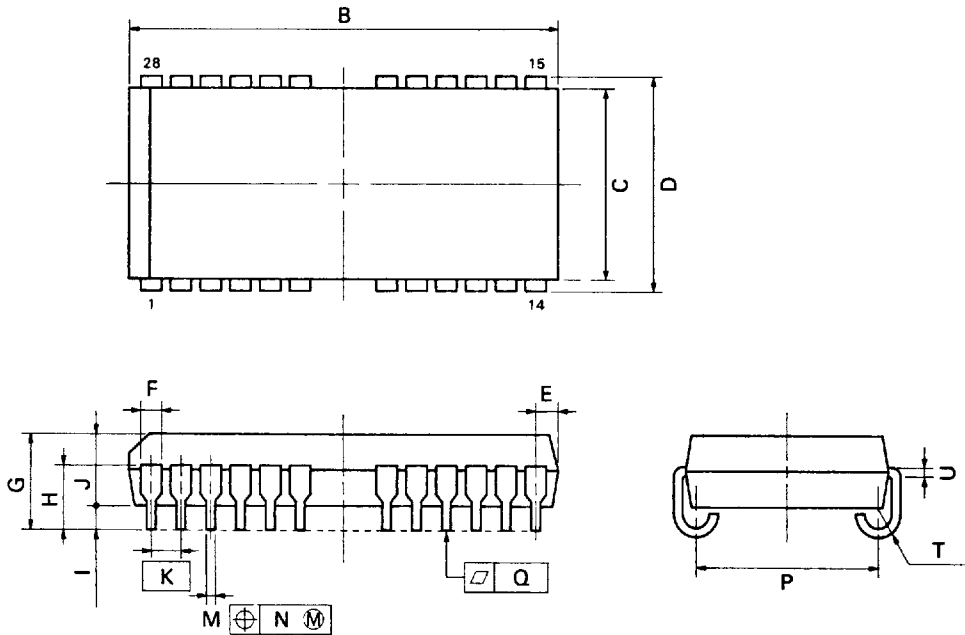
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| B | 17.1 ^{+0.25} _{-0.05} | 0.673 ^{+0.010} _{-0.002} |
| C | 7.62 | 0.300 |
| D | 8.47±0.2 | 0.333 ^{+0.009} _{-0.008} |
| E | 1.03±0.15 | 0.041 ^{+0.006} _{-0.007} |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138±0.008 |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN. | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| N | 0.12 | 0.005 |
| P | 6.73±0.20 | 0.265±0.008 |
| Q | 0.10 | 0.004 |
| T | R 0.85 | R 0.033 |
| U | 0.20 ^{+0.10} _{-0.05} | 0.008 ^{+0.004} _{-0.002} |

28 PIN PLASTIC SOJ (400mil)
24 Leads

NEC Cord:P28LE-400A



P28LE-400A

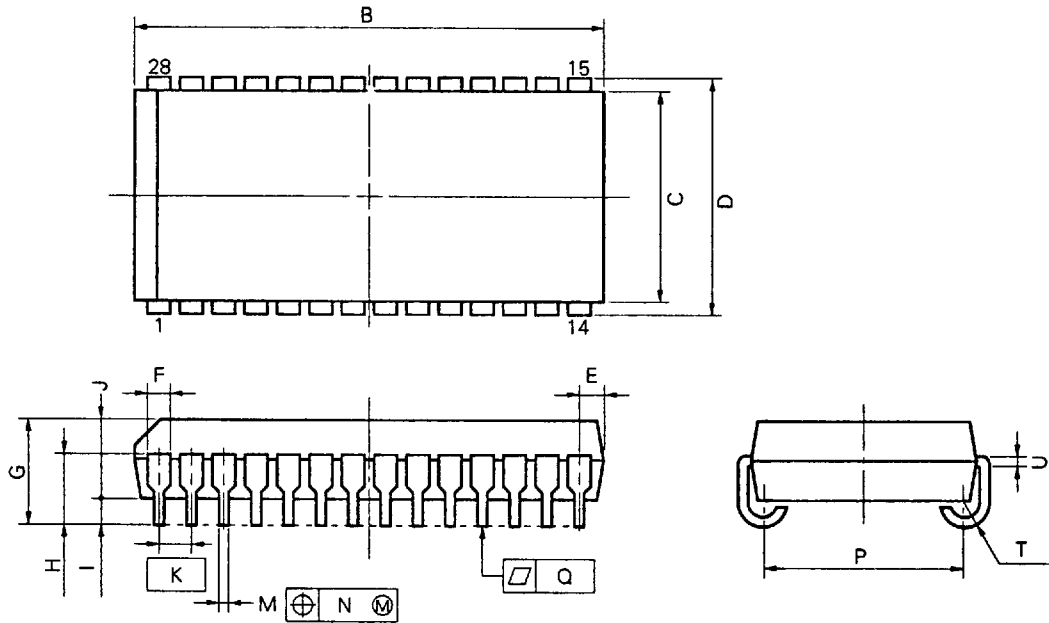
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| B | 18.67 ^{+0.35} _{-0.35} | 0.735 ^{+0.013} _{-0.013} |
| C | 10.16 | 0.400 |
| D | 11.18 ^{+0.2} _{-0.2} | 0.440 ^{+0.008} _{-0.008} |
| E | 1.08 ^{+0.15} _{-0.15} | 0.043 ^{+0.006} _{-0.007} |
| F | 0.7 | 0.028 |
| G | 3.5 ^{+0.2} _{-0.2} | 0.138 ^{+0.009} _{-0.009} |
| H | 2.4 ^{+0.2} _{-0.2} | 0.094 ^{+0.008} _{-0.008} |
| I | 0.8 MIN. | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40 ^{+0.10} _{-0.10} | 0.016 ^{+0.004} _{-0.004} |
| N | 0.12 | 0.005 |
| P | 9.40 ^{+0.20} _{-0.20} | 0.370 ^{+0.008} _{-0.008} |
| Q | 0.15 | 0.006 |
| T | R0.85 | R0.033 |
| U | 0.20 ^{+0.08} _{-0.08} | 0.008 ^{+0.002} _{-0.002} |

28 PIN PLASTIC SOJ (400mil)
28 Leads

NEC Cord:P28LE-400A1



NOTE

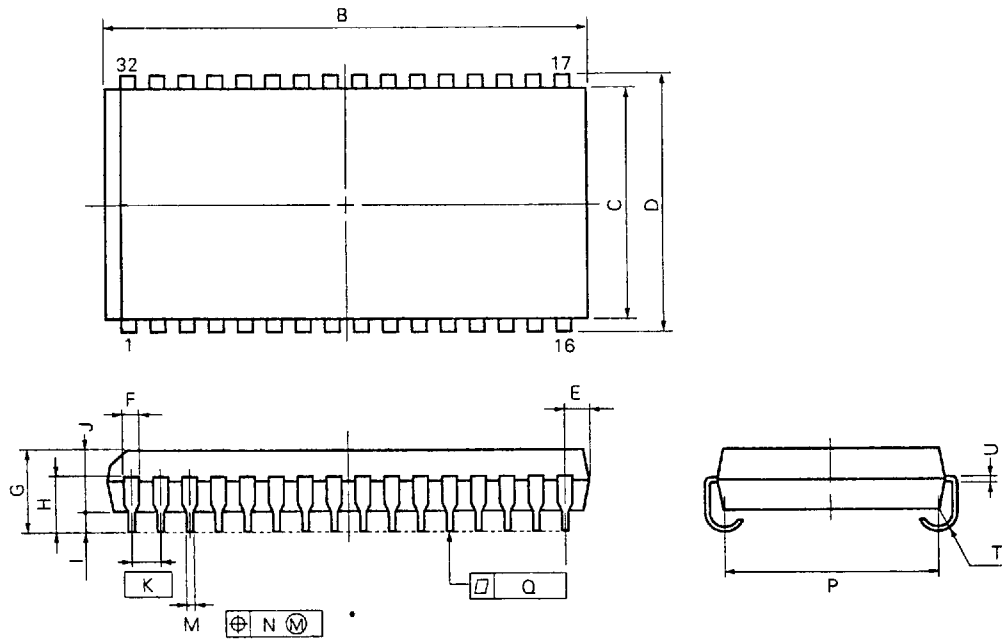
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P28LE-400A1

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| B | 18.67 ^{+0.2} _{-0.35} | 0.735 ^{+0.008} _{-0.013} |
| C | 10.16 | 0.400 |
| D | 11.18±0.2 | 0.440 ^{+0.008} _{-0.007} |
| E | 1.08±0.15 | 0.043 ^{+0.006} _{-0.007} |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138 ^{+0.008} _{-0.007} |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| N | 0.12 | 0.005 |
| P | 9.40±0.20 | 0.370 ^{+0.008} _{-0.007} |
| Q | 0.10 | 0.004 |
| T | R 0.85 | R 0.033 |
| U | 0.20 ^{+0.10} _{-0.05} | 0.008 ^{+0.004} _{-0.002} |

32 PIN PLASTIC SOJ (400mil)

NEC Cord:P32LE-400A



NOTE

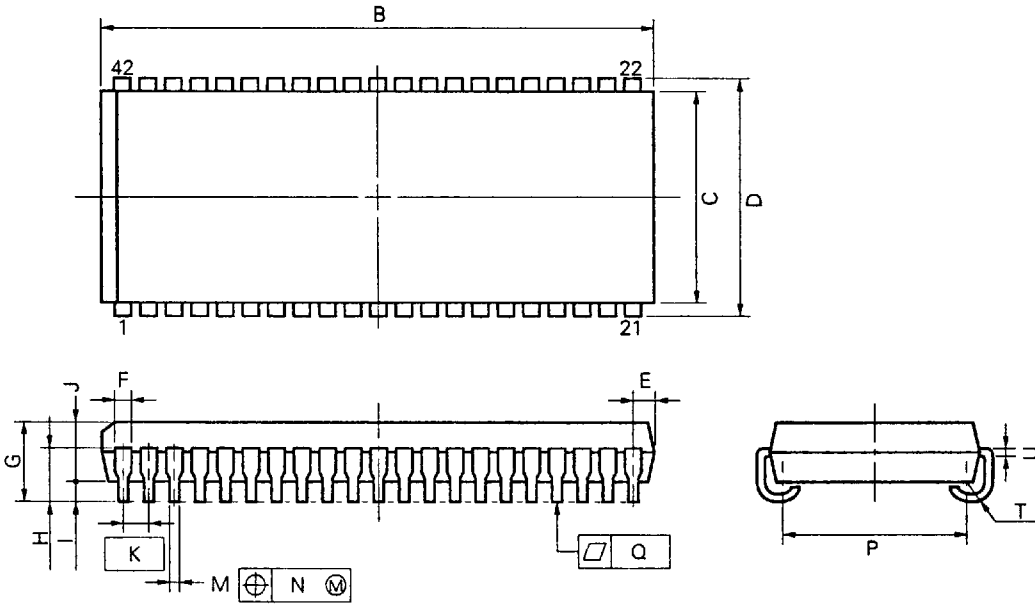
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition

P32LE-400A

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| B | 21.06±0.2 | 0.829±0.008 |
| C | 10.16 | 0.400 |
| D | 11.18±0.2 | 0.440±0.008 |
| E | 1.005±0.1 | 0.040 ^{+0.004} _{-0.005} |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138±0.008 |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN | 0.031 MIN |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| N | 0.12 | 0.005 |
| P | 9.4±0.20 | 0.370±0.008 |
| Q | 0.1 | 0.004 |
| T | R 0.85 | R 0.033 |
| U | 0.20 ^{+0.10} _{-0.02} | 0.008 ^{+0.004} _{-0.002} |

42 PIN PLASTIC SOJ (400mil)

NEC Cord: P42LE-400A



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

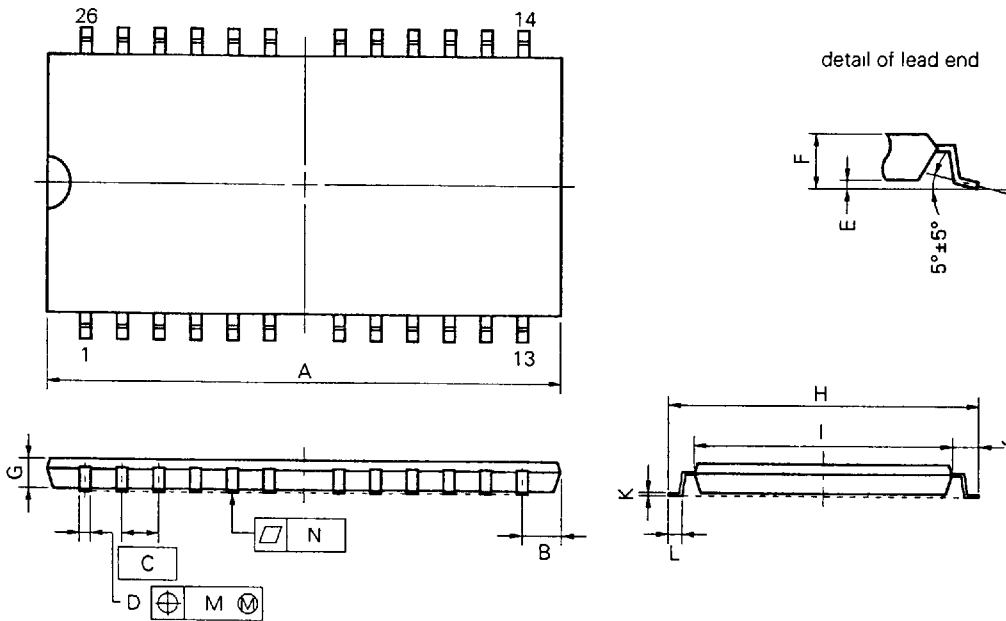
P42LE-400A

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| B | 27.56 ^{+0.2} _{-0.35} | 1.085 ^{+0.008} _{-0.014} |
| C | 10.16 | 0.400 |
| D | 11.18±0.2 | 0.440±0.008 |
| E | 1.08±0.15 | 0.043 ^{+0.006} _{-0.007} |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138±0.008 |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN. | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| N | 0.12 | 0.005 |
| P | 9.4±0.20 | 0.370±0.008 |
| Q | 0.10 | 0.004 |
| T | R 0.85 | R 0.033 |
| U | 0.20 ^{+0.10} _{-0.05} | 0.008 ^{+0.004} _{-0.002} |

26 PIN PLASTIC TSOP (300mil) *
24 Leads

* : under development

NEC Cord:S26G3-50-7JD



NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

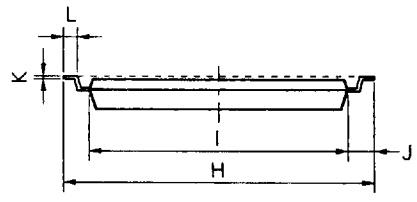
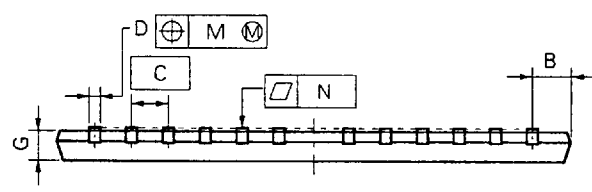
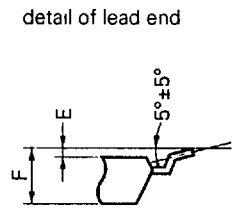
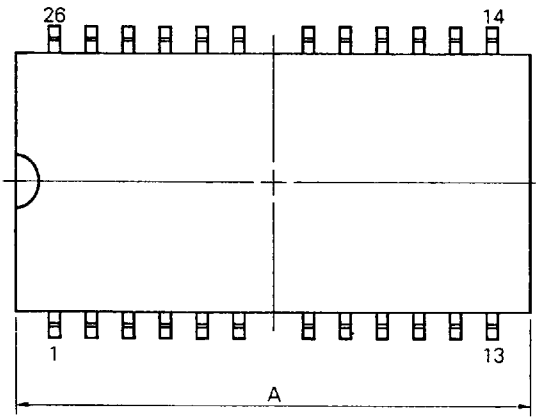
S26G3-50-7JD

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 17.40 MAX. | 0.685 MAX. |
| B | 1.06 MAX. | 0.042 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} / _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 9.22±0.2 | 0.363±0.008 |
| I | 7.62±0.1 | 0.300±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} / _{-0.008} |
| K | 0.125 ^{+0.10} / _{-0.05} | 0.005 ^{+0.004} / _{-0.002} |
| L | 0.5±0.1 | 0.020 ^{+0.004} / _{-0.005} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

26 PIN PLASTIC TSOP (300mil) *
24 Leads Reverse bent

* : under development

NEC Cord:S26G3-50-7KD



S26G3-50-7KD

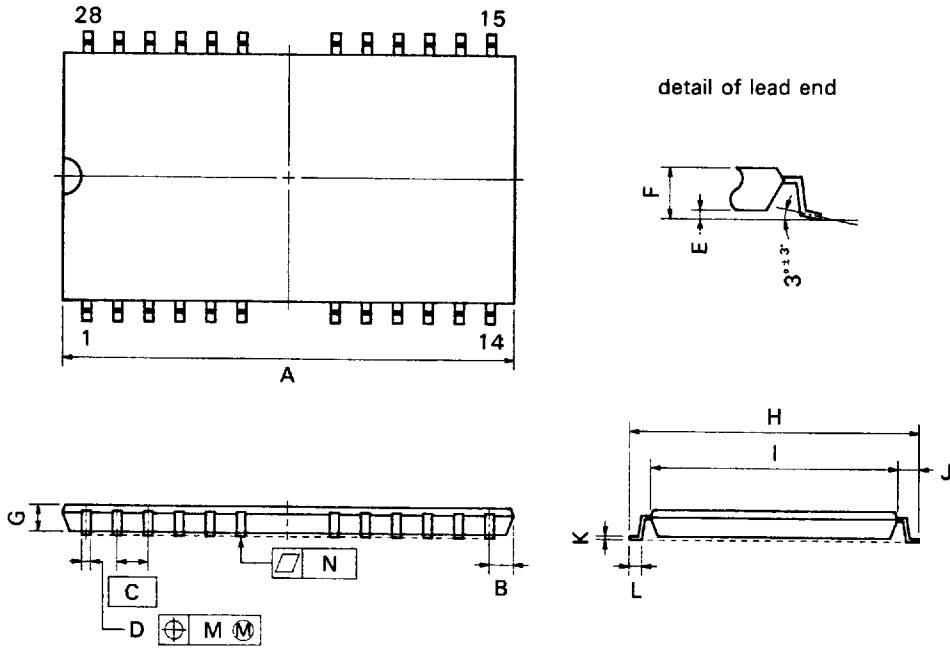
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P) at maximum material condition

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 17.40 MAX. | 0.685 MAX. |
| B | 1.06 MAX. | 0.042 MAX. |
| C | 1.27 (T P) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 9.22±0.2 | 0.363±0.008 |
| I | 7.62±0.1 | 0.300±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.125 ^{+0.10} _{-0.05} | 0.005 ^{+0.004} _{-0.002} |
| L | 0.5±0.1 | 0.020 ^{+0.004} _{-0.005} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

28 PIN PLASTIC TSOP (400mil)
24 Leads

NEC Cord:S28G5-50-7JD1



NOTE

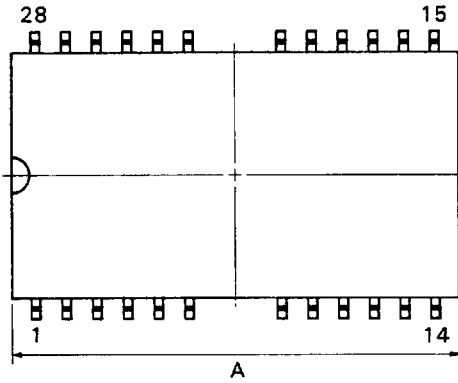
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD1

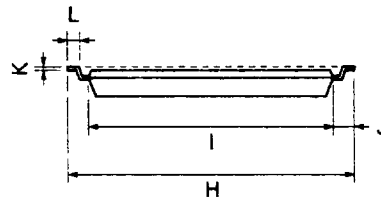
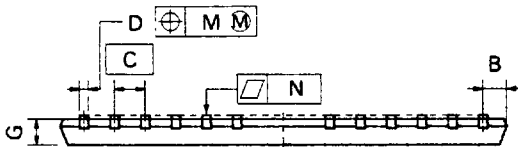
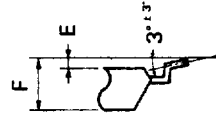
| ITEM | MILLIMETERS | INCHES |
|------|------------------------|-------------------------|
| A | 18.81 MAX. | 0.741 MAX. |
| B | 1.15 MAX. | 0.046 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40 ^{+0.10} | 0.016 ^{+0.004} |
| E | 0.05 ^{+0.05} | 0.002 ^{+0.002} |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76 ^{+0.2} | 0.463 ^{+0.008} |
| I | 10.16 ^{+0.1} | 0.400 ^{+0.004} |
| J | 0.8 ^{+0.2} | 0.031 ^{+0.008} |
| K | 0.125 ^{+0.10} | 0.005 ^{+0.004} |
| L | 0.5 ^{+0.1} | 0.020 ^{+0.004} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

28 PIN PLASTIC TSOP (400mil)
24 Leads Reverse bent

NEC Cord:S28G5-50-7KD1



detail of lead end



S28G5-50-7KD1

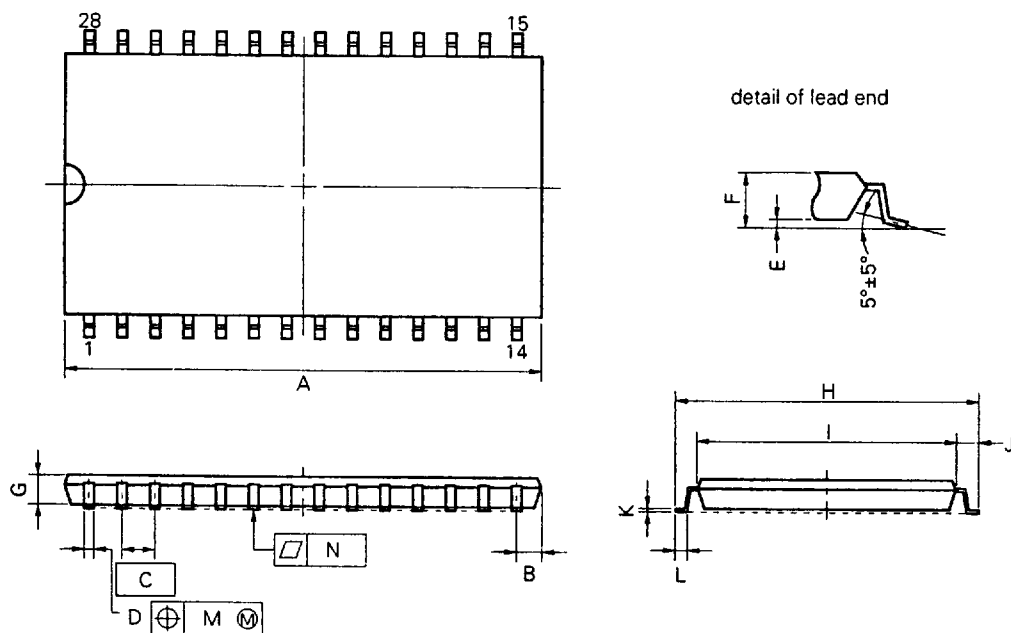
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|-------------------------|-------------------------|
| A | 18.81 MAX. | 0.741 MAX. |
| B | 1.15 MAX. | 0.046 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40 ^{+0.10} | 0.016 ^{-0.005} |
| E | 0.05 ^{+0.05} | 0.002 ^{+0.002} |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76 ^{+0.2} | 0.463 ^{+0.008} |
| I | 10.16 ^{+0.1} | 0.400 ^{+0.004} |
| J | 0.8 ^{+0.2} | 0.031 ^{-0.008} |
| K | 0.125 ^{-0.018} | 0.005 ^{-0.002} |
| L | 0.5 ^{+0.1} | 0.020 ^{-0.005} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

28 PIN PLASTIC TSOP (400mil)
28 Leads

NEC Cord:S28G5-50-7JD2



NOTE

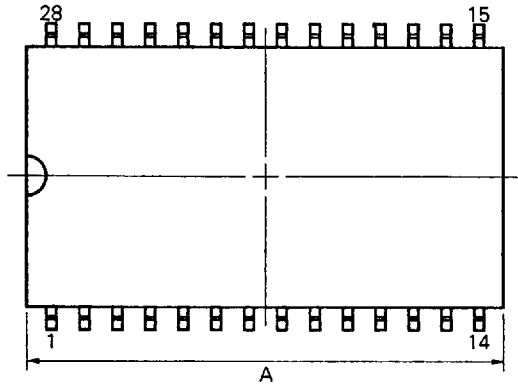
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S28G5-50-7JD2

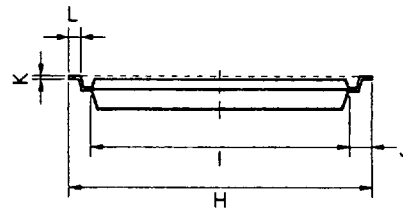
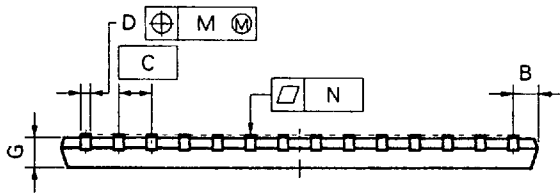
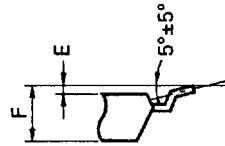
| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 18.81 MAX. | 0.741 MAX. |
| B | 1.15 MAX. | 0.046 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.125 ^{+0.10} _{-0.05} | 0.005 ^{+0.004} _{-0.002} |
| L | 0.5±0.15 | 0.020 ^{+0.006} _{-0.007} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

28 PIN PLASTIC TSOP (400mil)
28 Leads Reverse bent

NEC Cord:S28G5-50-7KD2



detail of lead end



S28G5-50-7KD2

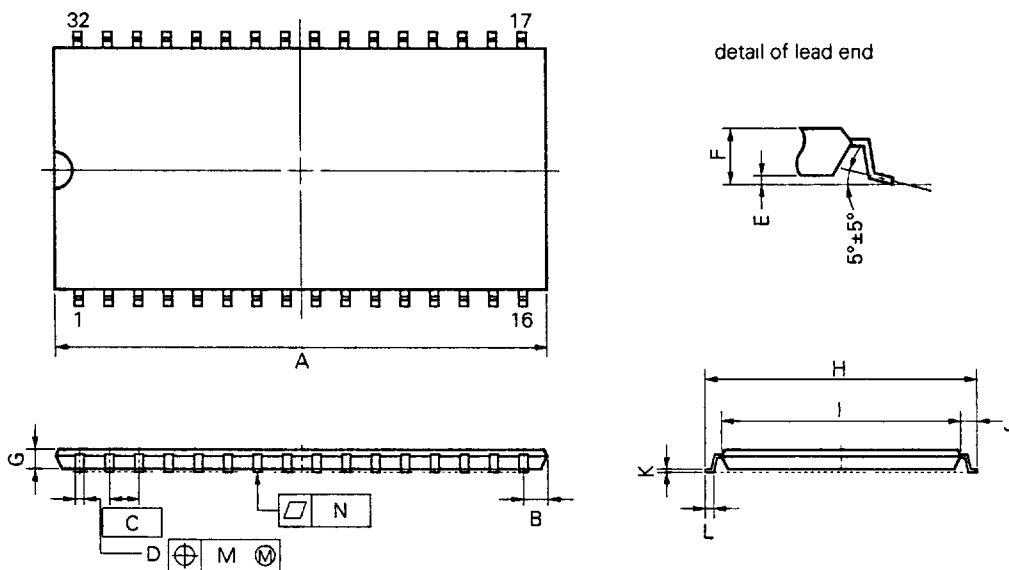
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 18.81 MAX. | 0.741 MAX. |
| B | 1.15 MAX. | 0.046 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.125 ^{+0.10} _{-0.05} | 0.005 ^{+0.004} _{-0.002} |
| L | 0.5±0.15 | 0.020 ^{+0.006} _{-0.007} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

32 PIN PLASTIC TSOP (400mil)

NEC Cord:S32G5-50-7JD1



NOTE

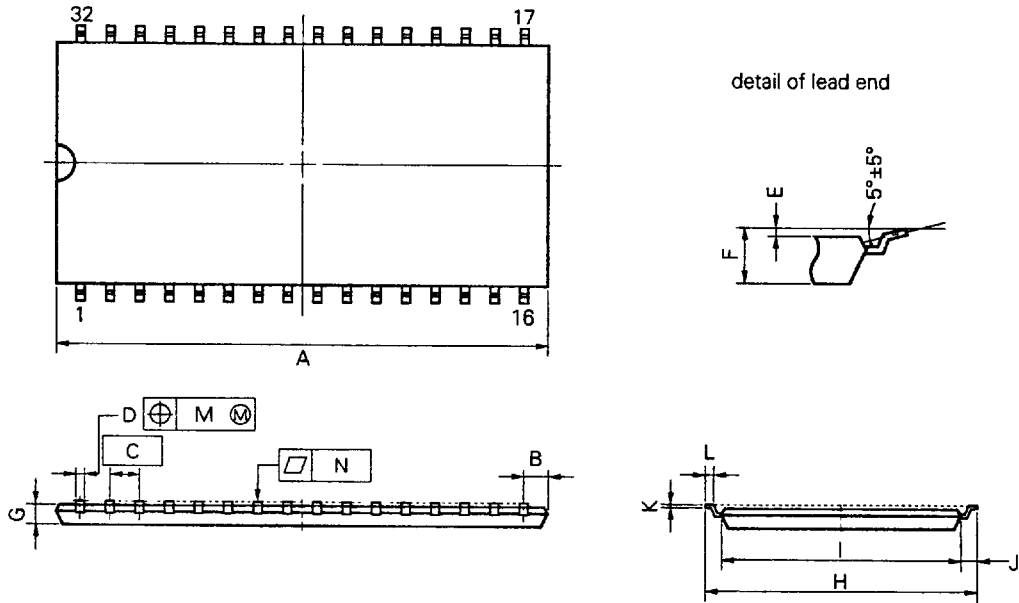
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S32G5-50-7JD1

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 21.17 MAX. | 0.834 MAX. |
| B | 1.06 MAX. | 0.042 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.125 ^{+0.10} _{-0.05} | 0.005 ^{+0.004} _{-0.002} |
| L | 0.5±0.15 | 0.020 ^{+0.006} _{-0.007} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

32 PIN PLASTIC TSOP (400mil)
Reverse bent

NEC Cord:S32G5-50-7KD1



NOTE

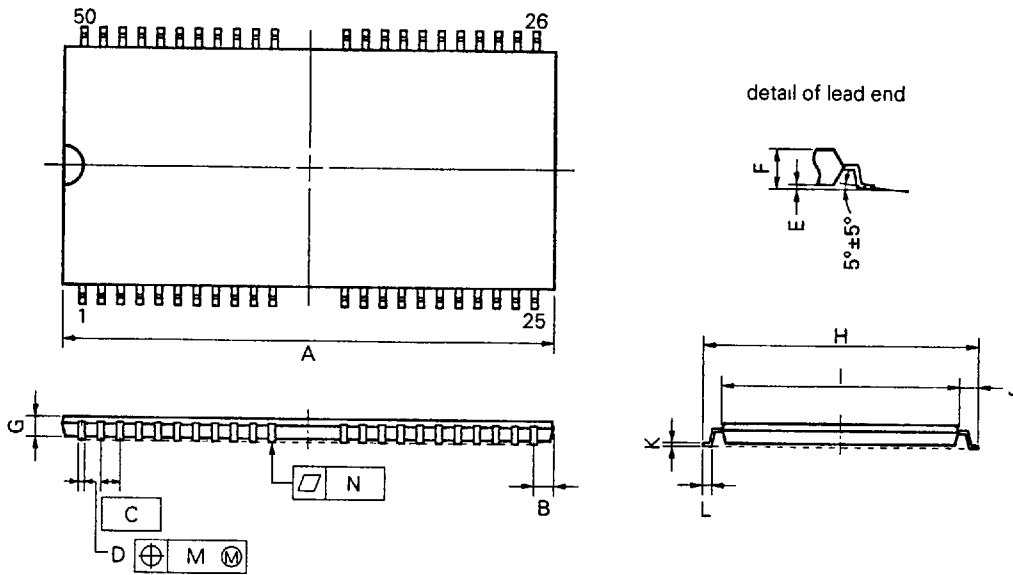
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

S32G5-50-7KD1

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 21.17 MAX. | 0.834 MAX. |
| B | 1.06 MAX. | 0.042 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.125 ^{+0.10} _{-0.05} | 0.005 ^{+0.004} _{-0.002} |
| L | 0.5±0.15 | 0.020 ^{+0.006} _{-0.007} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |

50 PIN PLASTIC TSOP (400mil)
44 Leads

NEC Cord:S50G5-80-7JF



NOTE

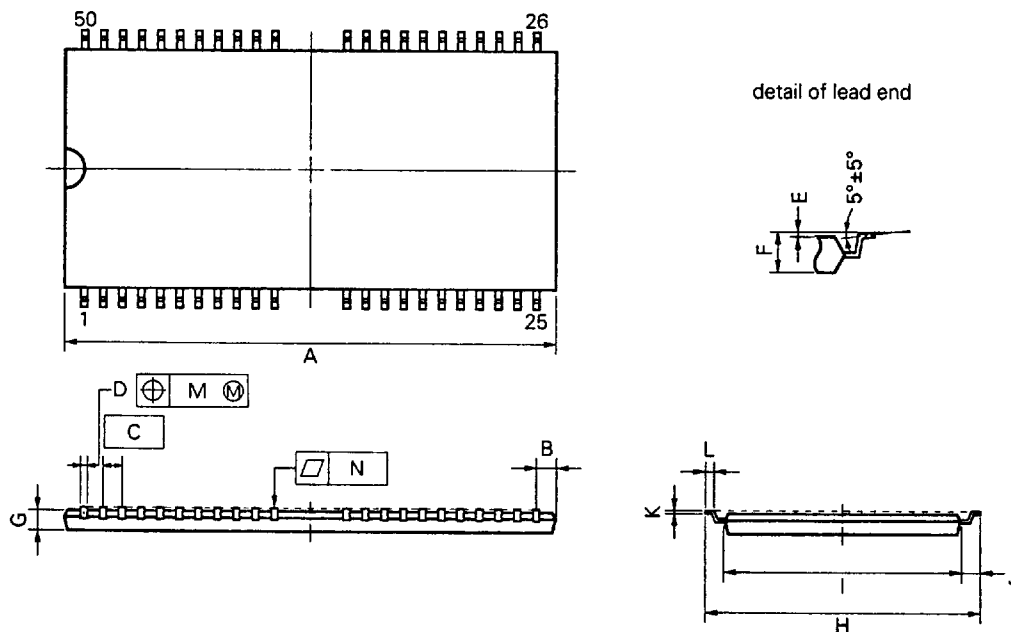
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7JF

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 21.45 MAX. | 0.845 MAX. |
| B | 1.13 MAX. | 0.045 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | 0.30±0.10 | 0.012 ^{+0.004} _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.125 ^{+0.10} _{-0.05} | 0.005 ^{+0.004} _{-0.002} |
| L | 0.5±0.15 | 0.020 ^{+0.006} _{-0.007} |
| M | 0.13 | 0.005 |
| N | 0.10 | 0.004 |

50 PIN PLASTIC TSOP (400mil)
44 Leads Reverse bent

NEC Cord:S50G5-80-7KF



NOTE

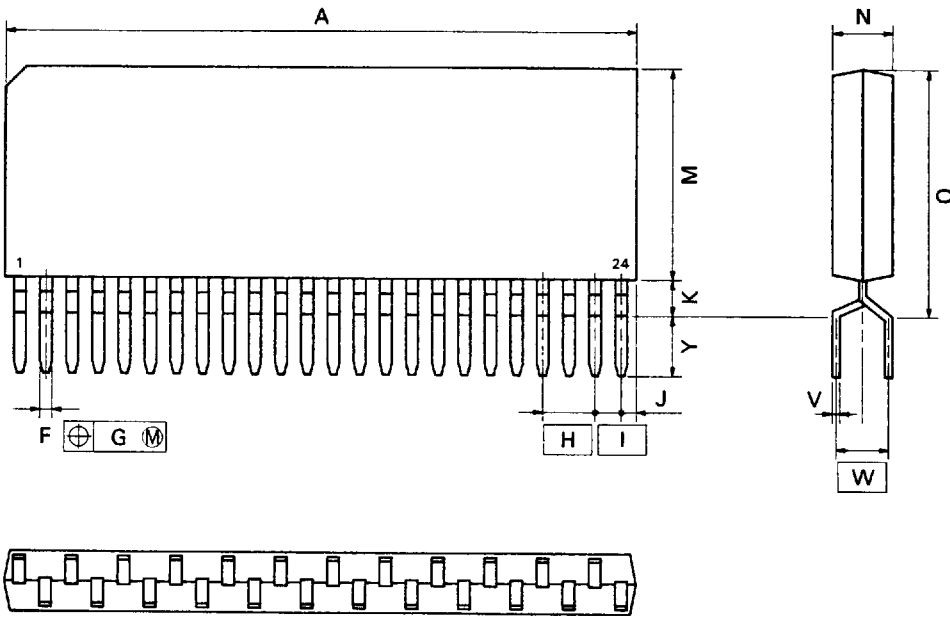
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S50G5-80-7KF

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 21.45 MAX. | 0.845 MAX. |
| B | 1.13 MAX. | 0.045 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | 0.30±0.10 | 0.012 ^{+0.004} / _{-0.005} |
| E | 0.05±0.05 | 0.002±0.002 |
| F | 1.1 MAX. | 0.044 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} / _{-0.008} |
| K | 0.125 ^{+0.10} / _{-0.05} | 0.005 ^{+0.004} / _{-0.002} |
| L | 0.5±0.15 | 0.020 ^{+0.006} / _{-0.007} |
| M | 0.13 | 0.005 |
| N | 0.10 | 0.004 |

24 PIN PLASTIC ZIP (475mil)

NEC Cord:P24V-100-475A



NOTE

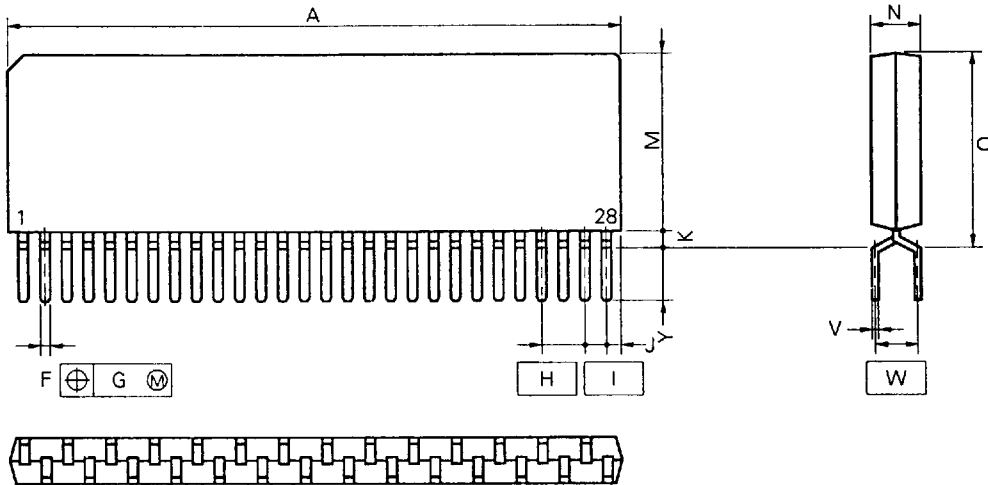
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P24V-100-475A

| ITEM | MILLIMETERS | INCHES |
|------|-----------------------|-------------------------|
| A | 31.75 MAX. | 1.250 MAX. |
| F | 0.50 ^{±0.1} | 0.020 ^{-0.002} |
| G | φ0.25 | φ0.010 |
| H | 2.54 | 0.100 |
| I | 1.27 | 0.050 |
| J | 1.27 MAX. | 0.050 MAX. |
| K | 1.0 MIN. | 0.039 MIN. |
| M | 10.8 MAX. | 0.426 MAX. |
| N | 2.8 ^{±0.2} | 0.110 ^{-0.002} |
| Q | 12.07 MAX. | 0.476 MAX. |
| V | 0.25 ^{+0.10} | 0.010 ^{-0.004} |
| W | 2.54 | 0.100 |
| Y | 3.3 ^{±0.5} | 0.130 ^{±0.02} |

28 PIN PLASTIC ZIP (475mil)

NEC Cord:P28VF-100-475A



NOTE

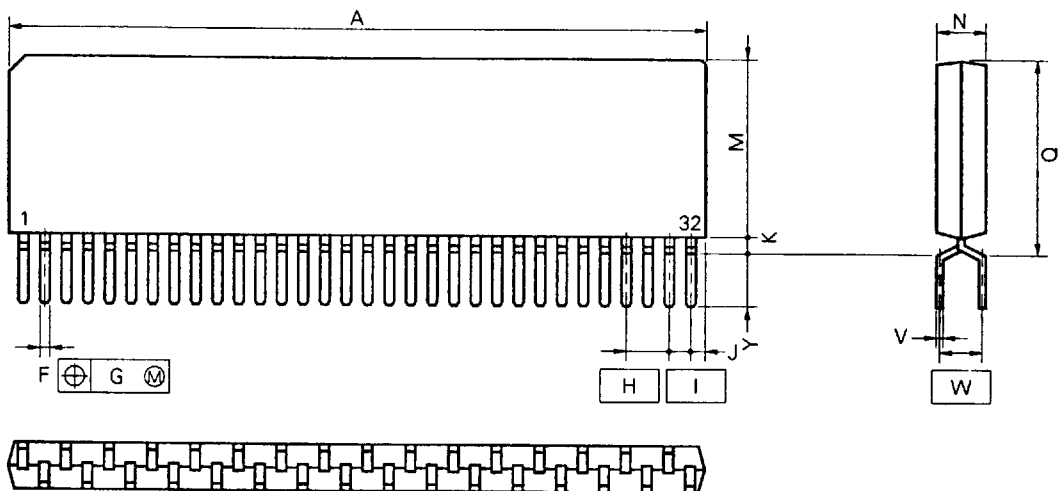
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

P28VF-100-475A

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 36.83 MAX. | 1.450 MAX. |
| F | 0.5 ± 0.10 | 0.020 ^{+0.004} _{-0.005} |
| G | 0.25 | 0.010 |
| H | 2.54 (T.P.) | 0.100 (T.P.) |
| I | 1.27 (T.P.) | 0.050 (T.P.) |
| J | 1.27 MAX. | 0.050 MAX. |
| K | 0.9 MIN. | 0.035 MIN. |
| M | 10.8 MAX. | 0.426 MAX. |
| N | 2.8 ± 0.2 | 0.110 ^{+0.009} _{-0.008} |
| Q | 12.07 MAX. | 0.475 MAX. |
| V | 0.25 ^{+0.10} _{-0.05} | 0.010 ^{+0.004} _{-0.003} |
| W | 2.54 (T.P.) | 0.100 (T.P.) |
| Y | 3.25 ± 0.2 | 0.128 ± 0.008 |

32 PIN PLASTIC ZIP (475mil)

NEC Cord:P32VF-100-475A



P32VF-100-475A

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 41.91 MAX. | 1.650 MAX |
| F | 0.5±0.10 | 0.020 ^{+0.004} _{-0.005} |
| G | 0.25 | 0.010 |
| H | 2.54 (T.P.) | 0.100 (T.P.) |
| I | 1.27 (T.P.) | 0.050 (T.P.) |
| J | 1.27 MAX. | 0.050 MAX. |
| K | 0.9 MIN. | 0.035 MIN. |
| M | 10.8 MAX. | 0.426 MAX. |
| N | 2.8±0.2 | 0.110 ^{+0.009} _{-0.008} |
| Q | 12.07 MAX. | 0.475 MAX. |
| V | 0.25 ^{+0.10} _{-0.05} | 0.010 ^{+0.004} _{-0.003} |
| W | 2.54 (T.P.) | 0.100 (T.P.) |
| Y | 3.25±0.2 | 0.128±0.008 |