SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7540 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7540 Group has a serial I/O, 8-bit timers, a 16-bit timer, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

FEATURES

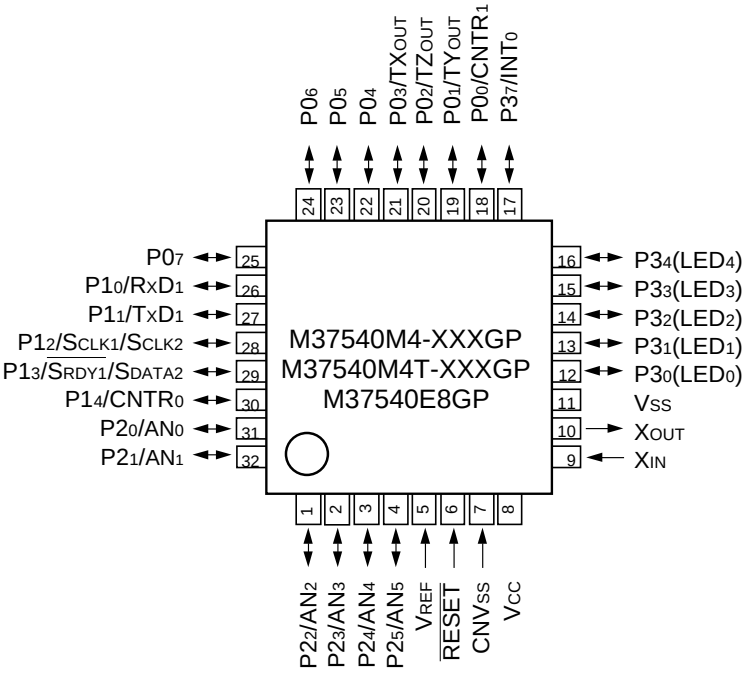
- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.34 µs
  (at 6 MHz oscillation frequency, double-speed mode for the shortest instruction)
- Memory size ROM ..... 16 K to 32 K bytes
  RAM ..... 512 to 768 bytes
- Programmable I/O ports ..... 29 (25 in 32-pin version)
- Interrupts ..... 15 sources, 15 vectors
  ..... (14 sources, 14 vectors for 32-pin version)
- Timers ..... 8-bit × 4
  ..... 16-bit × 1
- Serial I/O1 ..... 8-bit × 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit × 1 (Clock-synchronized)
- A-D converter ..... 10-bit × 8 channels
  ..... (6 channels for 32-pin version)
- Clock generating circuit ..... Built-in type
  (low-power dissipation by a ring oscillator enabled)
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  XIN oscillation frequency at ceramic oscillation, in double-speed mode
  At 6 MHz ..... 4.5 to 5.5 V
  XIN oscillation frequency at ceramic oscillation, in high-speed mode
  At 8 MHz ..... 4.0 to 5.5 V
  At 4 MHz ..... 2.4 to 5.5 V
  At 2 MHz ..... 2.2 to 5.5 V
  XIN oscillation frequency at RC oscillation
  At 4 MHz ..... 4.0 to 5.5 V
  At 2 MHz ..... 2.4 to 5.5 V
  At 1 MHz ..... 2.2 to 5.5 V
- Power dissipation
  Mask ROM version ..... 22.5 mW (standard)
  One Time PROM version ..... 30 mW (standard)
- Operating temperature range ..... –20 to 85 °C
  (–40 to 85 °C for extended operating temperature version)

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

Note: Serial I/O2 can be used in the following cases;
(1) Serial I/O1 is not used,
(2) Serial I/O1 is used as UART and BRG output divided by 16 is selected as the synchronized clock.

PIN CONFIGURATION (TOP VIEW)



Package type: 32P6U-A

Fig. 1 M37540M4-XXXGP, M37540E8GP, M37540M4T-XXXGP pin configuration

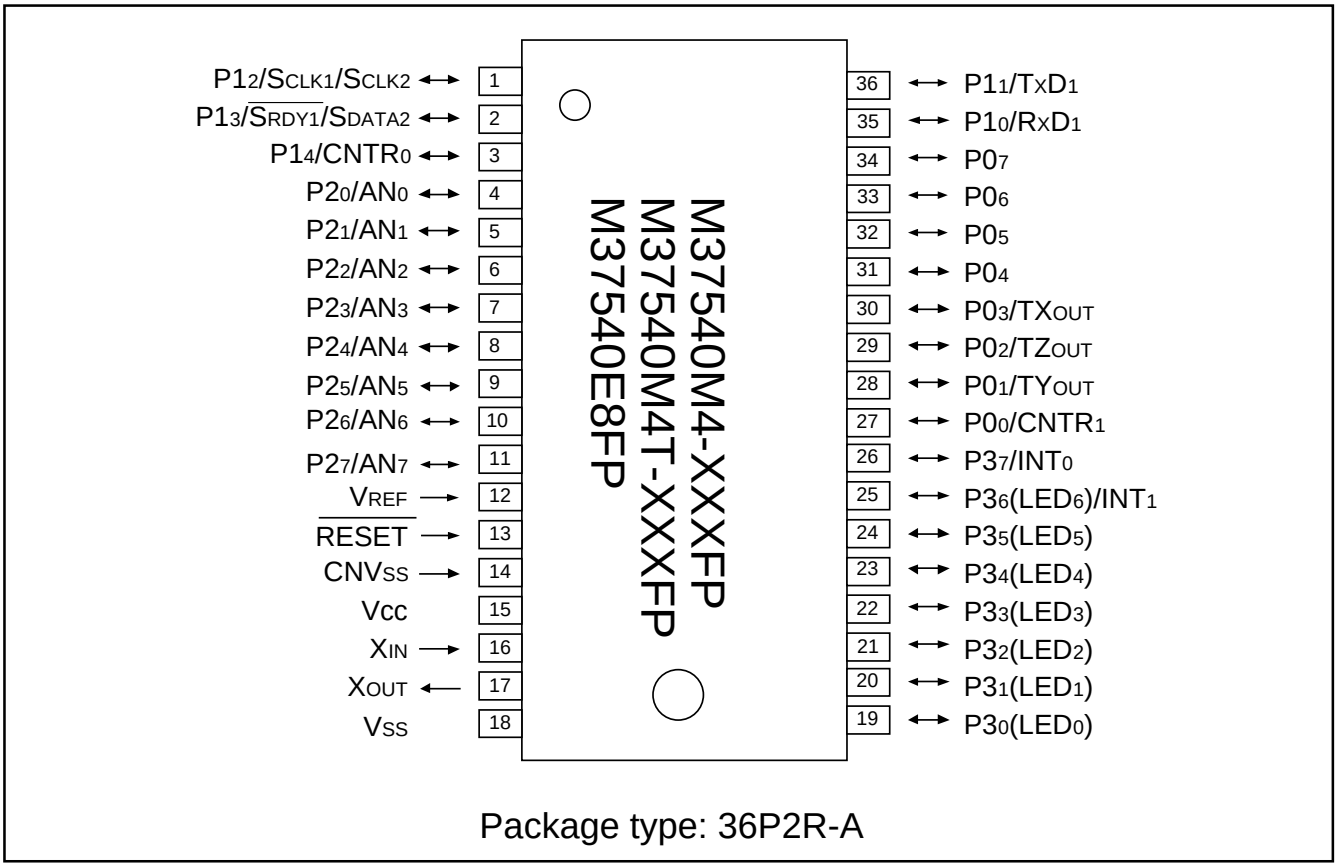


Fig. 2 M37540M4-XXXFP, M37540M4T-XXXFP, M37540E8FP pin configuration

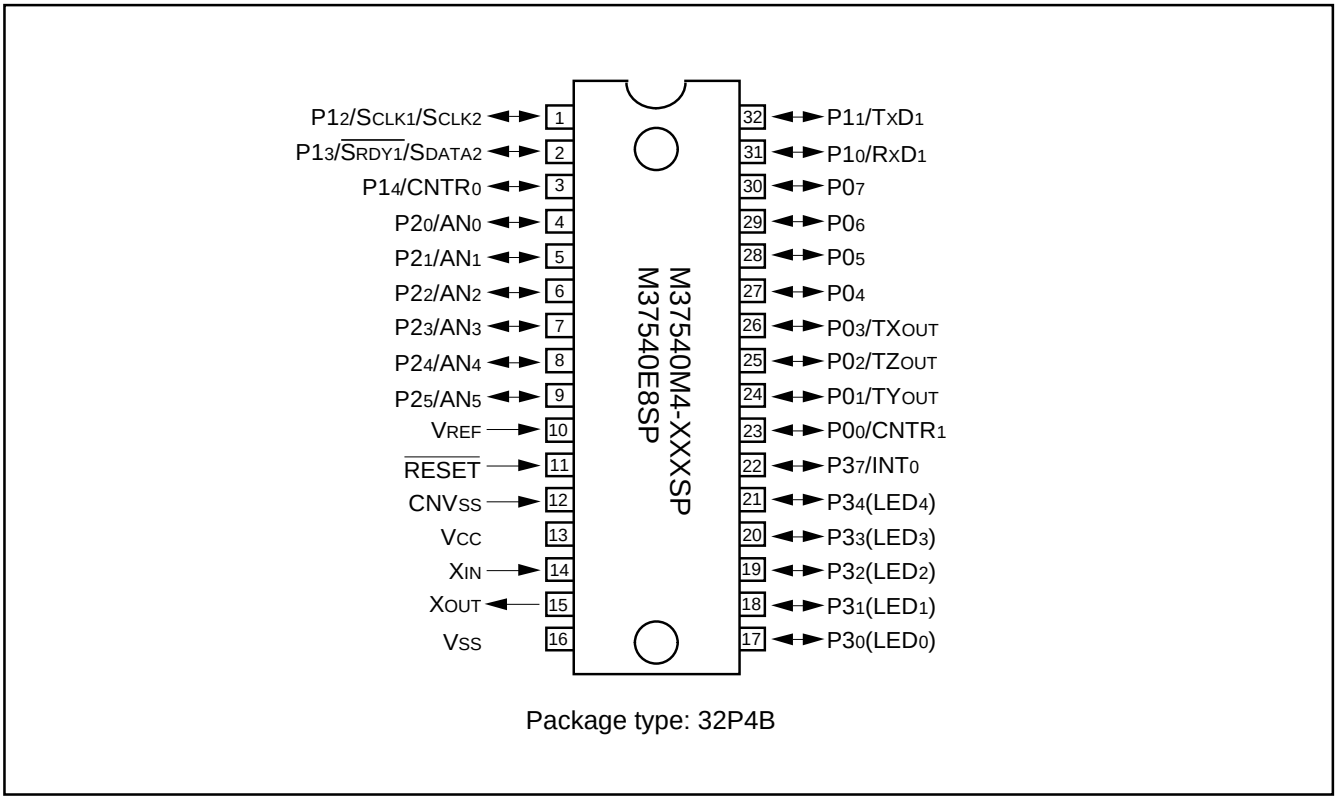
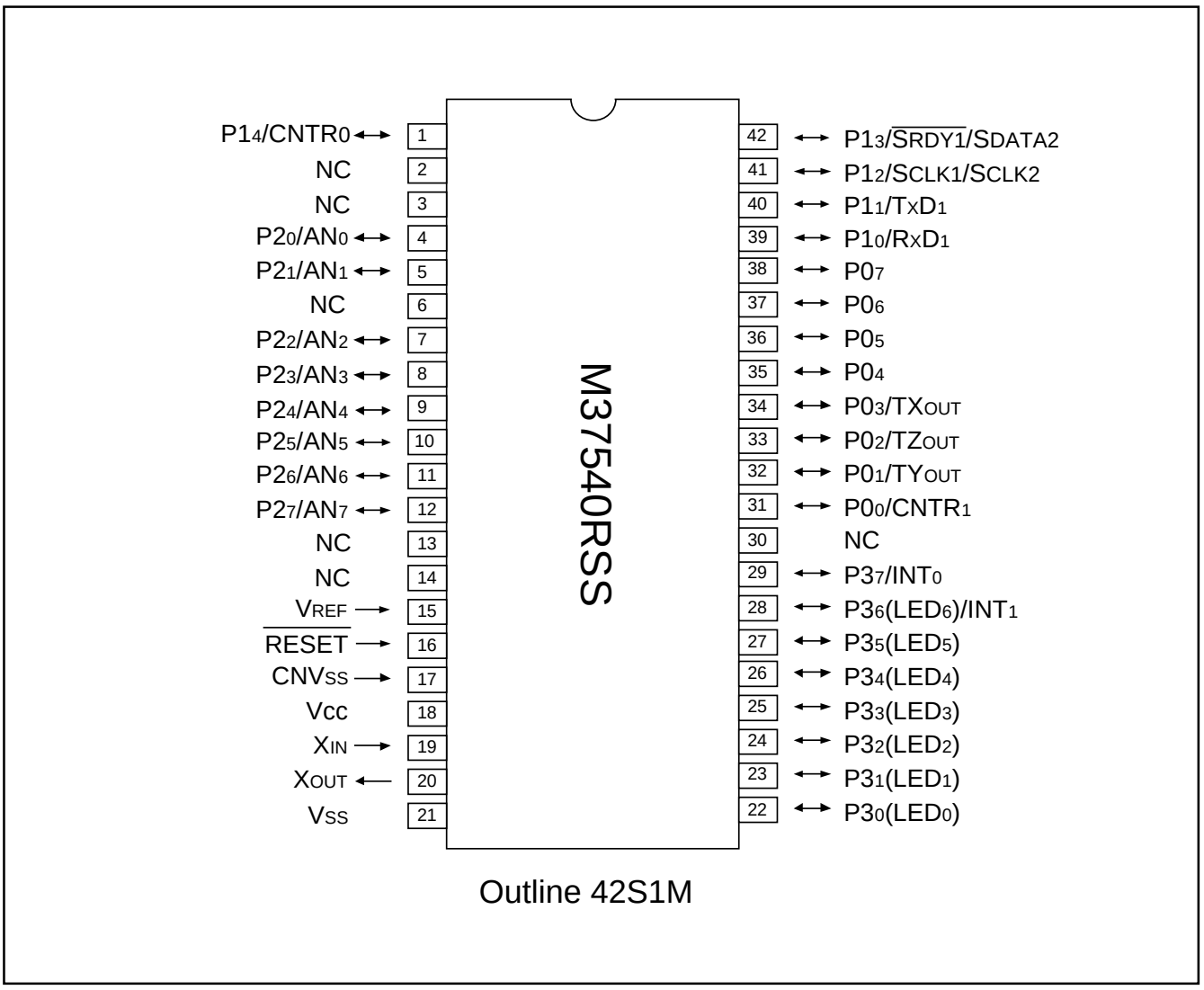


Fig. 3 M37540M4-XXXSP, M37540E8SP pin configuration



Outline 42S1M

Fig. 4 M37540RSS pin configuration

FUNCTIONAL BLOCK

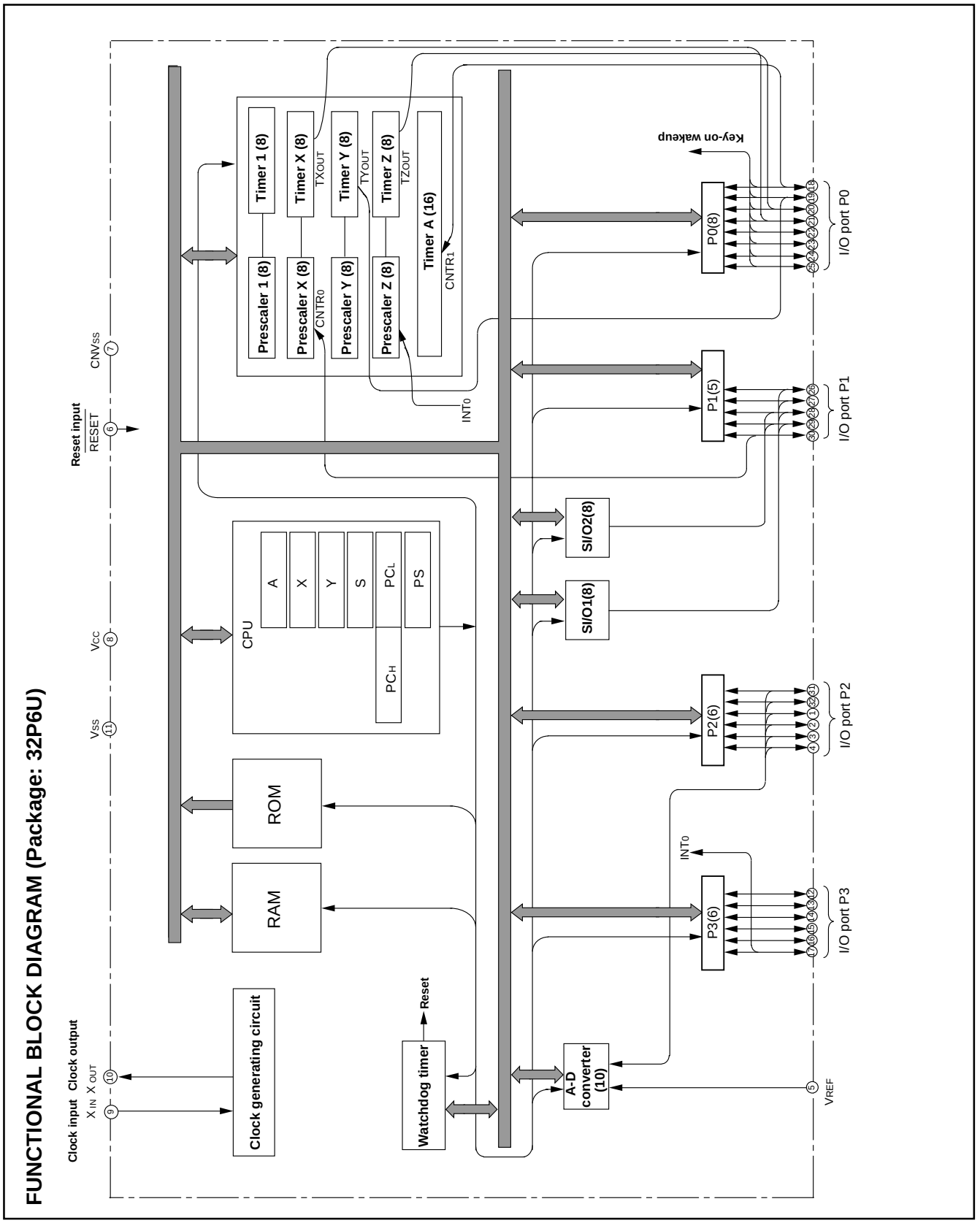


Fig. 5 Functional block diagram (32P6U package)

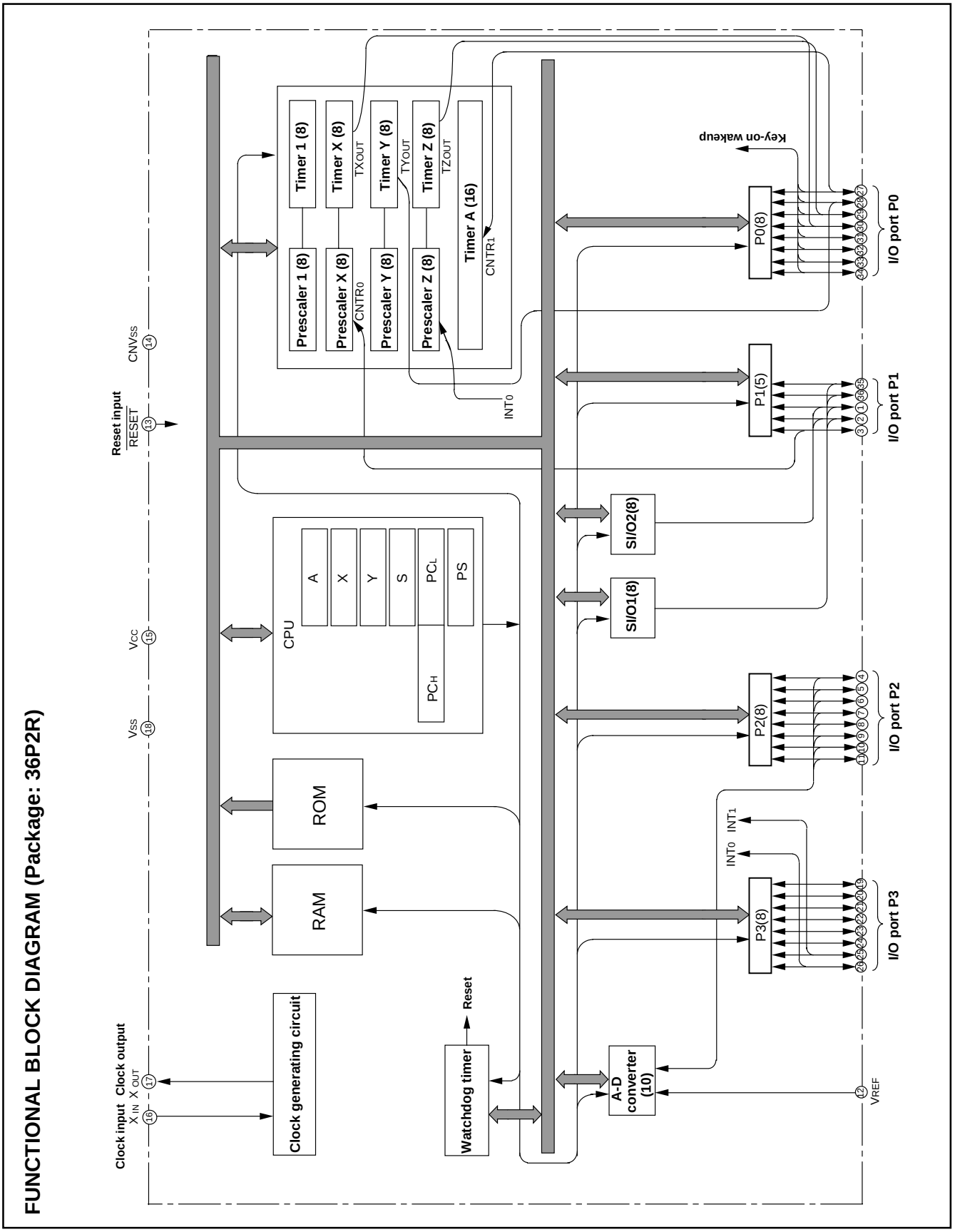


Fig. 6 Functional block diagram (36P2R package)

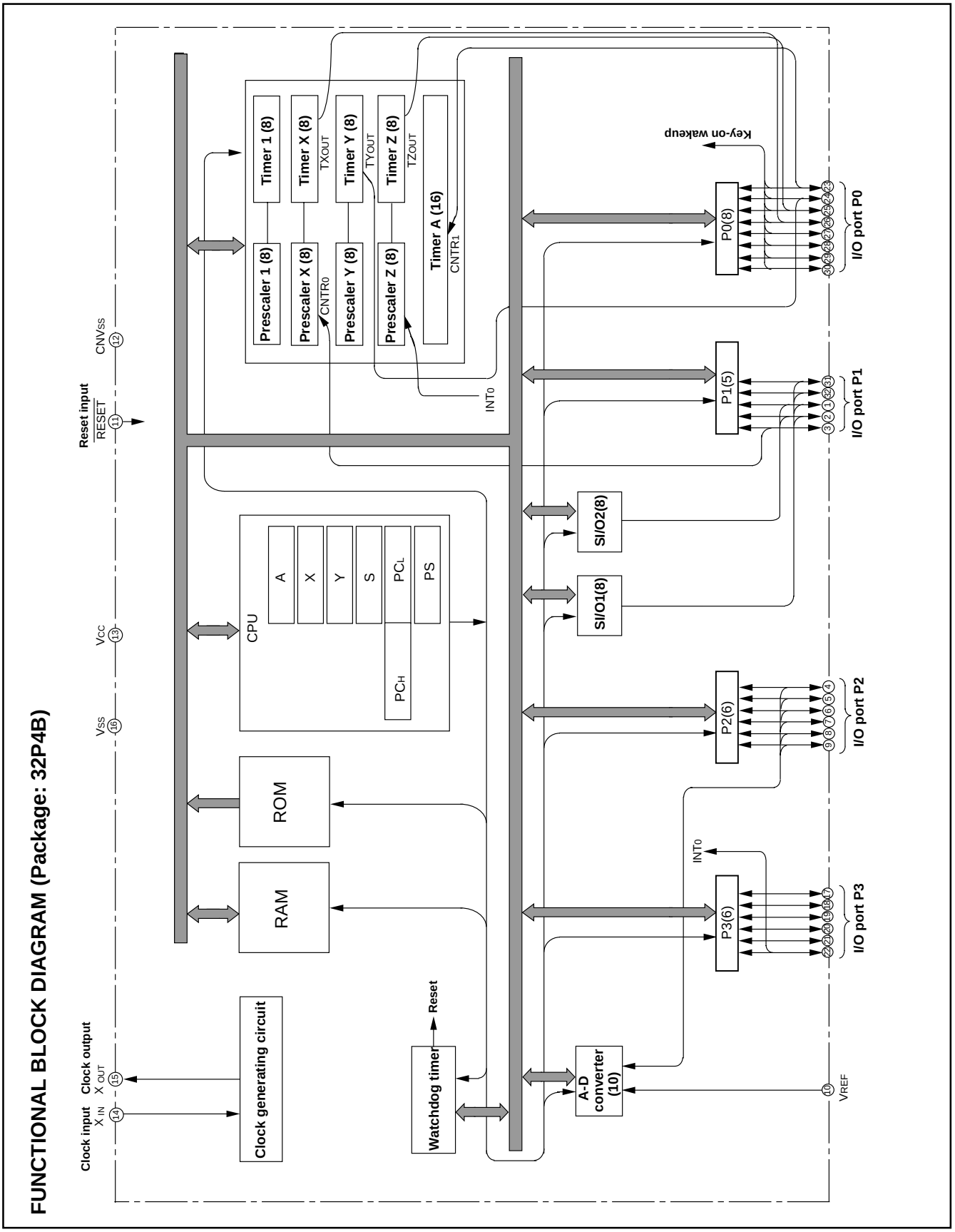


Fig. 7 Functional block diagram (32P4B package)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source (Note 1)	•Apply voltage of 2.2 to 5.5 V to Vcc, and 0 V to Vss.	
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active "L"	
XIN	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz crystal oscillator between the XIN and XOUT pins. •For using RC oscillator, short between the XIN and XOUT pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/CNTR1 P01/TYOUT P02/TZOUT P03/TXOUT P04–P07	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Key-input (key-on wake up interrupt input) pins • Timer Y, timer Z, timer X and timer A function pin
P10/RxD1 P11/TxD1	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for P10, P12 and P13	• Serial I/O1 function pin
P12/SCLK1/SCLK2 P13/$\overline{\text{SRDY1}}$/SDATA2			• Serial I/O1 function pin • Serial I/O2 function pin
P14/CNTR0			• Timer X function pin
P20/AN0–P27/AN7	I/O port P2 (Note 2)	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	• Input pins for A-D converter
P30–P35	I/O port P3 (Note 3)	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for P36 and P37). •CMOS 3-state output structure •P30 to P36 can output a large current for driving LED.	
P36/INT1 P37/INT0		•Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Interrupt input pins

Notes 1: VCC = 2.4 to 5.5 V for the extended operating temperature version.
2: P26/AN6 and P27/AN7 do not exist for the 32-pin version, so that Port P2 is a 6-bit I/O port.
3: P35 and P36/INT1 do not exist for the 32-pin version, so that Port P3 is a 6-bit I/O port.

GROUP EXPANSION

Mitsubishi plans to expand the 7540 group as follow:

Memory type

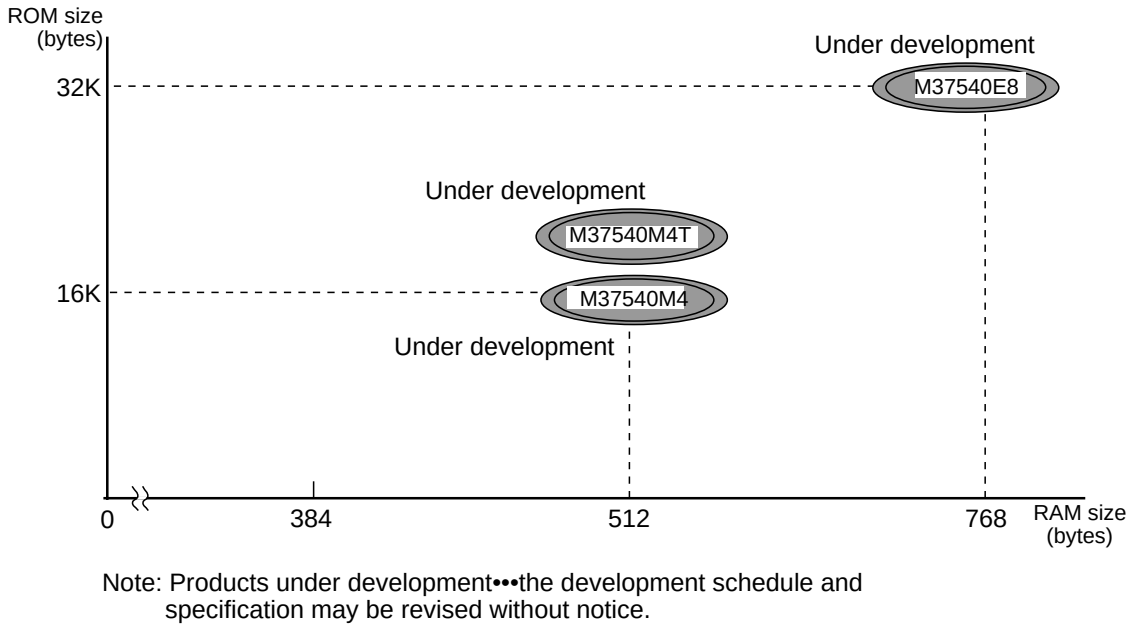
Support for Mask ROM version, One Time PROM version, and Emulator MCU.

Memory size

ROM/PROM size ..... 16 K to 32 K bytes
RAM size ..... 512 to 768 bytes

Package

32P4B ..... 32-pin shrink plastic molded DIP
32P6U-A ..... 0.8 mm-pitch plastic molded LQFP
36P2R-A ..... 0.8 mm-pitch plastic molded SSOP
42S1M ..... 42-pin shrink ceramic PIGGY BACK



Note: Products under development•••the development schedule and specification may be revised without notice.

Fig. 8 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37540M4-XXXSP	16384	512	32P4B	Mask ROM version
M37540M4-XXXFP	(16254)		36P2R-A	Mask ROM version
M37540M4T-XXXFP				Mask ROM version (extended operating temperature version)
M37540M4-XXXGP			32P6U-A	Mask ROM version
M37540M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37540E8SP	32768	768	32P4B	One Time PROM version (blank)
M37540E8FP	(32638)		36P2R-A	One Time PROM version (blank)
M37540E8GP			32P6U-A	One Time PROM version (blank)
M37540RSS	————	768	42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The MCU uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the SERIES 740 <SOFTWARE> USER'S MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

This instruction cannot be used while CPU operates by a ring oscillator.

Accumulator (A)

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

Index register X (X), Index register Y (Y)

Both index register X and index register Y are 8-bit registers. In the index addressing modes, the value of the OPERAND is added to the contents of register X or register Y and specifies the real address.

When the T flag in the processor status register is set to "1", the value contained in index register X becomes the address for the second OPERAND.

Stack pointer (S)

The stack pointer is an 8-bit register used during subroutine calls and interrupts. The stack is used to store the current address data and processor status when branching to subroutines or interrupt routines.

The lower eight bits of the stack address are determined by the contents of the stack pointer. The upper eight bits of the stack address are determined by the Stack Page Selection Bit. If the Stack Page Selection Bit is "0", then the RAM in the zero page is used as the stack area. If the Stack Page Selection Bit is "1", then RAM in page 1 is used as the stack area.

The Stack Page Selection Bit is located in the SFR area in the zero page. Note that the initial value of the Stack Page Selection Bit varies with each microcomputer type. Also some microcomputer types have no Stack Page Selection Bit and the upper eight bits of the stack address are fixed. The operations of pushing register contents onto the stack and popping them from the stack are shown in Fig. 9.

Program counter (PC)

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

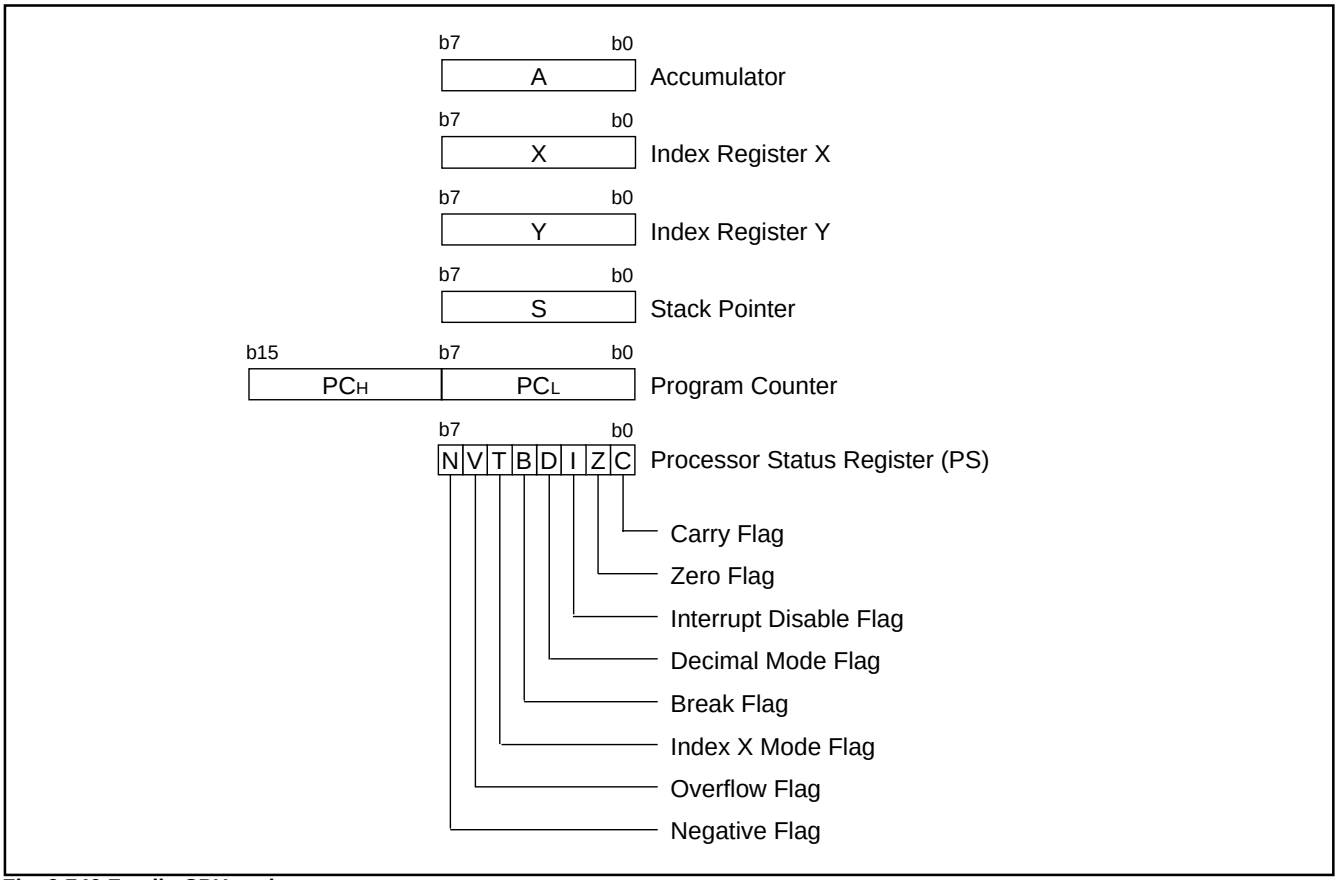


Fig. 9 740 Family CPU register structure

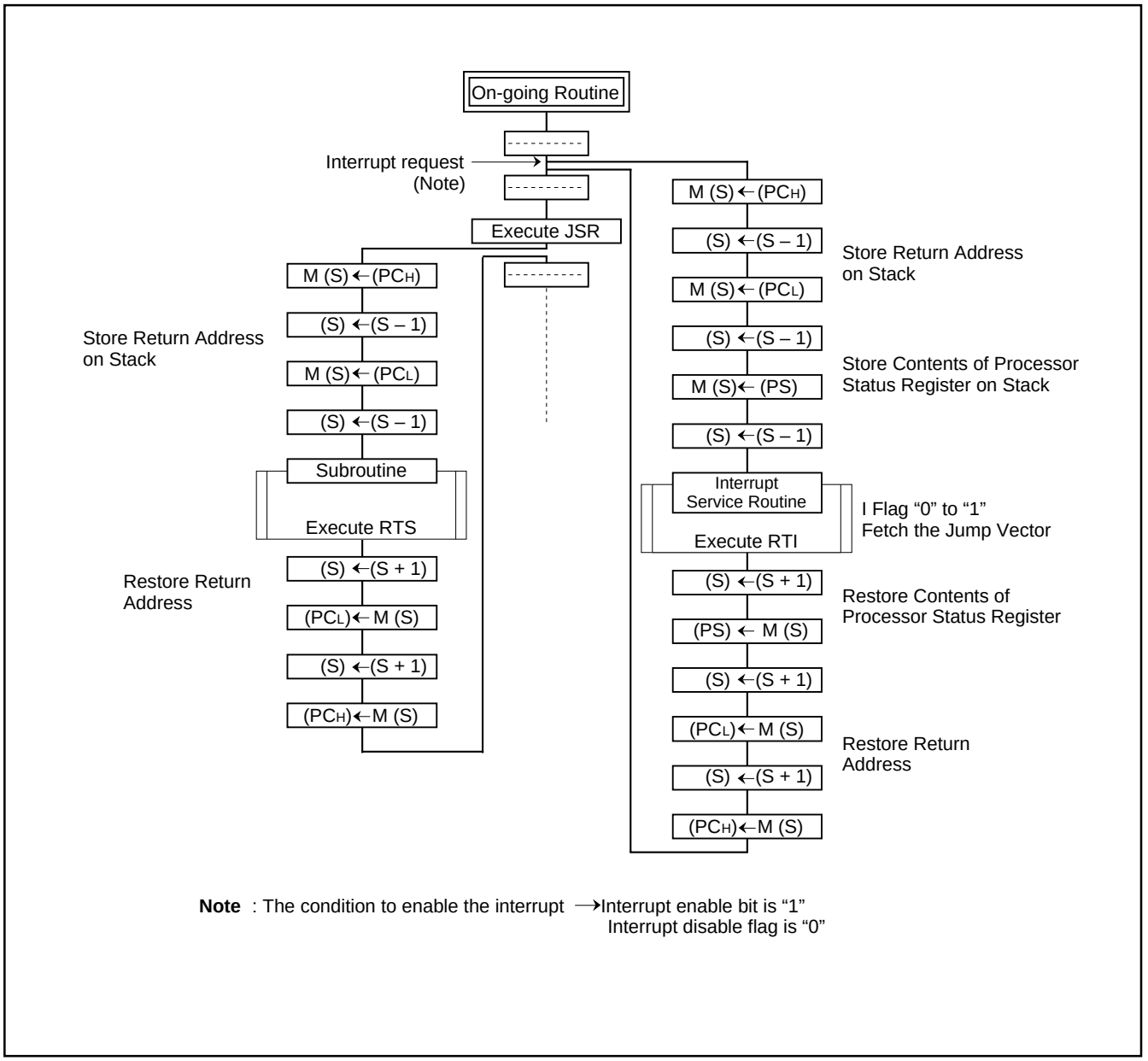


Fig. 10 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

Processor status register (PS)

The processor status register is an 8-bit register consisting of flags which indicate the status of the processor after an arithmetic operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.
After reset, the Interrupt disable (I) flag is set to "1", but all other flags are undefined. Since the Index X mode (T) and Decimal mode (D) flags directly affect arithmetic operations, they should be initialized in the beginning of a program.

(1) Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

(2) Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

(3) Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction. Interrupts are disabled when the I flag is "1".
When an interrupt occurs, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is serviced.

(4) Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".
Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

(5) Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1". The saved processor status is the only place where the break flag is ever set.

(6) Index X mode flag (T)
When the T flag is "0", arithmetic operations are performed between accumulator and memory, e.g. the results of an operation between two memory locations is stored in the accumulator. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations, i.e. between memory and memory, memory and I/O, and I/O and I/O. In this case, the result of an arithmetic operation performed on data in memory location 1 and memory location 2 is stored in memory location 1. The address of memory location 1 is specified by index register X, and the address of memory location 2 is specified by normal addressing modes.

(7) Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

(8) Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

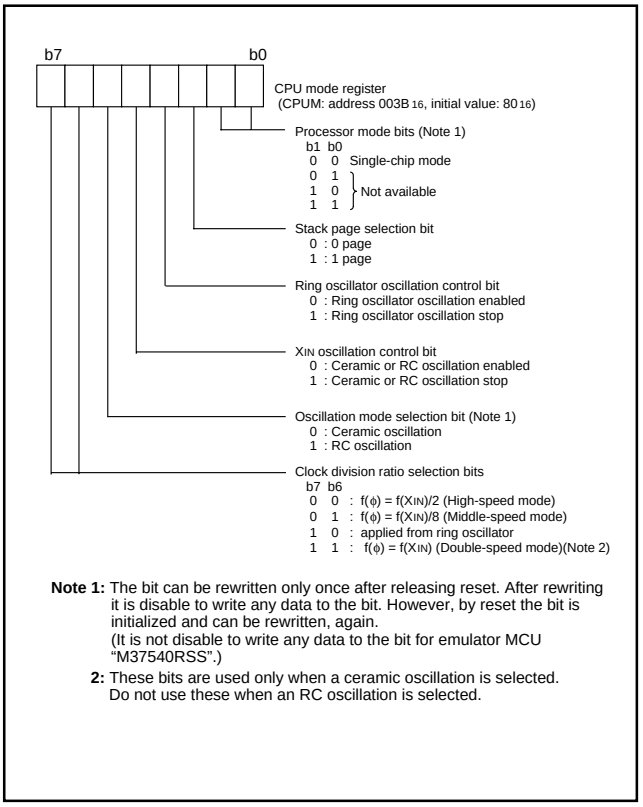
	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit. This register is allocated at address 003B16.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.



Note 1: The bit can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. However, by reset the bit is initialized and can be rewritten, again.
(It is not disable to write any data to the bit for emulator MCU "M37540RSS".)

2: These bits are used only when a ceramic oscillation is selected. Do not use these when an RC oscillation is selected.

Fig. 11 Structure of CPU mode register

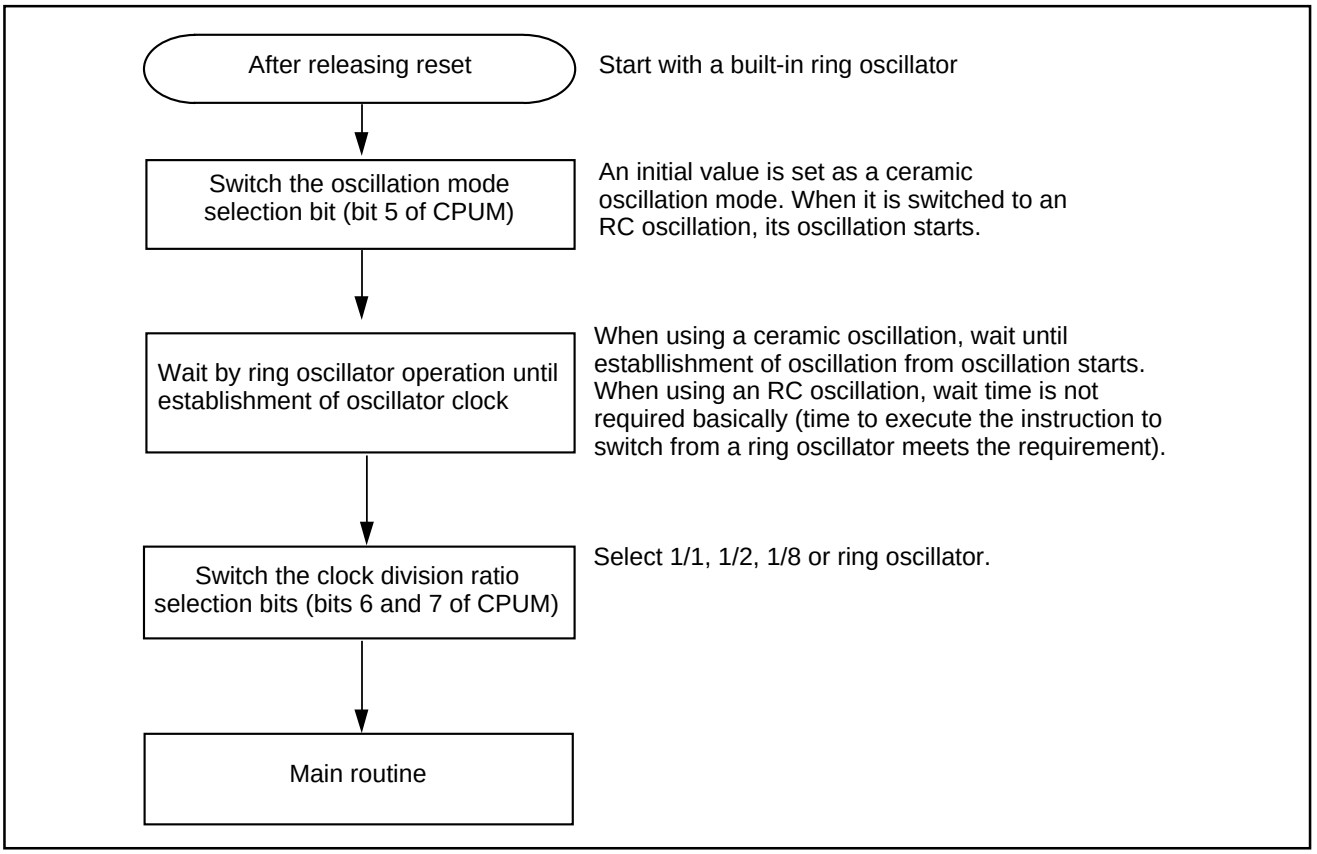


Fig. 12 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

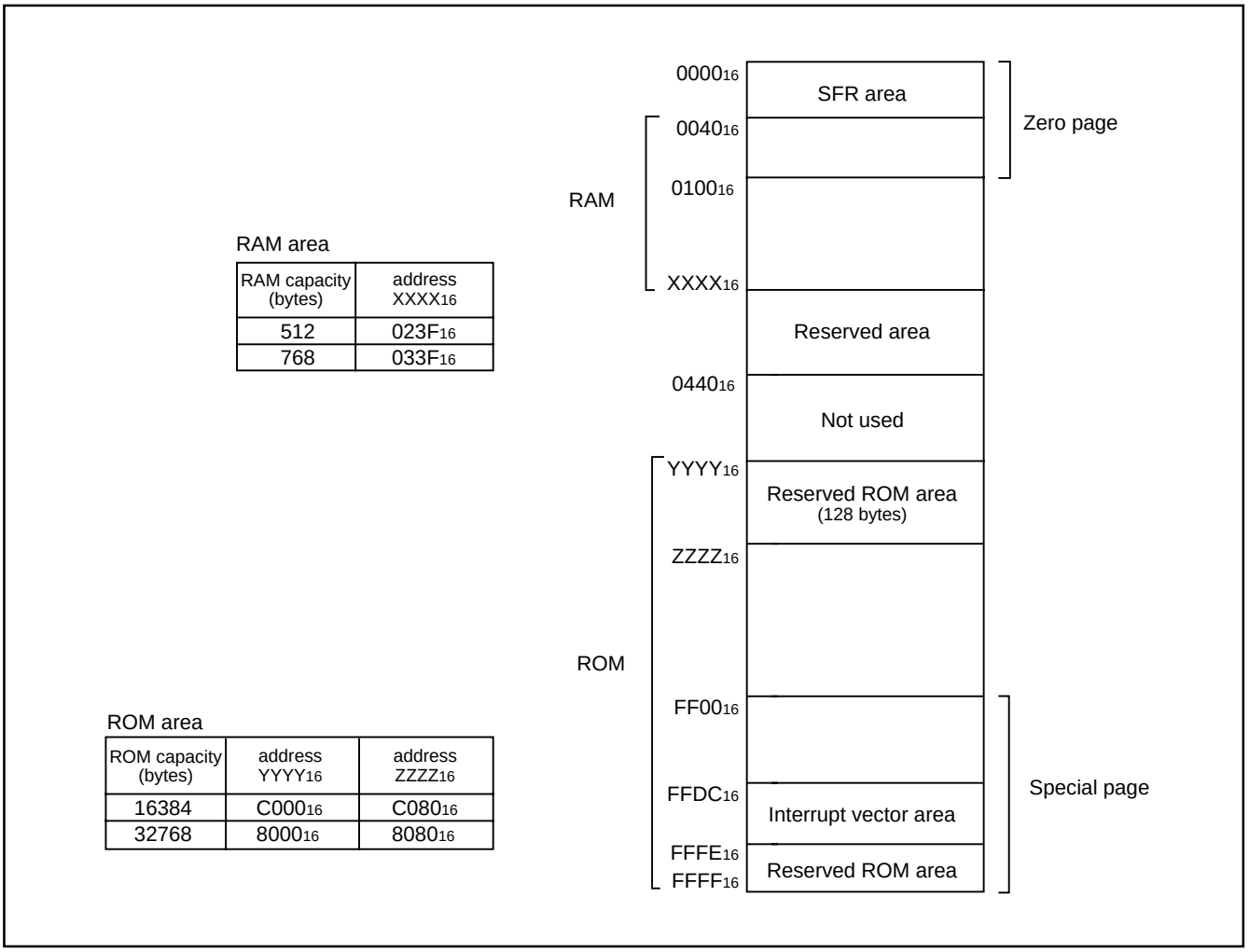
Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.



RAM area

RAM capacity (bytes)	address XXXX₁₆
512	023F₁₆
768	033F₁₆

ROM area

ROM capacity (bytes)	address YYYY₁₆	address ZZZZ₁₆
16384	C000₁₆	C080₁₆
32768	8000₁₆	8080₁₆

Fig. 13 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer Y, Z mode register (TYZM)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Prescaler Y (PREY)
0002_{16}	Port P1 (P1)	0022_{16}	Timer Y secondary (TYS)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer Y primary (TYP)
0004_{16}	Port P2 (P2)	0024_{16}	Timer Y, Z waveform output control register (PUM)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Prescaler Z (PREZ)
0006_{16}	Port P3 (P3)	0026_{16}	Timer Z secondary (TZS)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Z primary (TZP)
0008_{16}		0028_{16}	Prescaler 1 (PRE1)
0009_{16}		0029_{16}	Timer 1 (T1)
$000A_{16}$		$002A_{16}$	One-shot start register (ONS)
$000B_{16}$		$002B_{16}$	Timer X mode register (TXM)
$000C_{16}$		$002C_{16}$	Prescaler X (PREX)
$000D_{16}$		$002D_{16}$	Timer X (TX)
$000E_{16}$		$002E_{16}$	Timer count source set register (TCSS)
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}		0031_{16}	Serial I/O2 register (SIO2)
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A-D control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A-D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Timer A mode register (TAM)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Timer A (low-order) (TAL)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Timer A (high-order) (TAH)	$003F_{16}$	Interrupt control register 2 (ICON2)

Note : Do not access to the SFR area including nothing.

Fig. 14 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port.

When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

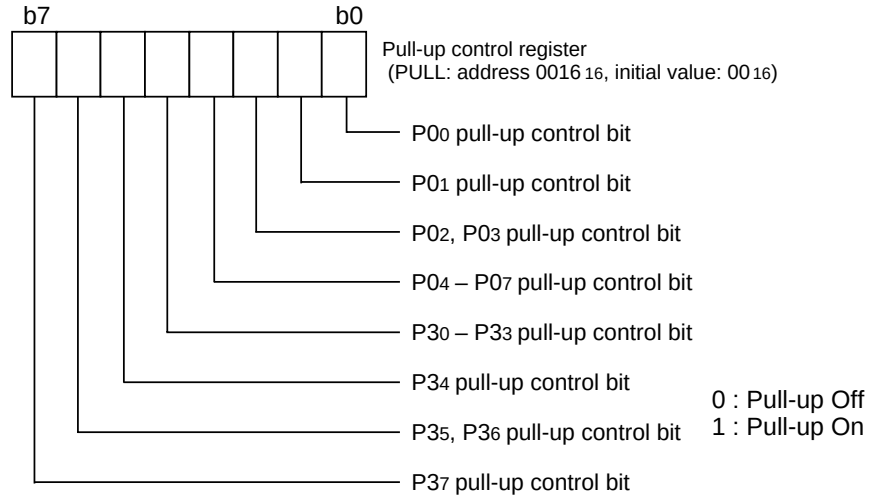
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control register] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

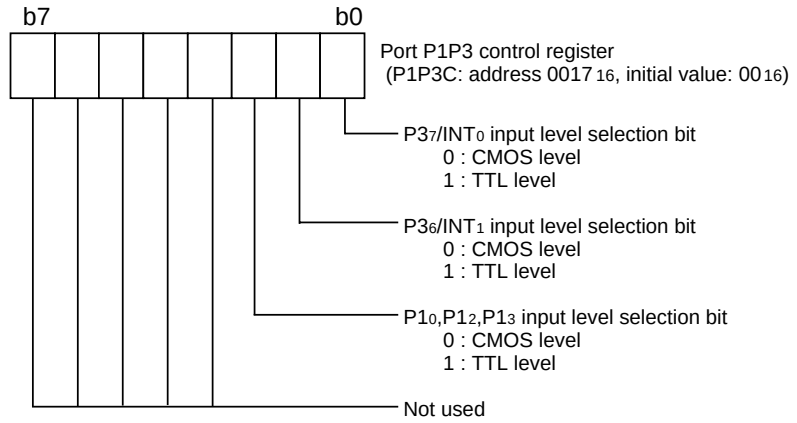
[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ by program.



Note 1: Pins set to output ports are disconnected from pull-up control.
2: Set the $P3_5$, $P3_6$ pull-up control bit to "1" (initial value: "0") for 32-pin version.

Fig. 15 Structure of pull-up control register



Note: Keep setting the $P3_6$/INT_1 input level selection bit to "0" (initial value) for 32-pin version.

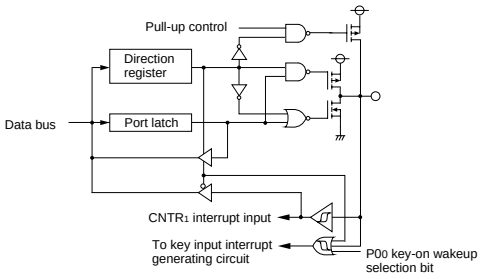
Fig. 16 Structure of port P1P3 control register

Table 5 I/O port function table

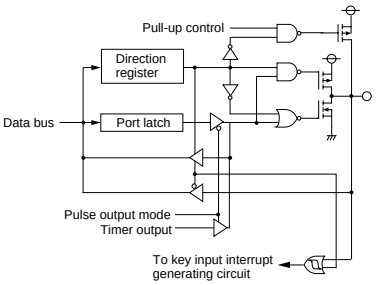
Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
P0$_0$/CNTR$_1$ P0$_1$/TY$_{OUT}$ P0$_2$/TZ$_{OUT}$ P0$_3$/TX$_{OUT}$ P0$_4$–P0$_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (Note 1)	Key input interrupt Timer X function output Timer Y function output Timer Z function output Timer A function input	Pull-up control register Timer Y mode register Timer Z mode register Timer X mode register Timer Y,Z waveform output control register Timer A mode register	(1) (2) (3) (4)
P1$_0$/RxD$_1$ P1$_1$/TxD$_1$	I/O port P1			Serial I/O1 function input/output	Serial I/O1 control register	(5) (6)
P1$_2$/S$_{CLK1}$/S$_{CLK2}$ P1$_3$/S$_{RDY1}$/S$_{DATA2}$				Serial I/O2 function input/output	Serial I/O1 control register Serial I/O2 control register	(7) (8)
P1$_4$/CNTR$_0$				Timer X function input/output	Timer X mode register	(9)
P2$_0$/AN$_0$– P2$_7$/AN$_7$	I/O port P2 (Note 2)			A-D conversion input	A-D control register	(10)
P3$_0$–P3$_5$	I/O port P3					(11)
P3$_6$/INT$_1$ P3$_7$/INT$_0$	(Note 3)			External interrupt input	Interrupt edge selection register	(12)

Notes 1: Ports P1$_0$, P1$_2$, P1$_3$, P3$_6$, and P3$_7$ are CMOS/TTL level.
2: P2$_6$/AN$_6$ and P2$_7$/AN$_7$ do not exist for the 32-pin version.
3: P3$_5$ and P3$_6$/INT$_1$ do not exist for the 32-pin version.

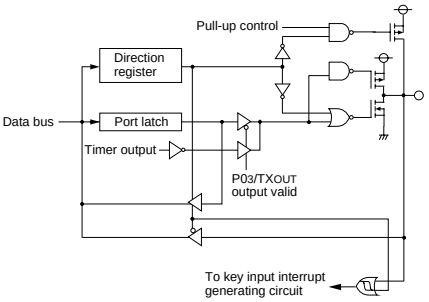
(1)Port $P0_0$



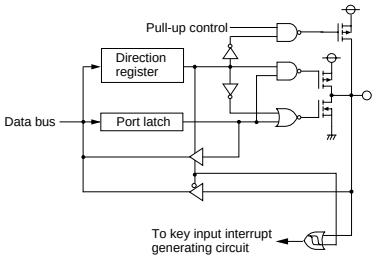
(2)Ports $P0_1$, $P0_2$



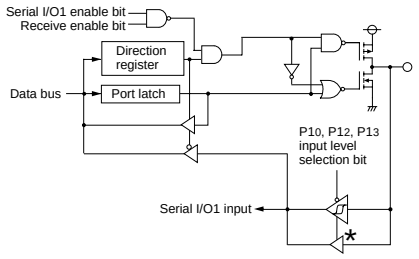
(3)Port $P0_3$



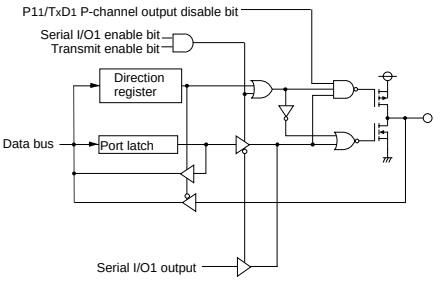
(4)Ports $P0_4$–$P0_7$



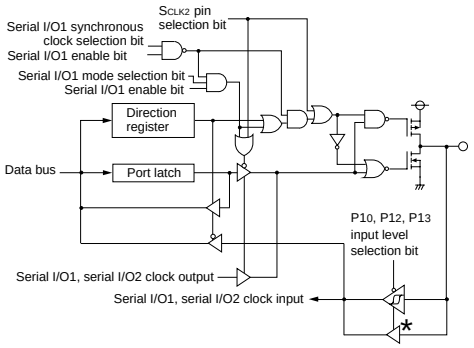
(5)Port $P1_0$



(6)Port $P1_1$



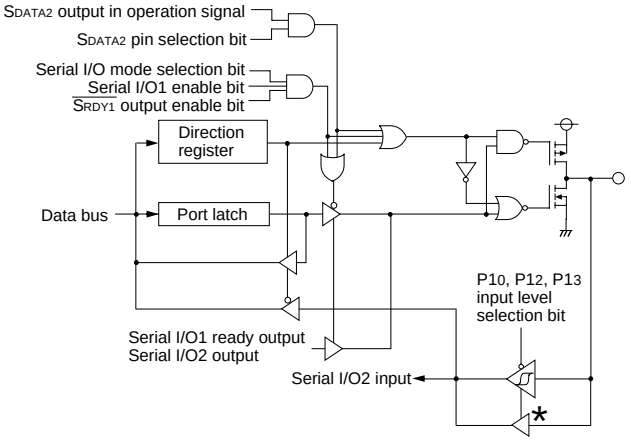
(7)Port $P1_2$



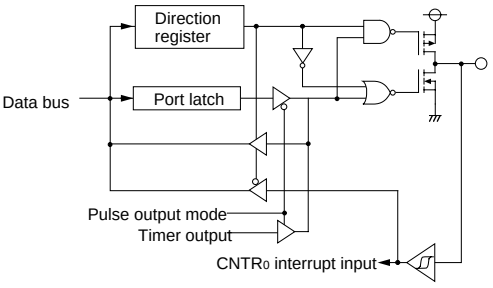
* $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register. When the TTL level is selected, there is no hysteresis characteristics.

Fig. 17 Block diagram of ports (1)

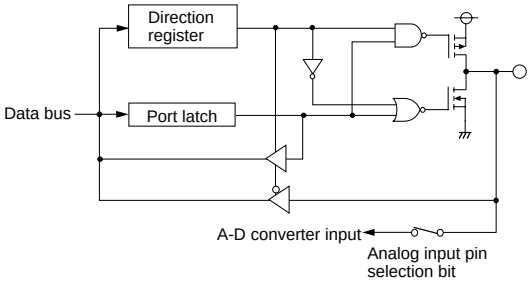
(8) Port P13



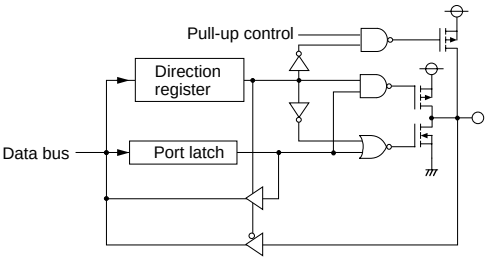
(9) Port P14



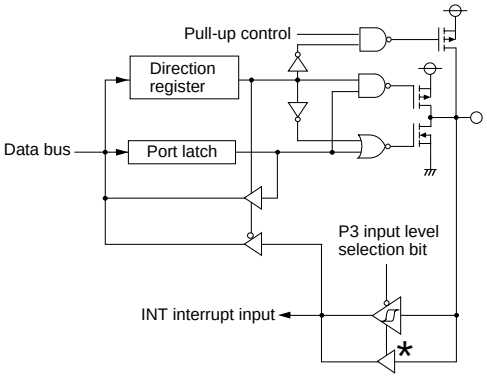
(10) Ports P20–P27



(11) Ports P30–P35



(12) Ports P36, P37



* P10, P12, P13, P36, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.
When the TTL level is selected, there is no hysteresis characteristics.

Fig. 18 Block diagram of ports (2)

Interrupts

Interrupts occur by 15 different sources : 5 external sources, 9 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to “1” and the interrupt disable flag is set to “0”, an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set.

The interrupt enable bit can be set and cleared by program.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT_0, INT_1,$CNTR_0$,$CNTR_1$) is set, the interrupt request bit may be set to “1”.

Related register: Interrupt edge selection register (address $003A_{16}$)

When not requiring the interrupt occurrence synchronized with this setting, take following sequence:

1. Clear the interrupt enable bit to “0” (disabled).
2. Set the interrupt edge selection bit to “1”.
3. Clear the interrupt request bit to “0” after 1 or more instructions have been executed.
4. Set the interrupt enable bit to “1” (enabled).

Table 6 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O1 receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid only when serial I/O1 is selected
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1 (Note 3)	5	$FFF5_{16}$	$FFF4_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Key-on wake-up	6	$FFF3_{16}$	$FFF2_{16}$	At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
$CNTR_0$	7	$FFF1_{16}$	$FFF0_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer X	9	$FFED_{16}$	$FFEC_{16}$	At timer X underflow	
Timer Y	10	$FFEB_{16}$	$FFEA_{16}$	At timer Y underflow	
Timer Z	11	$FFE9_{16}$	$FFE8_{16}$	At timer Z underflow	
Timer A	12	$FFE7_{16}$	$FFE6_{16}$	At timer A underflow	
Serial I/O2	13	$FFE5_{16}$	$FFE4_{16}$	At completion of transmit/receive shift	
A-D conversion	14	$FFE3_{16}$	$FFE2_{16}$	At completion of A-D conversion	
Timer 1	15	$FFE1_{16}$	$FFE0_{16}$	At timer 1 underflow	STP release timer underflow
Reserved area	16	$FFDF_{16}$	$FFDE_{16}$	Not available	
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.
3: It is an interrupt which can use only for 36 pin version.

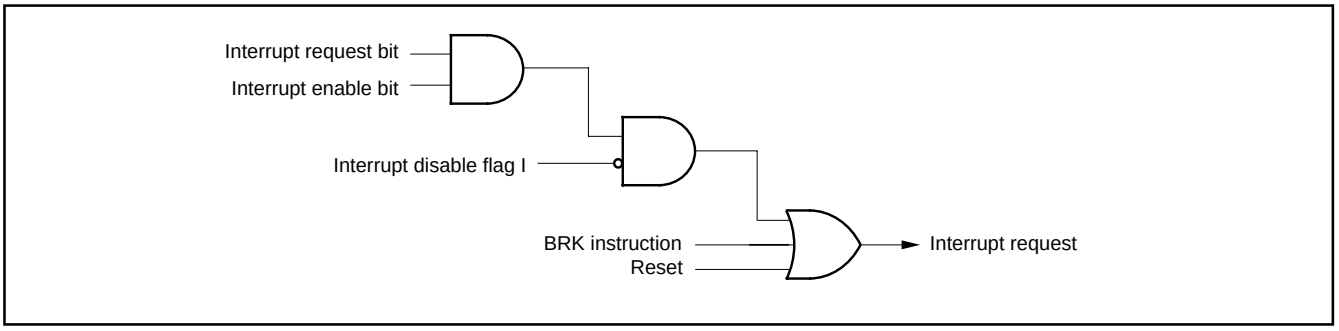


Fig. 19 Interrupt control

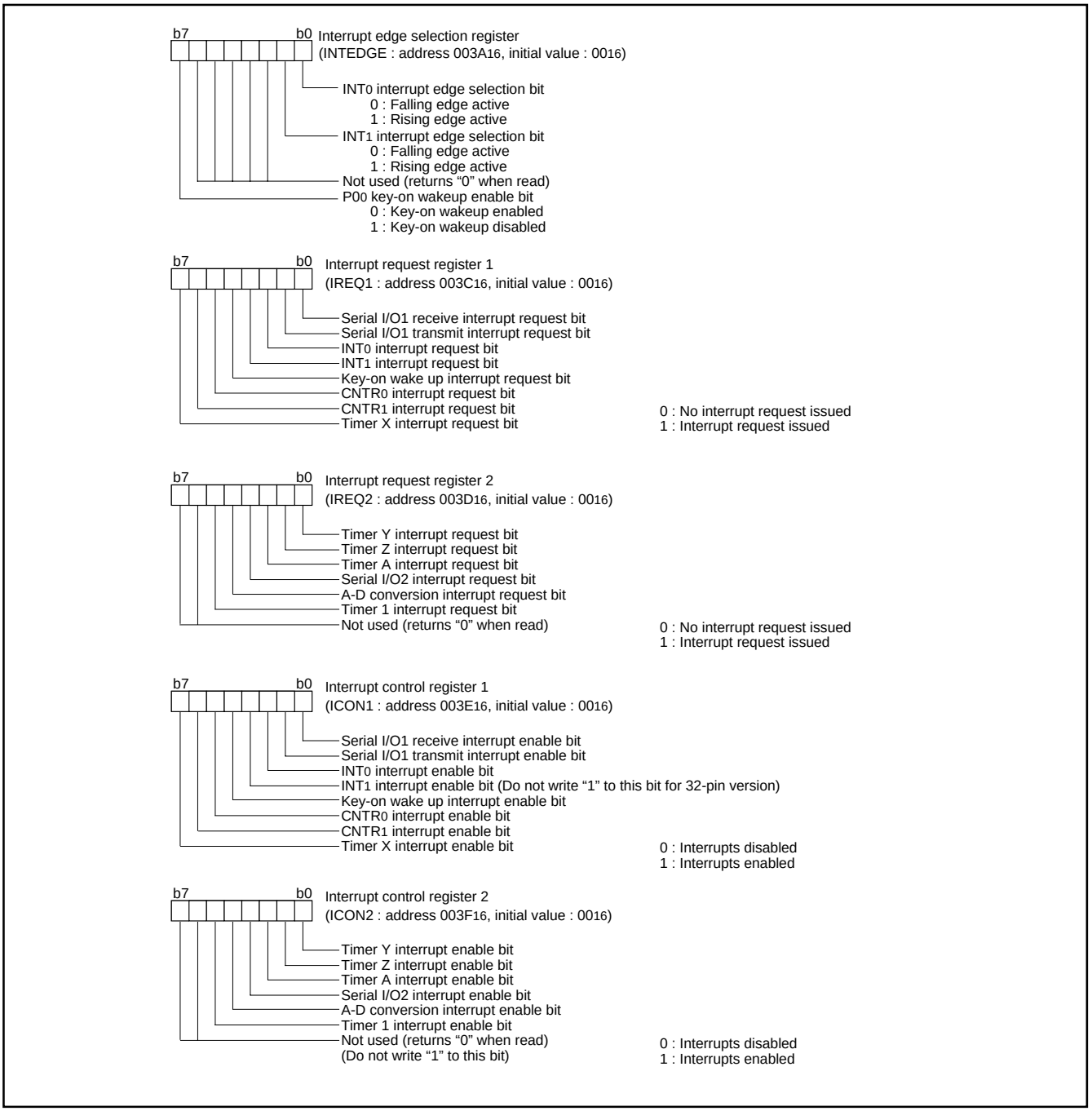


Fig. 20 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying "L" level to any pin of port P0 that has been set to input mode.
In other words, it is generated when the AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 21, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P00 to P03 as input ports.

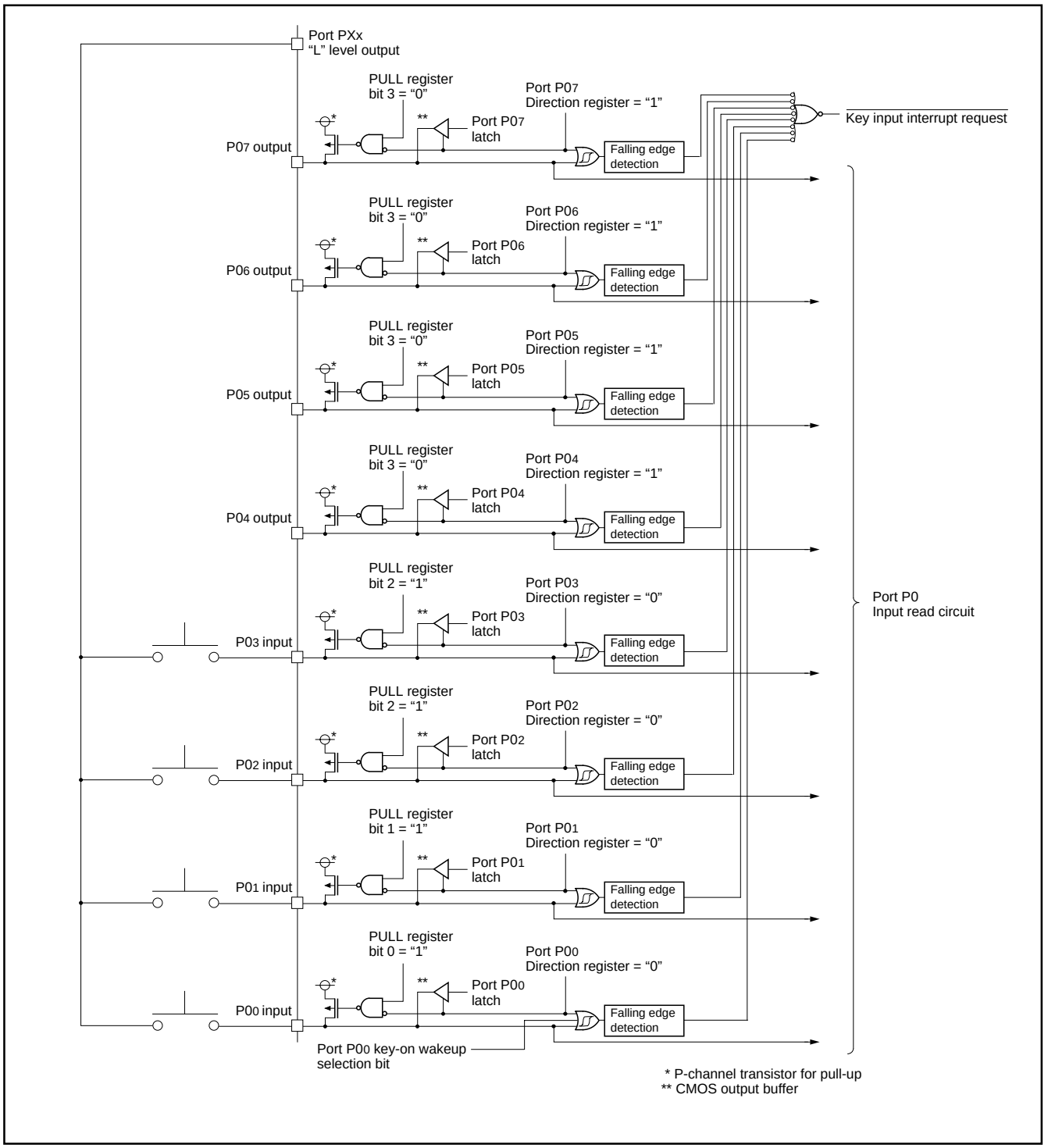


Fig. 21 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7540 Group has 5 timers: timer 1, timer A, timer X, timer Y and timer Z.

The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.

All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

●Timer 1

Timer 1 is an 8-bit timer and counts the prescaler output.

When Timer 1 underflows, the timer 1 interrupt request bit is set to "1".

Prescaler 1 is an 8-bit prescaler and counts the signal which is the oscillation frequency divided by 16.

Prescaler 1 and Timer 1 have the prescaler 1 latch and the timer 1 latch to retain the reload value, respectively. The value of prescaler 1 latch is set to Prescaler 1 when Prescaler 1 underflows.The value of timer 1 latch is set to Timer 1 when Timer 1 underflows.

When writing to Prescaler 1 (PRE1) is executed, the value is written to both the prescaler 1 latch and Prescaler 1.

When writing to Timer 1 (T1) is executed, the value is written to both the timer 1 latch and Timer 1.

When reading from Prescaler 1 (PRE1) and Timer 1 (T1) is executed, each count value is read out.

Timer 1 always operates in the timer mode.

Prescaler 1 counts the selected count source. Each time the count clock is input, the contents of Prescaler 1 is decremented by 1. When the contents of Prescaler 1 reach "00_{16}", an underflow occurs at the next count clock, and the prescaler 1 latch is reloaded into Prescaler 1 and count continues. The division ratio of Prescaler 1 is 1/(n+1) provided that the value of Prescaler 1 is n.

The contents of Timer 1 is decremented by 1 each time the underflow signal of Prescaler 1 is input. When the contents of Timer 1 reach "00_{16}", an underflow occurs at the next count clock, and the timer 1 latch is reloaded into Timer 1 and count continues. The division ratio of Timer 1 is 1/(m+1) provided that the value of Timer 1 is m. Accordingly, the division ratio of Prescaler 1 and Timer 1 is 1/((n+1)×(m+1)) provided that the value of Prescaler 1 is n and the value of Timer 1 is m.

Timer 1 cannot stop counting by software.

●Timer A

Timer A is a 16-bit timer and counts the signal which is the oscillation frequency divided by 16. When Timer A underflows, the timer A interrupt request bit is set to "1".
Timer A consists of the low-order of Timer A (TAL) and the high-order of Timer A (TAH).
Timer A has the timer A latch to retain the reload value. The value of timer A latch is set to Timer A at the timing shown below.
• When Timer A undeflows.
• When an active edge is input from CNTR1 pin (valid only when period measurement mode and pulse width HL continuously measurement mode).
When writing to both the low-order of Timer A (TAL) and the high-order of Timer A (TAH) is executed, the value is written to both the timer A latch and Timer A.
When reading from TAL and TAH is executed, the following values are read out according to the operating mode.
• In timer mode, event counter mode:
The count value of Timer A is read out.
• In period measurement mode, pulse width HL continuously measurement mode:
The measured value is read out.

Be sure to write to/read out the low-order of Timer A (TAL) and the high-order of Timer A (TAH) in the following order;
Read
Read the high-order of Timer A (TAH) first, and the low-order of Timer A (TAL) next and be sure to read out both TAH and TAL.
Write
Write to the low-order of Timer A (TAL) first, and the high-order of Timer A (TAH) next and be sure to write to both TAL and TAH.

Timer A can be selected in one of 4 operating modes by setting the timer A mode register.

(1) Timer mode

Timer A counts f(XIN)/16. Each time the count clock is input, the contents of Timer A is decremented by 1. When the contents of Timer A reach "0000$_{16}$", an underflow occurs at the next count clock, and the timer A latch is reloaded into Timer A. The division ratio of Timer A is 1/(n+1) provided that the value of Timer A is n.

(2) Period measurement mode

In the period measurement mode, the pulse period input from the P00/CNTR1 pin is measured.
CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input singal. Simultaneousuly, the value in the timer A latch is reloaded inTimer A and count continues. The active edge of CNTR1 pin input signal can be selected from rising or falling by the CNTR1 active edge switch bit .The count value when trigger input from CNTR1 pin is accepted is retained until Timer A is read once.

(3) Event counter mode

Timer A counts signals input from the P00/CNTR1 pin.
Except for this, the operation in event counter mode is the same as in timer mode.
The active edge of CNTR1 pin input signal can be selected from rising or falling by the CNTR1 active edge switch bit .

(4) Pulse width HL continuously measurement mode

In the pulse width HL continuously measurement mode, the pulse width ("H" and "L" levels) input to the P00/CNTR1 pin is measured. CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode.
The count value when trigger input from the CNTR1 pin is accepted is retained until Timer A is read once.

Timer A can stop counting by setting "1" to the timer A count stop bit in any mode.
Also, when Timer A underflows, the timer A interrupt request bit is set to "1".

Note on Timer A is described below;

■ Note on Timer A

CNTR1 interrupt active edge selection
CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit.
When this bit is "0", the CNTR1 interrupt request bit is set to "1" at the falling edge of the CNTR1 pin input signal. When this bit is "1", the CNTR1 interrupt request bit is set to "1" at the rising edge of the CNTR1 pin input signal.
However, in the pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

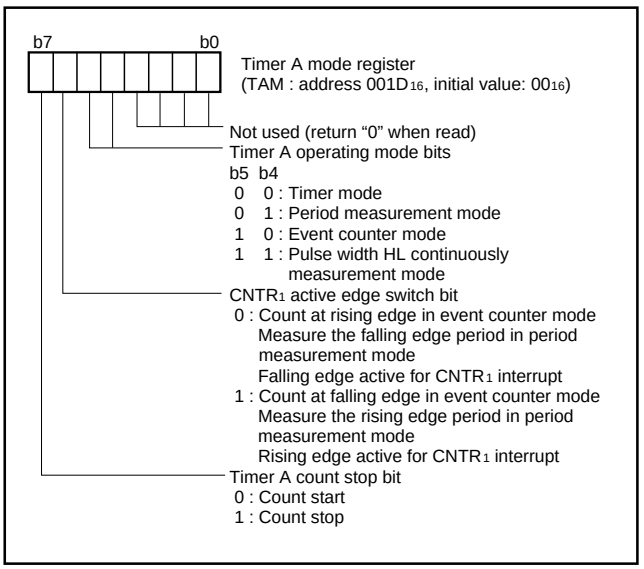


Fig. 22 Structure of timer A mode register

●Timer X

Timer X is an 8-bit timer and counts the prescaler X output.
When Timer X underflows, the timer X interrupt request bit is set to "1".
Prescaler X is an 8-bit prescaler and counts the signal selected by the timer X count source selection bit.
Prescaler X and Timer X have the prescaler X latch and the timer X latch to retain the reload value, respectively. The value of prescaler X latch is set to Prescaler X when Prescaler X underflows.The value of timer X latch is set to Timer X when Timer X underflows.
When writing to Prescaler X (PREX) is executed, the value is written to both the prescaler X latch and Prescaler X.
When writing to Timer X (TX) is executed, the value is written to both the timer X latch and Timer X.
When reading from Prescaler X (PREX) and Timer X (TX) is executed, each count value is read out.

Timer X can can be selected in one of 4 operating modes by setting the timer X mode register.

(1) Timer mode

Prescaler X counts the selected count source. Each time the count clock is input, the contents of Prescaler X is decremented by 1. When the contents of Prescaler X reach "00_{16}", an underflow occurs at the next count clock, and the prescaler X latch is reloaded into Prescaler X and count continues. The division ratio of Prescaler X is 1/(n+1) provided that the value of Prescaler X is n.
The contents of Timer X is decremented by 1 each time the underflow signal of Prescaler X is input. When the contents of Timer X reach "00_{16}", an underflow occurs at the next count clock, and the timer X latch is reloaded into Timer X and count continues. The division ratio of Timer X is 1/(m+1) provided that the value of Timer X is m. Accordingly, the division ratio of Prescaler X and Timer X is 1/((n+1)×(m+1)) provided that the value of Prescaler X is n and the value of Timer X is m.

(2) Pulse output mode

In the pulse output mode, the waveform whose polarity is inverted each time timer X underflows is output from the $CNTR_0$ pin.
The output level of $CNTR_0$ pin can be selected by the $CNTR_0$ active edge switch bit. When the $CNTR_0$ active edge switch bit is "0", the output of $CNTR_0$ pin is started at "H" level. When this bit is "1", the output is started at "L" level.
Also, the inverted waveform of pulse output from $CNTR_0$ pin can be output from TX_{OUT} pin by setting "1" to the $P0_3/TX_{OUT}$ output valid bit.
When using a timer in this mode, set the port $P1_4$ and $P0_3$ direction registers to output mode.

(3) Event counter mode

The timer X counts signals input from the $P1_4/CNTR_0$ pin.
Except for this, the operation in event counter mode is the same as in timer mode.
The active edge of $CNTR_0$ pin input signal can be selected from rising or falling by the $CNTR_0$ active edge switch bit .

(4) Pulse width measurement mode

In the pulse width measurement mode, the pulse width of the signal input to $P1_4/CNTR_0$ pin is measured.
The operation of Timer X can be controlled by the level of the signal input from the $CNTR_0$ pin.
When the $CNTR_0$ active edge switch bit is "0", the signal selected by the timer X count source selection bit is counted while the $CNTR_0$ pin is "H". The count is stopped while the pin is "L". Also, when the $CNTR_0$ active edge switch bit is "1", the signal selected by the timer X count source selection bit is counted while the $CNTR_0$ pin is "L". The count is stopped while the pin is "H".

Timer X can stop counting by setting "1" to the timer X count stop bit in any mode.
Also, when Timer X underflows, the timer X interrupt request bit is set to "1".

Note on Timer X is described below;

■ Note on Timer X

$CNTR_0$ interrupt active edge selection
$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit.
When this bit is "0", the $CNTR_0$ interrupt request bit is set to "1" at the falling edge of $CNTR_0$ pin input signal. When this bit is "1", the $CNTR_0$ interrupt request bit is set to "1" at the rising edge of $CNTR_0$ pin input signal.

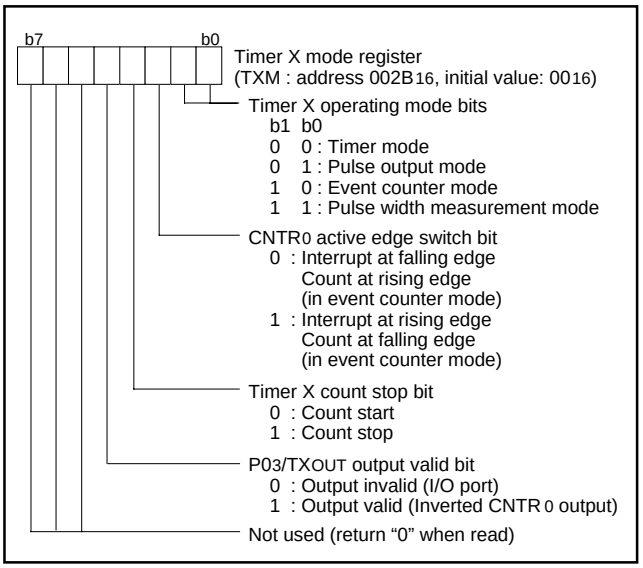
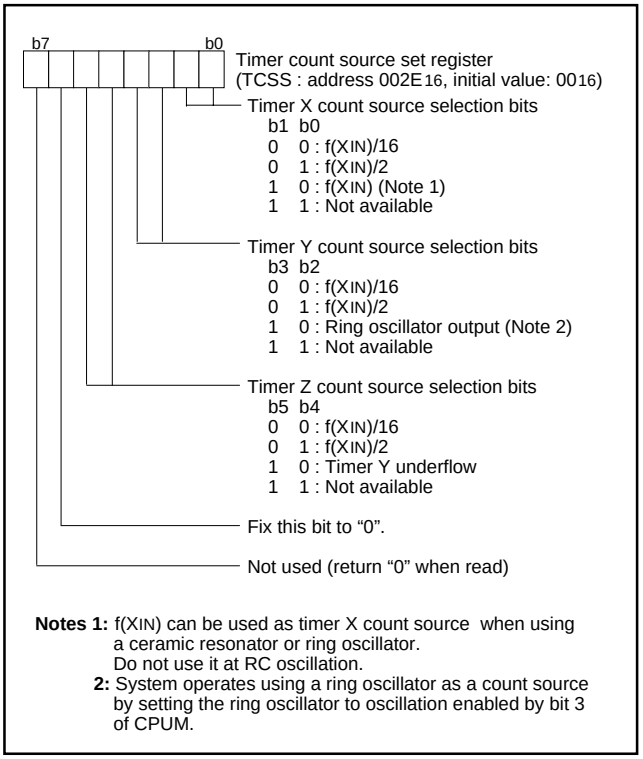


Fig. 23 Structure of timer X mode register



Notes 1: f(XIN) can be used as timer X count source when using a ceramic resonator or ring oscillator.
Do not use it at RC oscillation.
2: System operates using a ring oscillator as a count source by setting the ring oscillator to oscillation enabled by bit 3 of CPUM.

Fig. 24 Timer count source set register

●Timer Y

Timer Y is an 8-bit timer and counts the prescaler Y output.
When Timer Y underflows, the timer Y interrupt request bit is set to "1".
Prescaler Y is an 8-bit prescaler and counts the signal selected by the timer Y count source selection bit.
Prescaler Y has the prescaler Y latch to retain the reload value. Timer Y has the timer Y primary latch and timer Y secondary latch to retain the reload value.
The value of prescaler Y latch is set to Prescaler Y when Prescaler Y underflows.The value of timer Y primary latch or timer Y secondary latch are set to Timer Y when Timer Y underflows.
As for the value to transfer to Timer Y, either of timer Y primary or timer Y secondary is selected depending on the timer Y operating mode.

When writing to Prescaler Y (PREY), timer Y primary (TYP) or timer Y secondary (TYS) is executed, writing to "latch only" or "latch and prescaler (timer)" can be selected by the setting value of the timer Y write control bit. Be sure to set the write control bit because there are some notes according to the operating mode.
When reading from Prescaler Y (PREY) is executed, the count value of Prescaler Y is read out. When reading from timer Y primary (TYP) is executed, the count value of Timer Y is read out. The count value of Timer Y can be read out by reading from the timer Y primary (TYP) even when the value of timer Y primary latch or timer Y secondary latch is counted. When reading the timer Y secondary (TYS) is executed, the undefined value is read out.

Timer Y can be selected in one of 2 operating modes by setting the timer Y, Z mode register.

(1) Timer mode

Prescaler Y counts the selected count source. Each time the count clock is input, the contents of Prescaler Y is decremented by 1. When the contents of Prescaler Y reach "00_{16}", an underflow occurs at the next count clock, and the prescaler Y latch is reloaded into Prescaler Y. The division ratio of Prescaler Y is 1/(n+1) provided that the value of Prescaler Y is n.
The contents of Timer Y is decremented by 1 each time the underflow signal of Prescaler Y is input. When the contents of Timer Y reach "00_{16}", an underflow occurs at the next count clock, and the timer Y primary latch is reloaded into Timer Y and count continues. (In the timer mode, the contents of timer Y primary latch is counted. Timer Y secondary latch is not used in this mode.)
The division ratio of Timer Y is 1/(m+1) provided that the value of Timer Y is m. Accordingly, the division ratio of Prescaler Y and Timer Y is 1/((n+1)×(m+1)) provided that the value of Prescaler Y is n and the value of Timer Y is m.
In the timer mode, writing to "latch only" or "latches and Prescaler Y and timer Y primary" can be selected by the setting value of the timer Y write control bit.

(2) Programmable waveform generation mode

In the programmable waveform generation mode, timer counts the setting value of timer Y primary and the setting value of timer Y secondary alternately, the waveform inverted each time Timer Y underflows is output from TYOUT pin.
When using this mode, be sure to set "1" to the timer Y write control bit to select "write to latch only". Also, set the port $P0_1$ direction registers to output mode.
The active edge of output waveform is set by the timer Y output level latch (b5) of the timer Y, Z waveform output control register (PUM). When "0" is set to b5 of PUM, "H" interval by the setting value of TYP or "L" interval by the setting value of TYS is output alternately. When "1" is set to b5 of PUM, "L" interval by the setting value of TYP or "H" interval by the setting value of TYS is output alternately.
Also, in this mode, the primary interval and the secondary interval of the output waveform can be extended respectively for 0.5 cycle of timer count source clock by setting the timer Y primary waveform extension control bit (b2) and the timer Y secondary waveform extension control bit (b3) of PUM to "1". As a result, the waveforms of more accurate resolution can be output.
When b2 and b3 of PUM are used, the frequency and duty of the output waveform are as follows;

Waveform frequency:
FYOUT=
(2×TMYCL)/(2×(TYP+1)+2×(TYS+1)+(EXPYP+EXPYS))
Duty:
DYOUT=
(2×(TYP+1)+EXPYP)((2×(TYP+1)+EXPYP)+(2×(TYS+1)+EXPYS))

TMYCL: Timer Y count source (frequency)
TYP: Timer Y primary (8bit)
TYS: Timer Y secondary (8bit)
EXPYP: Timer Y primary waveform extension control bit (1bit)
EXPYS: Timer Y secondary waveform extension control bit (1bit)

In the programmable waveform generation mode, when values of the TYP, TYS, EXPYP and EXPYS are changed, the output waveform is changed at the beginning (timer Y primary waveform interval) of waveform period.
When the count values are changed, set values to the TYS, EXPYP and EXPYS first. After then, set the value to TYP. The values are set all at once at the beginning of the next waveform period when the value is set to TYP. (When writing at timer stop is executed, writing to TYP at last is required.)

Notes on programmable waveform generation mode is described below;

■ Notes on programmable generation waveform mode

• Count set value

In the programmable waveform generation mode, values of TYS, EXPYP, and EXPYS are valid by writing to TYP because the setting to them is executed all at once by writing to TYP. Even when changing TYP is not required, write the same value again.

• Write timing to TYP

In the programmable waveform generation mode, when the setting value is changed while the waveform is output, set by software in order not to execute the writing to TYP and the timing of timer underflow during the secondary interval simultanesously.

• Usage of waveform extension function

The waveform extension function by the timer Y waveform extension control bit can be used only when "00_{16}" is set to Prescaler Y. When the value other than "00_{16}" is set to Prescaler Y, be sure to set "0" to EXPYP and EXPYS.

• Timer Y write mode

When using this mode, be sure to set "1" to the timer Y write control bit to select "write to latch only".

Timer Y can stop counting by setting "1" to the timer Y count stop bit in any mode.

Also, when Timer Y underflows, the timer Y interrupt request bit is set to "1".

●Timer Z

Timer Z is an 8-bit timer and counts the prescaler Z output.
When Timer Z underflows, the timer Z interrupt request bit is set to "1".
Prescaler Z is an 8-bit prescaler and counts the signal selected by the timer Z count source selection bit.
Prescaler Z has the prescaler Z latch to retain the reload value. Timer Z has the timer Z primary latch and timer Z secondary latch to retain the reload value.
The value of prescaler Z latch is set to Prescaler Z when Prescaler Z underflows.The value of timer Z primary latch or timer Z secondary latch are set to Timer Z when Timer Z underflows.
As for the value to transfer to Timer Z, either of timer Z primary or timer Z secondary is selected depending on the timer Z operating mode.

When writing to Prescaler Z (PREZ), timer Z primary (TZP) or timer Z secondary (TZS) is executed, writing to "latch only" or "latches and Prescaler Z and Timer Z" can be selected by the setting value of the timer Z write control bit. Be sure to set the write control bit because there are some notes according to the operating mode.
When reading from Prescaler Z (PREZ) is executed, the count value of Prescaler Z is read out. When reading from timer Z primary (TZP) is executed, the count value of Timer Z is read out. The count value of Timer Z can be read out by reading from the timer Z primary (TZP) even when the value of timer Z primary latch or timer Z secondary latch is counted. When reading the timer Z secondary (TZS) is executed, the undefined value is read out.

Timer Z can be selected in one of 4 operating modes by setting the timer Y, Z mode register.

(1) Timer mode

Prescaler Z counts the selected count source. Each time the count clock is input, the contents of Prescaler Z is decremented by 1. When the contents of Prescaler Z reach "00_{16}", an underflow occurs at the next count clock, and the prescaler Z latch is reloaded into Prescaler Z. The division ratio of Prescaler Z is 1/(n+1) provided that the value of Prescaler Z is n.
The contents of Timer Z is decremented by 1 each time the underflow signal of Prescaler Z is input. When the contents of Timer Z reach "00_{16}", an underflow occurs at the next count clock, and the timer Z primary latch is reloaded into Timer Z and count continues. (In the timer mode, the contents of timer Z primary latch is counted. Timer Z secondary latch is not used in this mode.)
The division ratio of Timer Z is 1/(m+1) provided that the value of Timer Z is m. Accordingly, the division ratio of Prescaler Z and Timer Z is 1/((n+1)×(m+1)) provided that the value of Prescaler Z is n and the value of Timer Z is m.
In the timer mode, writing to "latch only" or "latches and Prescaler Z and timer Z primary" can be selected by the setting value of the timer Z write control bit.

(2) Programmable waveform generation mode

In the programmable waveform generation mode, timer counts the setting value of timer Z primary and the setting value of timer Z secondary alternately, the waveform inverted each time Timer Z underflows is output from TZ_{OUT} pin.
When using this mode, be sure to set "1" to the timer Z write control bit to select "write to latch only". Also, set the port $P0_2$ direction registers to output mode.
The active edge of output waveform is set by the timer Z output level latch (b4) of the timer Y, Z waveform output control register (PUM). When "0" is set to b4 of PUM, "H" interval by the setting value of TZP or "L" interval by the setting value of TZS is output alternately. When "1" is set to b4 of PUM, "L" interval by the setting value of TZP or "H" interval by the setting value of TZS is output alternately.
Also, in this mode, the primary interval and the secondary interval of the output waveform can be extended respectively for 0.5 cycle of timer count source clock by setting the timer Z primary waveform extension control bit (b0) and the timer Z secondary waveform extension control bit (b1) of PUM to "1". As a result, the waveforms of more accurate resolution can be output.
When b0 and b1 of PUM are used, the frequency and duty of the output waveform are as follows;

Waveform frequency:
FZOUT=
(2×TMZCL)/(2×(TZP+1)+2×(TZS+1)+(EXPZP+EXPZS))

Duty:
DZOUT=
(2×(TZP+1)+EXPZP)((2×(TZP+1)+EXPZP)+(2×(TZS+1)+EXPZS))

TMZCL: Timer Z count source (frequency)
TZP: Timer Z primary (8bit)
TZS: Timer Z secondary (8bit)
EXPZP: Timer Z primary waveform extension control bit (1bit)
EXPZS: Timer Z secondary waveform extension control bit (1bit)

In the programmable waveform generation mode, when values of the TZP, TZS, EXPZP and EXPZS are changed, the output waveform is changed at the beginning (timer Z primary waveform interval) of waveform period.
When the count values are changed, set values to the TZS, EXPZP and EXPZS first. After then, set the value to TZP. The values are set all at once at the beginning of the next waveform period when the value is set to TZP. (When writing at timer stop is executed, writing to TZP at last is required.)

Notes on the programmable waveform generation mode are described below;

■ **Notes on programmable waveform generation mode**

• Count set value

In the programmable waveform generation mode, values of TZS, EXPZP, and EXPZS are valid by writing to TZP because the setting to them is executed all at once by writing to TZP. Even when changing TZP is not required, write the same value again.

• Write timing to TZP

In the programmable waveform generation mode, when the setting value is changed while the waveform is output, set by software in order not to execute the writing to TZP and the timing of timer underflow during the secondary interval simultanesously.

• Usage of waveform extension function

The waveform extension function by the timer Z waveform extension control bit can be used only when "00_{16}" is set to Prescaler Z. When the value other than "00_{16}" is set to Prescaler Z, be sure to set "0" to EXPZP and EXPZS. Also, when the timer Y underflow is selected as the count source, the waveform extension function cannot be used.

• Timer Z write mode

When using this mode, be sure to set "1" to the timer Z write control bit to select "write to latch only".

(3) Programmable one-shot generation mode

In the programmable one-shot generation mode, the one-shot pulse by the setting value of timer Z primary can be output from TZ_{OUT} pin by software or external trigger. When using this mode, be sure to set "1" to the timer Z write control bit to select "write to latch only". Also, set the port $P0_2$ direction registers to output mode. In this mode, TZS is not used.

The active edge of output waveform is set by the timer Z output level latch (b5) of the timer Y, Z waveform output control register (PUM). When "0" is set to b5 of PUM, "H" pulse during the interval of the TZP setting value is output. When "1" is set to b5 of PUM, "L" pulse during the interval of the TZP setting value is output.

Also, in this mode, the interval of the one-shot pulse output can be extended for 0.5 cycle of timer count source clock by setting the timer Z primary waveform extension control bit (b2) of PUM to "1". As a result, the waveforms of more accurate resolution can be output.

In the programmable one-shot generation mode, the trigger by software or the external INT_0 pin can be accepted by writing "0" to the timer Z count stop bit after the count value is set. (At the time when "0" is written to the timer Z count stop bit, Timer Z stops.)

By writing "1" to the timer Z one-shot start bit, or by inputting the valid trigger to the INT_0 pin after the trigger to the INT_0 pin becomes valid by writing "1" to the INT_0 pin one-shot trigger control bit, Timer Z starts counting, at the same time, the output of TZ_{OUT} pin is inverted. When Timer Z underflows, the output of TZ_{OUT} pin is inverted again and Timer Z stops. When also the trigger of INT_0 pin is accepted, the contents of the one-shot start bit is changed to "1" by hardware.

The falling or rising can be selected as the edge of the valid trigger of INT_0 pin by the INT_0 pin one-shot trigger edge selection bit.

During the one-shot pulse output interval, the one-shot pulse output can be stopped forcibly by writing "0" to the timer Z one-shot start bit.

In the programmable one-shot generation mode, when the count values are changed, set value to the EXPZP first. After then, set the value to TZP. The values are set all at once at the beginning of the next one-shot pulse when the value is set to TZP. (When writing at timer stop is executed, writing to TZP at last is required.)

Notes on the programmable one-shot generation mode are described below;

■ **Notes on programmable one-shot generation mode**

• Count set value

In the programmable one-shot generation mode, the value of EXPZP becomes valid by writing to TZP. Even when changing TZP is not required, write the same value again.

• Write timing to TZP

In the programmable one-shot generation mode, when the setting value is changed while the waveform is output, set by software in order not to execute the writing to TZP and the timing of timer underflow simultanesously.

• Usage of waveform extension function

The waveform extension function by the timer Z waveform extension control bit can be used only when "00_{16}" is set to Prescaler Z. When the value other than "00_{16}" is set to Prescaler Z, be sure to set "0" to EXPZP. Also, when the timer Y underflow is selected as the count source, the waveform extension function cannot be used.

• Timer Z write mode

When using this mode, be sure to set "1" to the timer Z write control bit to select "write to latch only".

(4) Programmable wait one-shot generation mode

In the programmable wait one-shot generation mode, the one-shot pulse by the setting value of timer Z secondary can be output from TZOUT pin by software or external trigger to INT0 pin after the wait by the setting value of the timer Z primary. When using this mode, be sure to set "1" to the timer Z write control bit to select "write to latch only". Also, set the port P02 direction registers to output mode.

The active edge of output waveform is set by the timer Z output level latch (b5) of the timer Y, Z waveform output control register (PUM). When "0" is set to b5 of PUM, after the wait during the interval of the TZP setting value, "H" pulse during the interval of the TZS setting value is output. When "1" is set to b5 of PUM, after the wait during the interval of the TZP setting value, "L" pulse during the interval of the TZS setting value is output.

Also, in this mode, the intervals of the wait and the one-shot pulse output can be extended for 0.5 cycle of timer count source clock by setting EXPZP and EXPZS of PUM to "1". As a result, the waveforms of more accurate resolution can be output.

In the programmable wait one-shot generation mode, the trigger by software or the external INT0 pin can be accepted by writing "0" to the timer Z count stop bit after the count value is set. (At the time when "0" is written to the timer Z count stop bit, Timer Z stops.)

By writing "1" to the timer Z one-shot start bit, or by inputting the valid trigger to the INT0 pin after the trigger to the INT0 pin becomes valid by writing "1" to the INT0 pin one-shot trigger control bit, Timer Z starts counting.

While Timer Z counts the TZP, the initial value of the TZOUT pin output is retained. When Timer Z underflows, the value of TZS is reloaded, at the same time, the output of TZOUT pin is inverted.

When Timer Z underflows, the output of TZOUT pin is inverted again and Timer Z stops. When also the trigger of INT0 pin is accepted, the contents of the one-shot start bit is changed to "1" by hardware.

The falling or rising can be selected as the edge of the valid trigger of INT0 pin by the INT0 pin one-shot trigger edge selection bit.

During the wait interval and the one-shot pulse output interval, the one-shot pulse output can be stopped forcibly by writing "0" to the timer Z one-shot start bit.

In the programmable wait one-shot generation mode, when the count values are changed, set values to the TZS, EXPZP and EXPZS first. After then, set the value to TZP. The values are set all at once at the beginning of the next wait interval when the value is set to TZP. (When writing at timer stop is executed, writing to TZP at last is required.)

Notes on the programmable wait one-shot generation mode are described below;

■ **Notes on programmable wait one-shot generation mode**

• Count set value

In the programmable wait one-shot generation mode, values of TZS, EXPZP and EXPZS are valid by writing to TZP. Even when changing TZP is not required, write the same value again.

• Write timing to TZP

In the programmable wait one-shot generation mode, when the setting value is changed while the waveform is output, set by software in order not to execute the writing to TZP and the timing of timer underflow during the secondary interval simultanesously.

• Usage of waveform extension function

The waveform extension function by the timer Z waveform extension control bit can be used only when "00_{16}" is set to Prescaler Z. When the value other than "00_{16}" is set to Prescaler Z, be sure to set "0" to EXPZP and EXPZS. Also, when the timer Y underflow is selected as the count source, the waveform extension function cannot be used.

• Timer Z write mode

When using this mode, be sure to set "1" to the timer Z write control bit to select "write to latch only".

Timer Z can stop counting by setting "1" to the timer Z count stop bit in any mode.

Also, when Timer Z underflows, the timer Z interrupt request bit is set to "1".

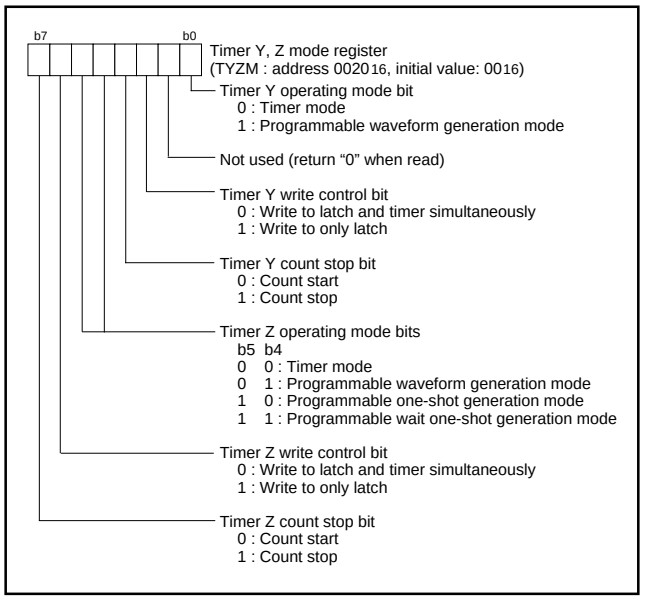


Fig. 25 Structure of timer Y, Z mode register

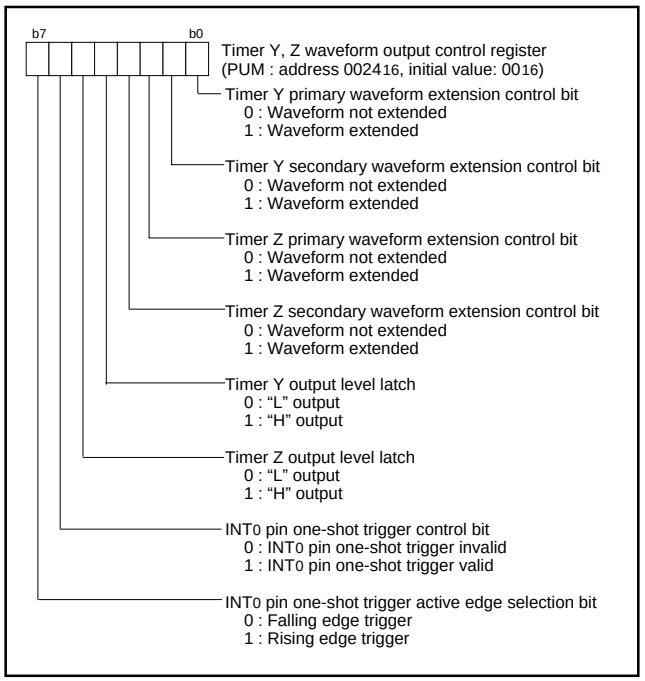


Fig. 26 Structure of timer YZ waveform output control register

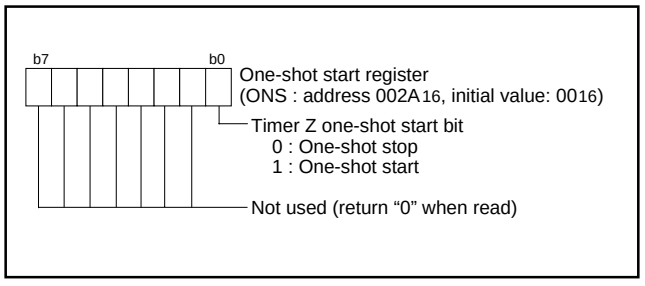


Fig. 27 Structure of one-shot start register

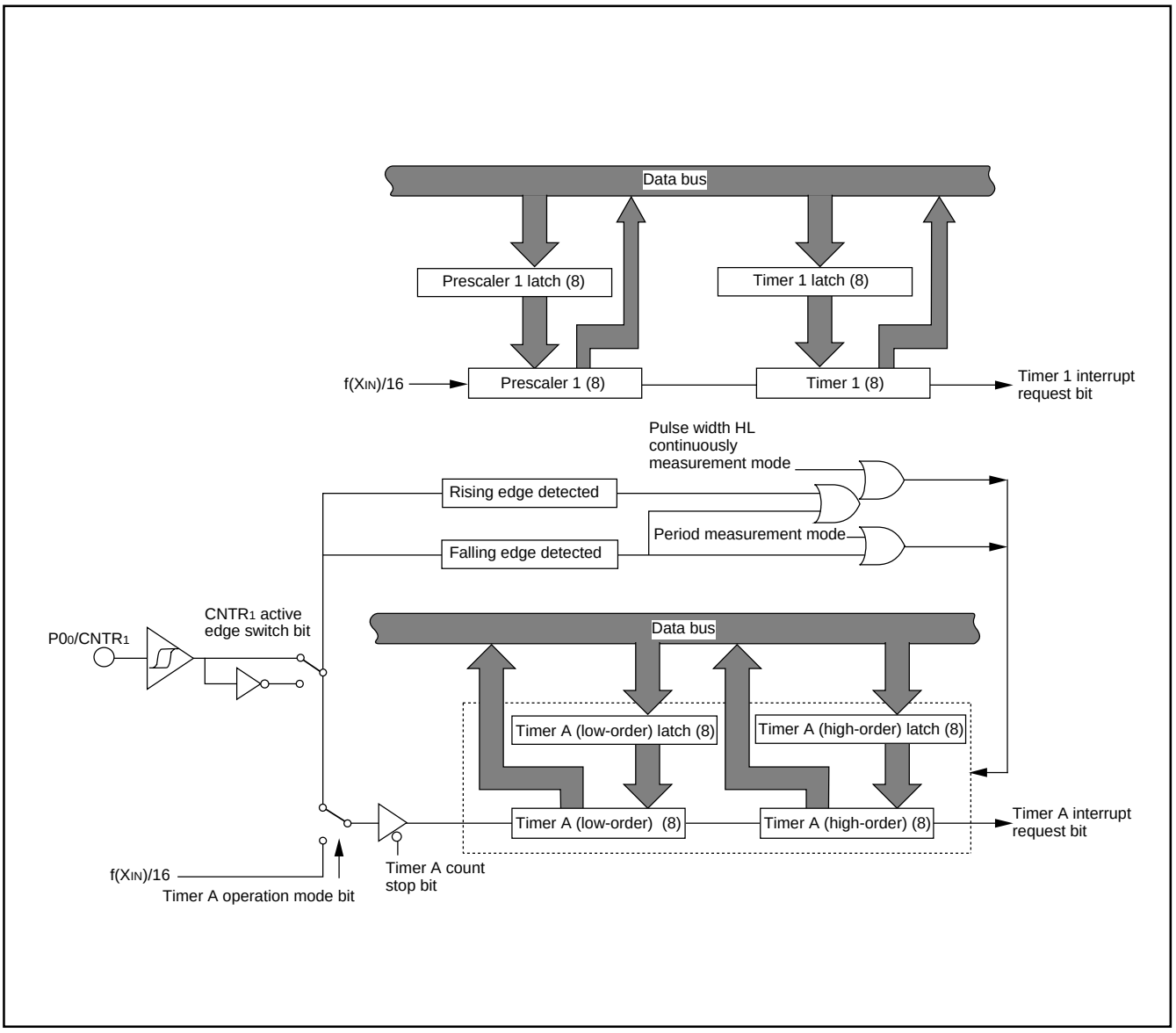


Fig. 28 Block diagram of timer 1 and timer A

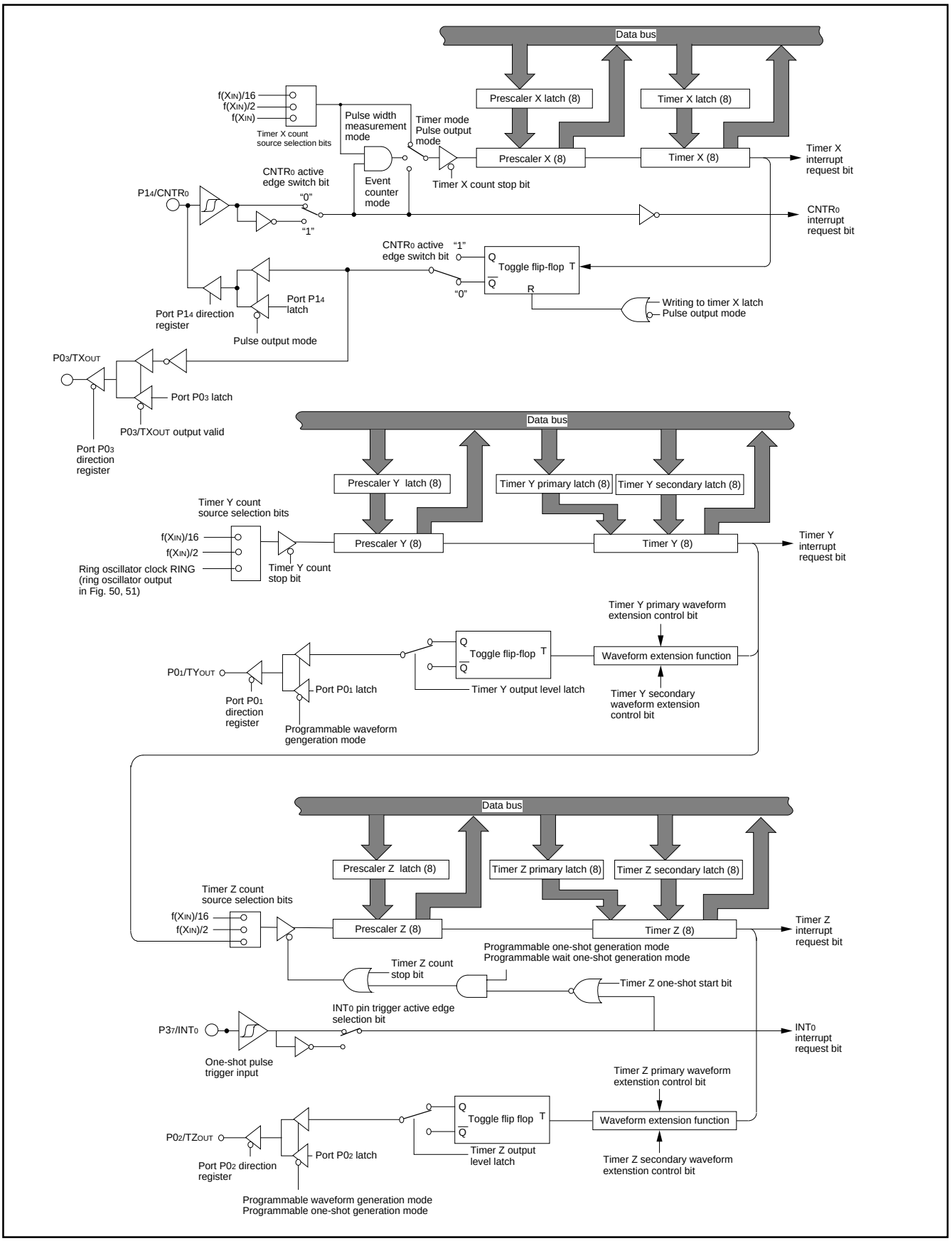


Fig. 29 Block diagram of timer X, timer Y and timer Z

Serial I/O

●Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6) to "1".

For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

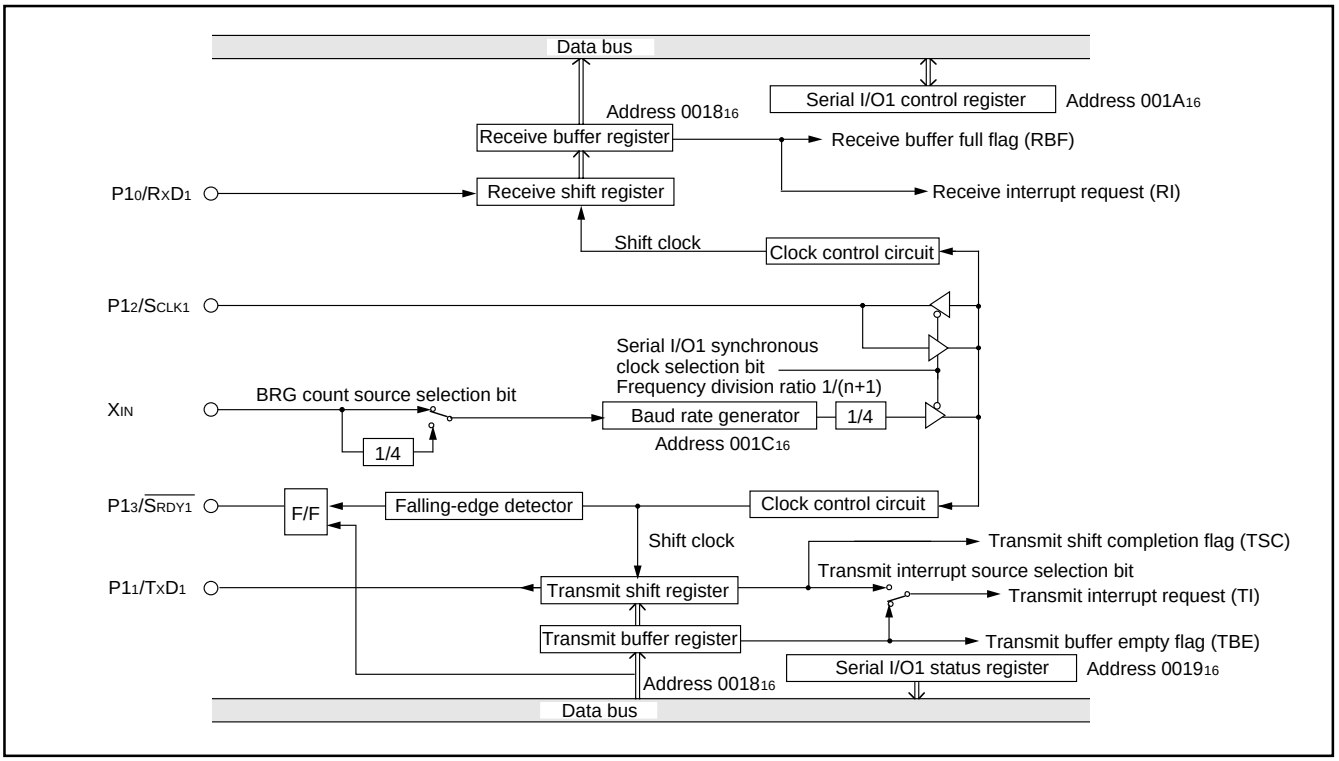
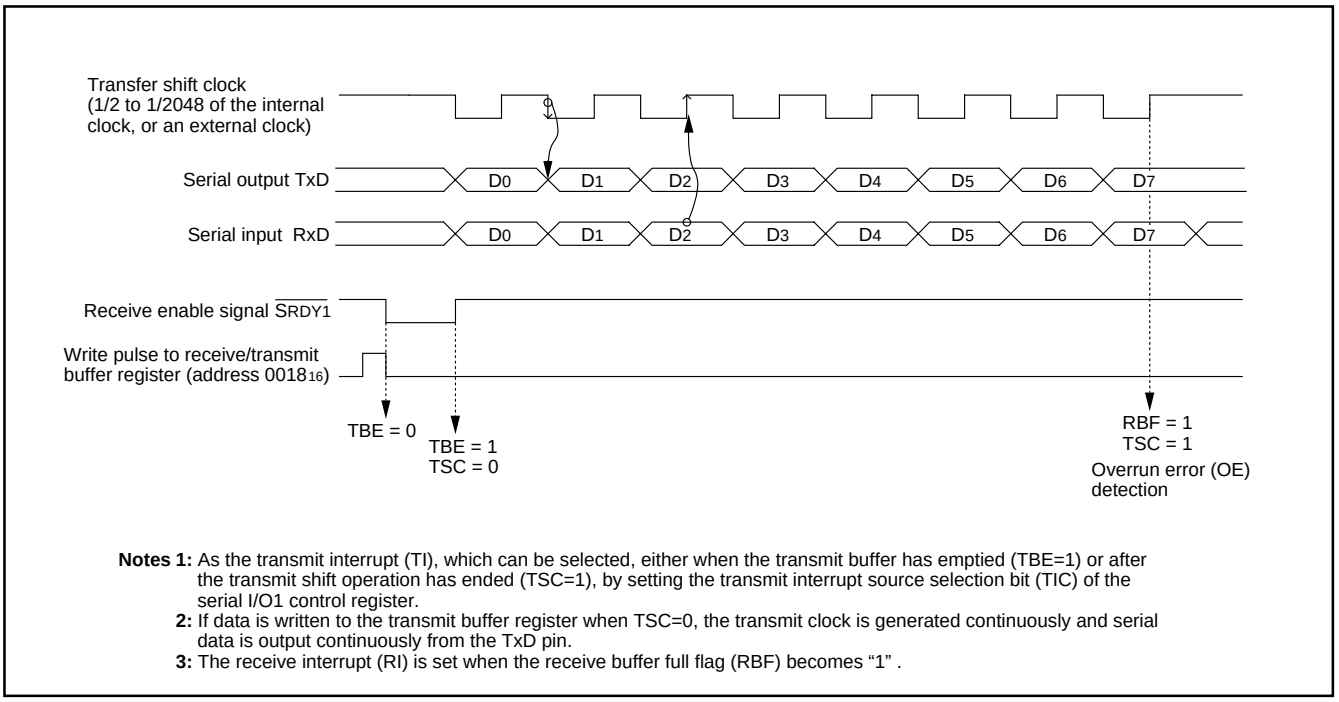


Fig. 30 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 31 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

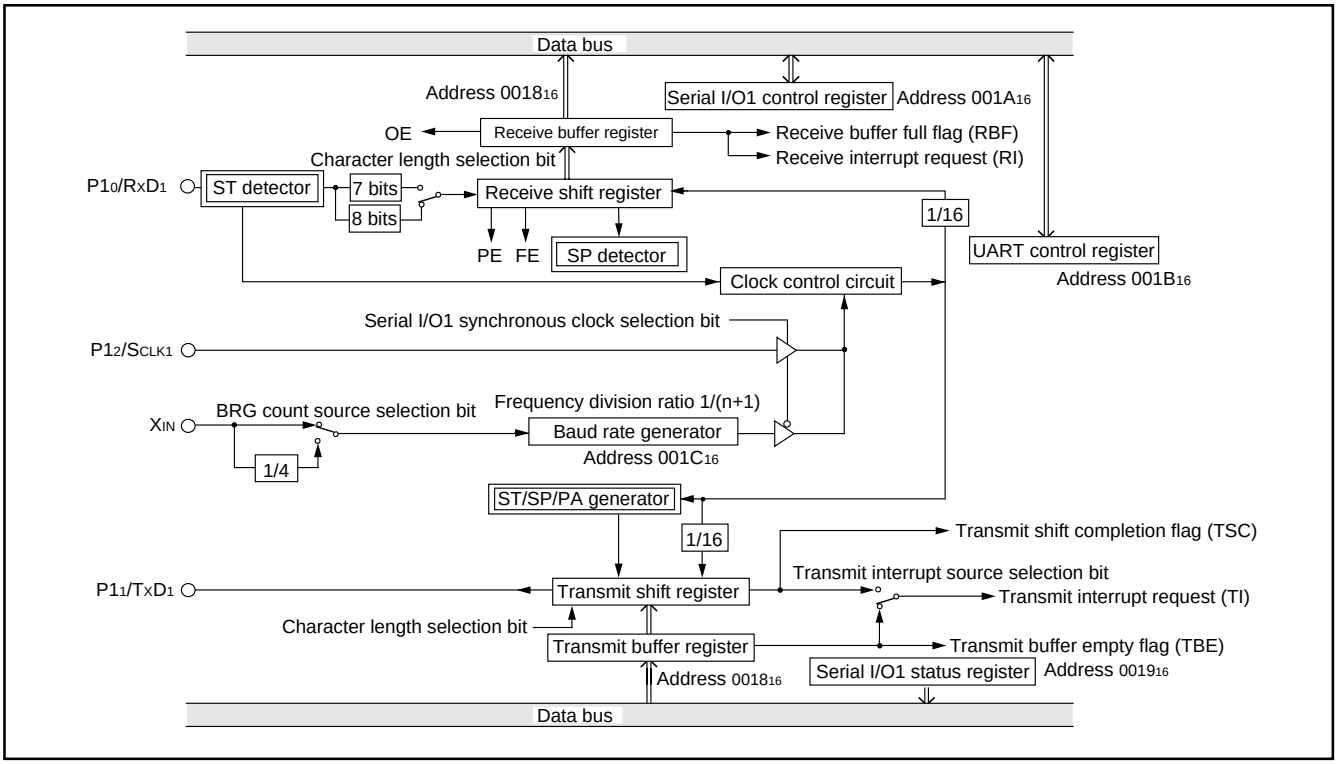
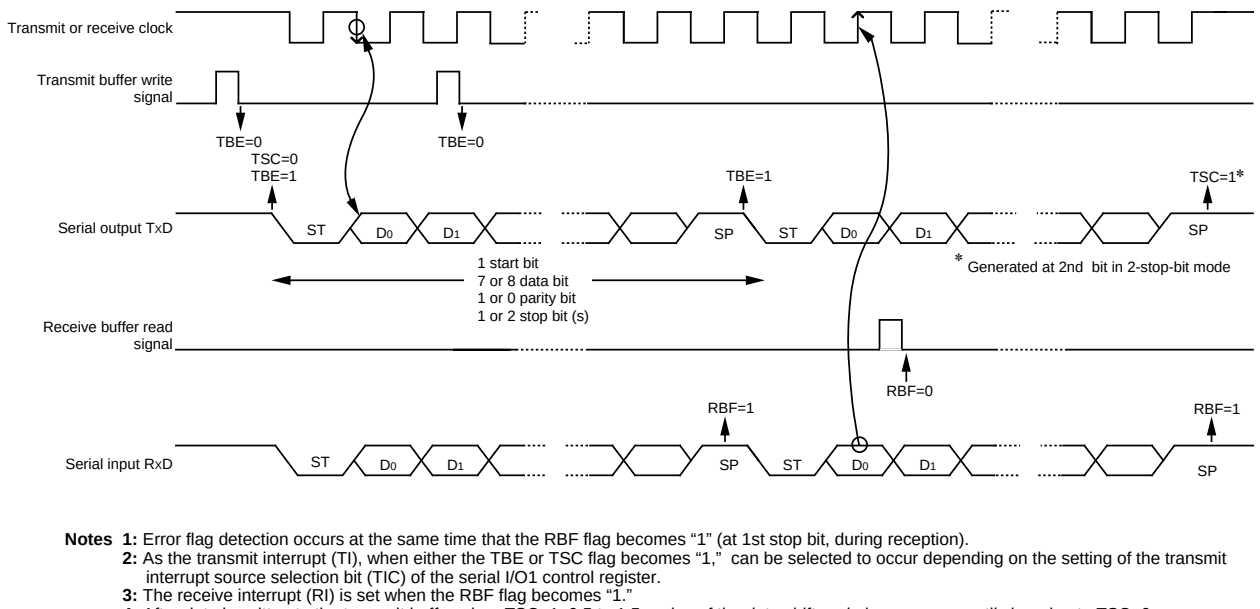


Fig. 32 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1."
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 33 Operation of UART serial I/O1 function

[Transmit buffer register/receive buffer register (TB/RB)] 0018_{16}

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 status register (SIO1STS)] 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 control register (SIO1CON)] $001A_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART control register (UARTCON)] $001B_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P11/TXD_1$ pin.

[Baud rate generator (BRG)] $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■ Notes

When setting the transmit enable bit to "1", the serial I/O1 transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.

① Clear the serial I/O1 transmit interrupt enable bit to "0" (disabled).
② Set the transmit enable bit to "1".
③ Clear the serial I/O1 transmit interrupt request bit to "0" after 1 or more instructions have been executed.
⑤ Set the serial I/O1 transmit interrupt enable bit to "1".

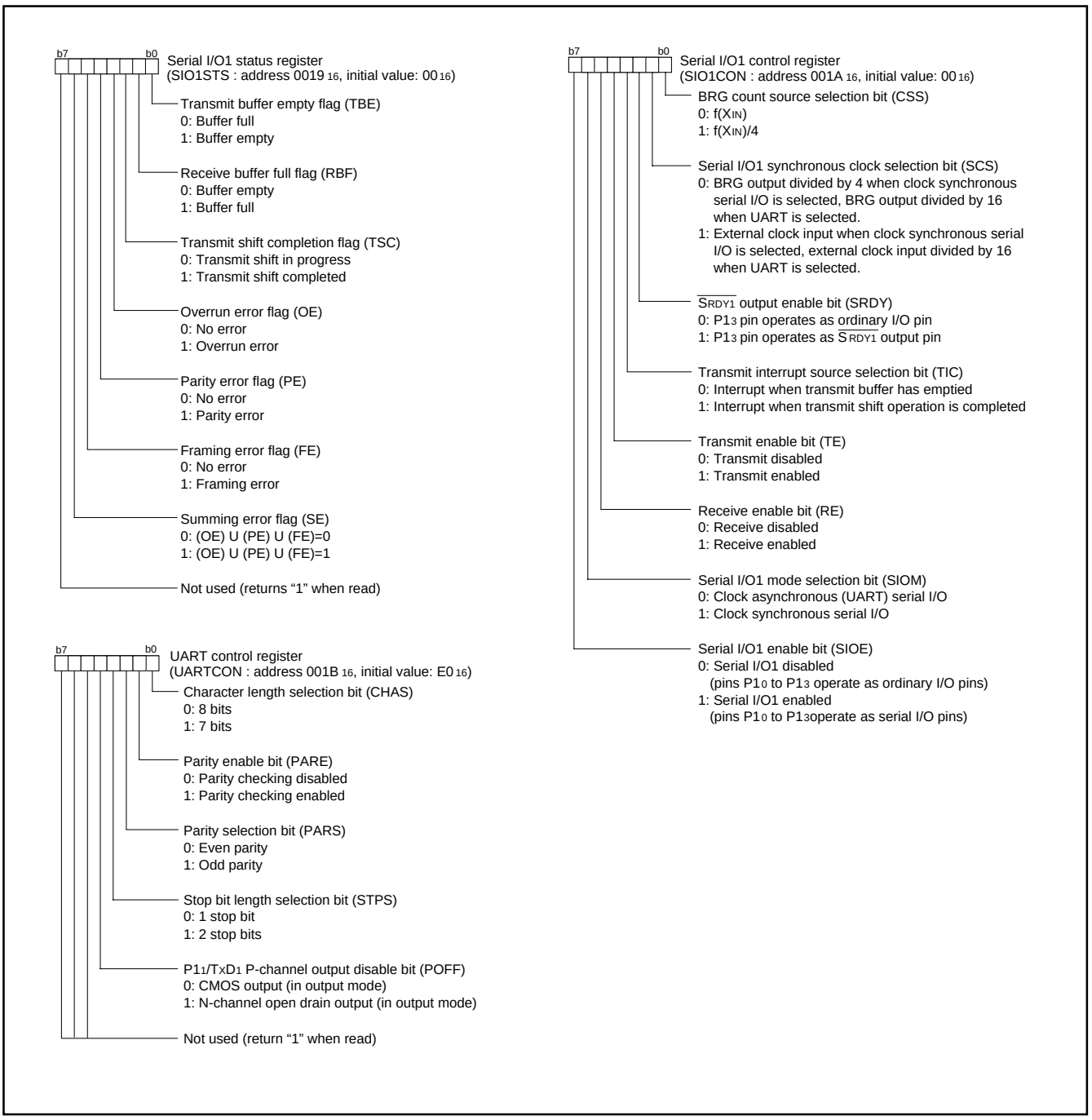


Fig. 34 Structure of serial I/O1-related registers

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

Note: Serial I/O2 can be used in the following cases;

(1) Serial I/O1 is not used,

(2) Serial I/O1 is used as UART and BRG output divided by 16 is selected as the synchronized clock.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

• Set “0” to bit 3 to receive.

• At reception, clear bit 7 to “0” by writing a dummy data to the serial I/O2 register after completion of shift.

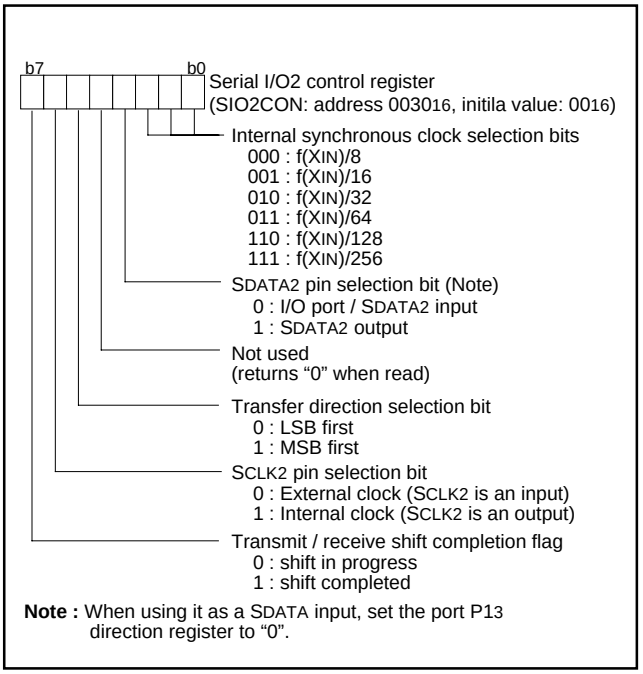


Fig. 35 Structure of serial I/O2 control registers

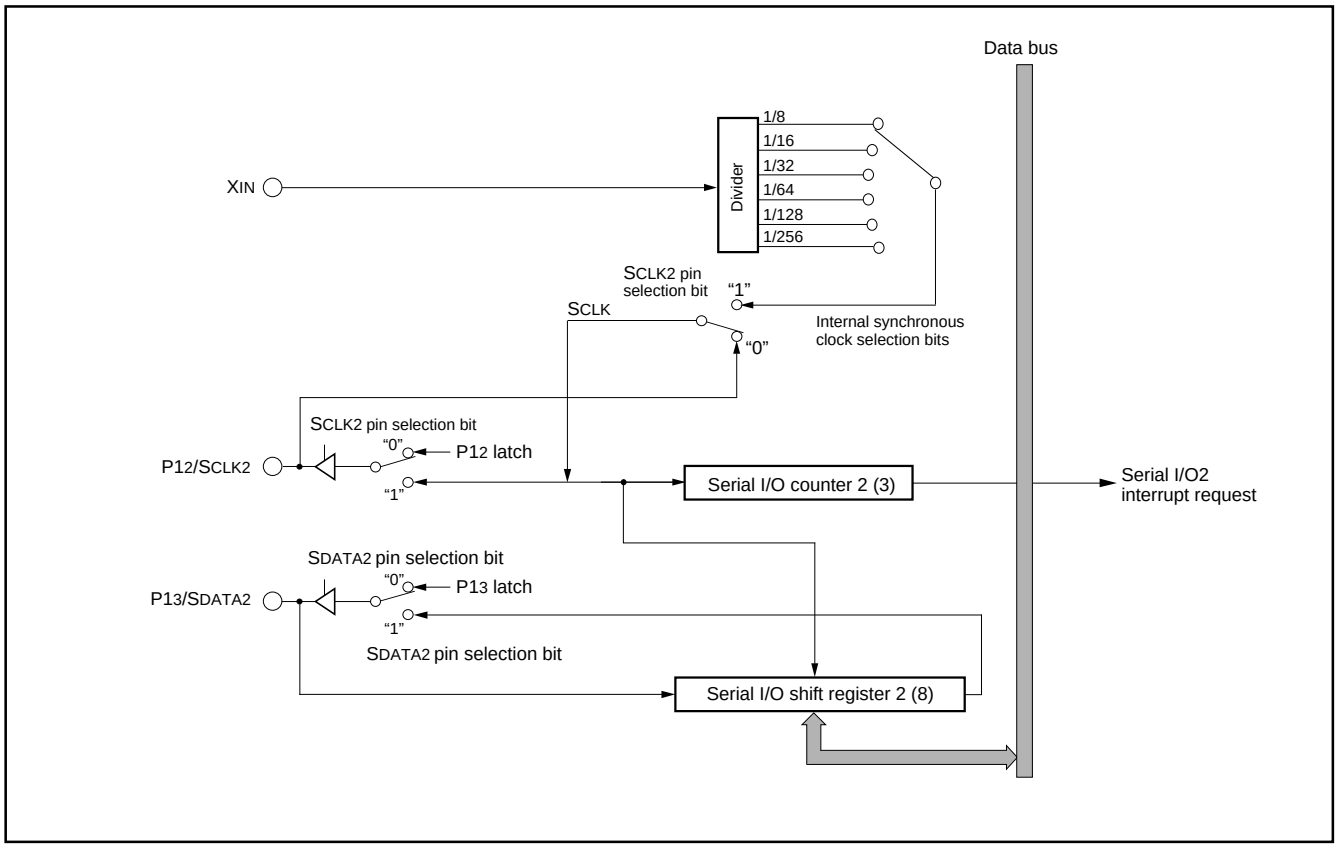


Fig. 36 Block diagram of serial I/O2

Serial I/O2 operation

By writing to the serial I/O2 register (address 0031_{16}) the serial I/O2 counter is set to "7".

After writing, the SDATA2 pin outputs data every time the transfer clock shifts from "H" to "L". And, as the transfer clock shifts from "L" to "H", the SDATA2 pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

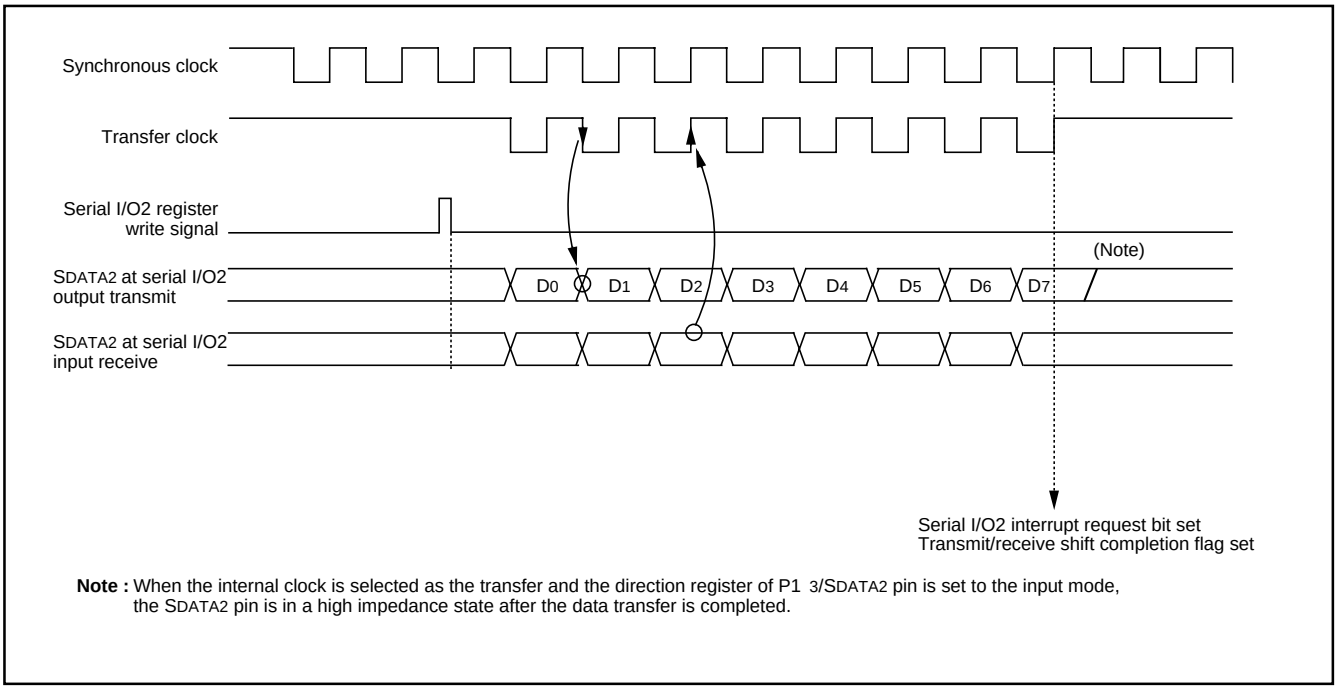
When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

- Serial I/O2 counter is cleared to "0".
- Transfer clock stops at an "H" level.
- Interrupt request bit is set.
- Shift completion flag is set.

Also, the SDATA2 pin is in a high impedance state after the data transfer is completed (refer to Fig.37).

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA2 pin is not in a high impedance state on the completion of data transfer.

Also, after the receive operation is completed, the transmit/receive shift completion flag is cleared by reading the serial I/O2 register. At transmit, the transmit/receive shift completion flag is cleared and the transmit operation is started by writing to serial I/O2 register.



Note : When the internal clock is selected as the transfer and the direction register of P1 3/SDATA2 pin is set to the input mode, the SDATA2 pin is in a high impedance state after the data transfer is completed.

Fig. 37 Serial I/O2 timing (LSB first)

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion.
A-D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 1024, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports P27/AN7 to P20/AN0, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A-D conversion.

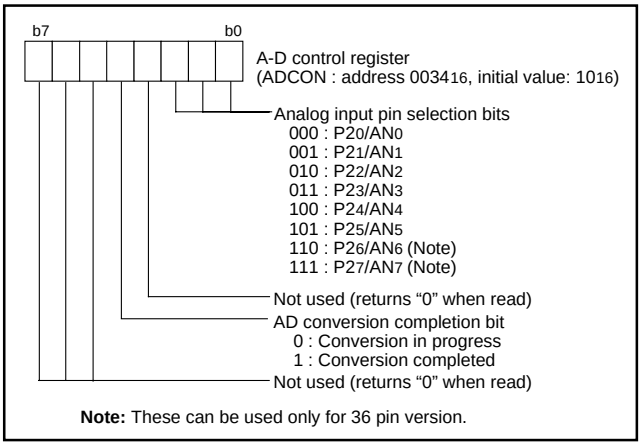


Fig. 38 Structure of A-D control register

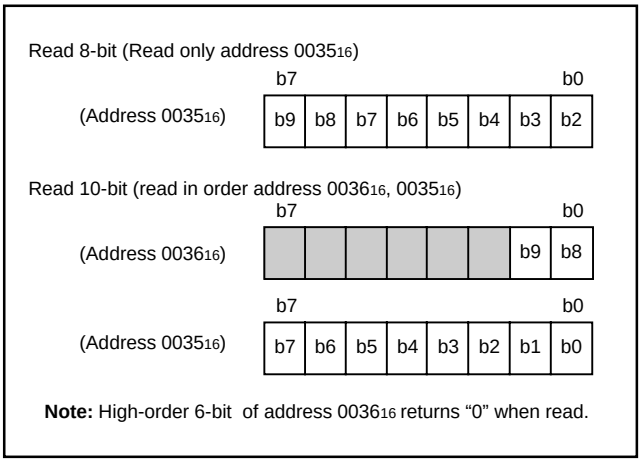


Fig. 39 Structure of A-D conversion register

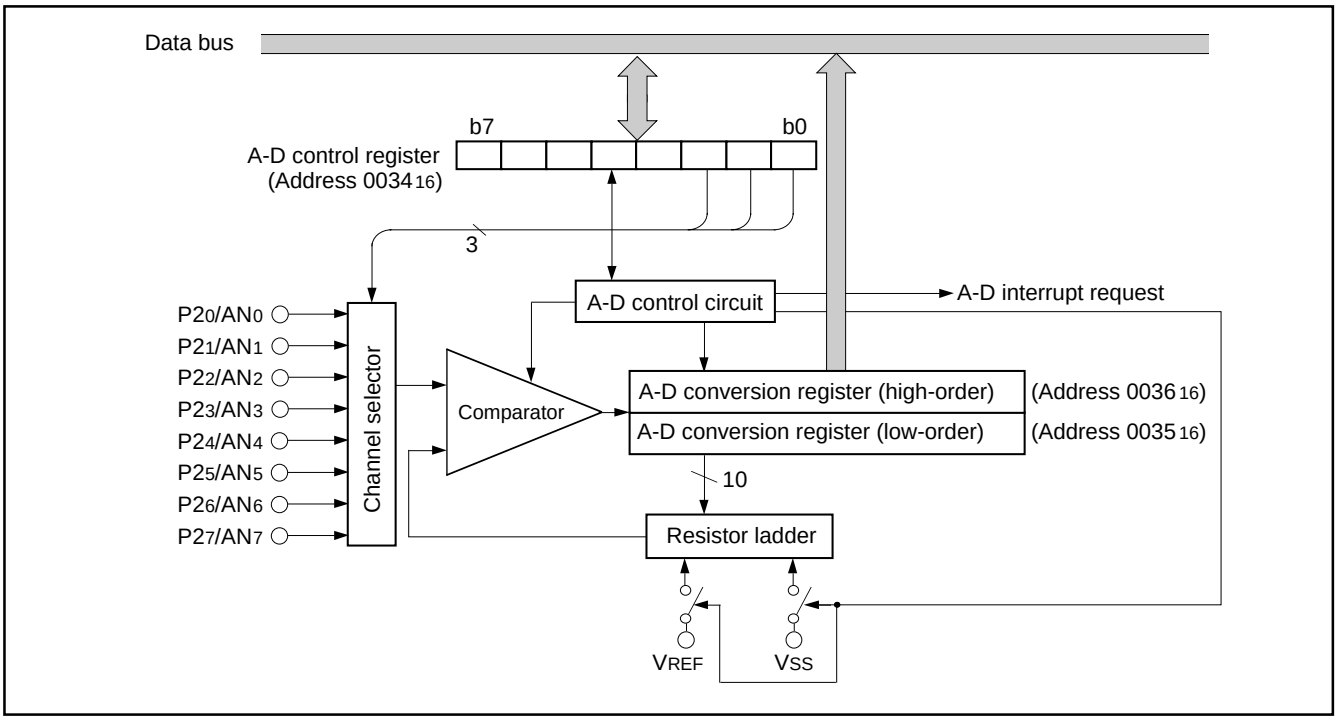


Fig. 40 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.

When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at f(XIN)=8 MHz.

When this bit is "1", the count source becomes f(XIN)/16. In this case, the detection time is 512 μs at f(XIN)=8 MHz.

This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.

Once this bit is set to "1", it cannot be changed to "0" by program.

This bit is cleared to "0" after reset.

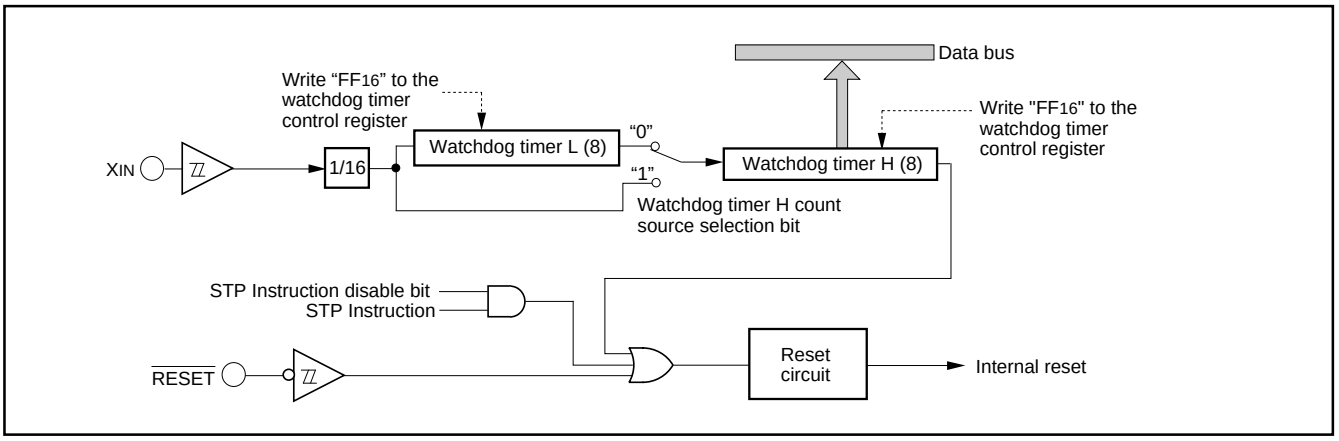


Fig. 41 Block diagram of watchdog timer

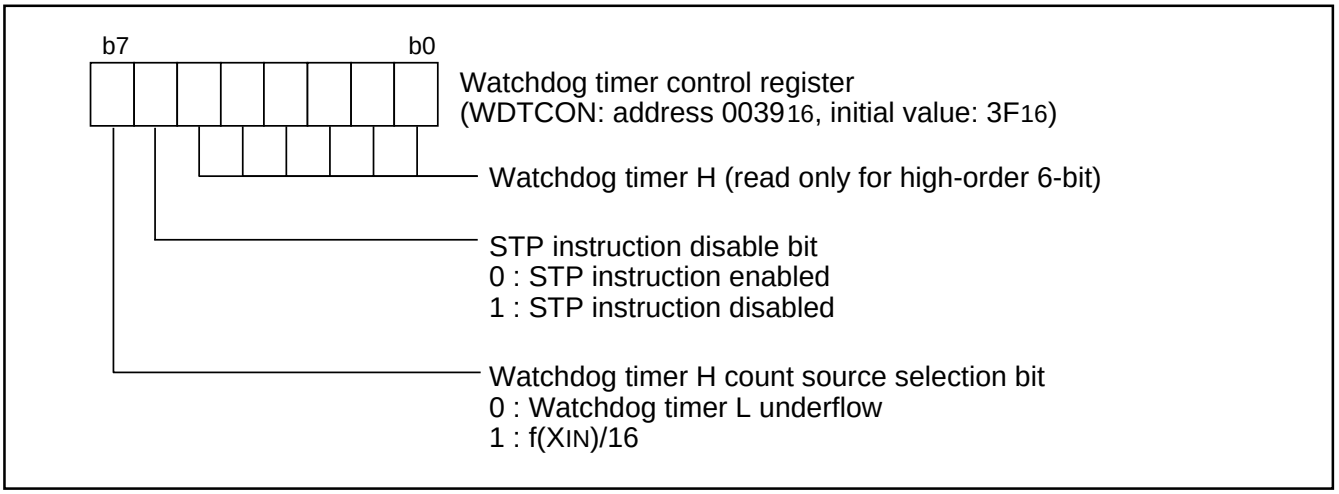


Fig. 42 Structure of watchdog timer control register

Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{\text{RESET}}$ pin at the "L" level for 2 μs or more when the power source voltage is 2.2 to 5.5 V and X_{IN} is in stable oscillation.

After that, this reset status is released by returning the $\overline{\text{RESET}}$ pin to the "H" level. The program starts from the address having the contents of address $FFFD_{16}$ as high-order address and the contents of address $FFFC_{16}$ as low-order address.

In the case of f(ϕ) ≤ 6 MHz, the reset input voltage must be 0.9 V or less when the power source voltage passes 4.5 V.

In the case of f(ϕ) ≤ 4 MHz, the reset input voltage must be 0.8 V or less when the power source voltage passes 4.0 V.

In the case of f(ϕ) ≤ 2 MHz, the reset input voltage must be 0.48 V or less when the power source voltage passes 2.4 V.

In the case of f(ϕ) ≤ 1 MHz, the reset input voltage must be 0.44 V or less when the power source voltage passes 2.2 V.

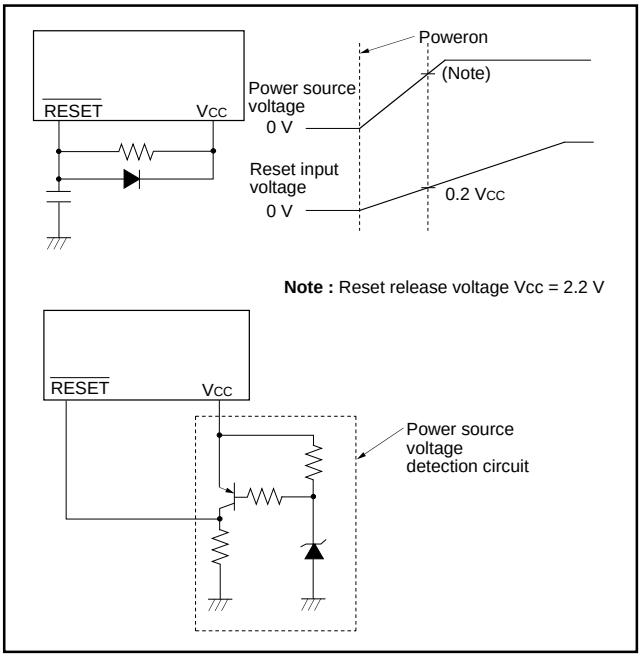


Fig. 43 Example of reset circuit

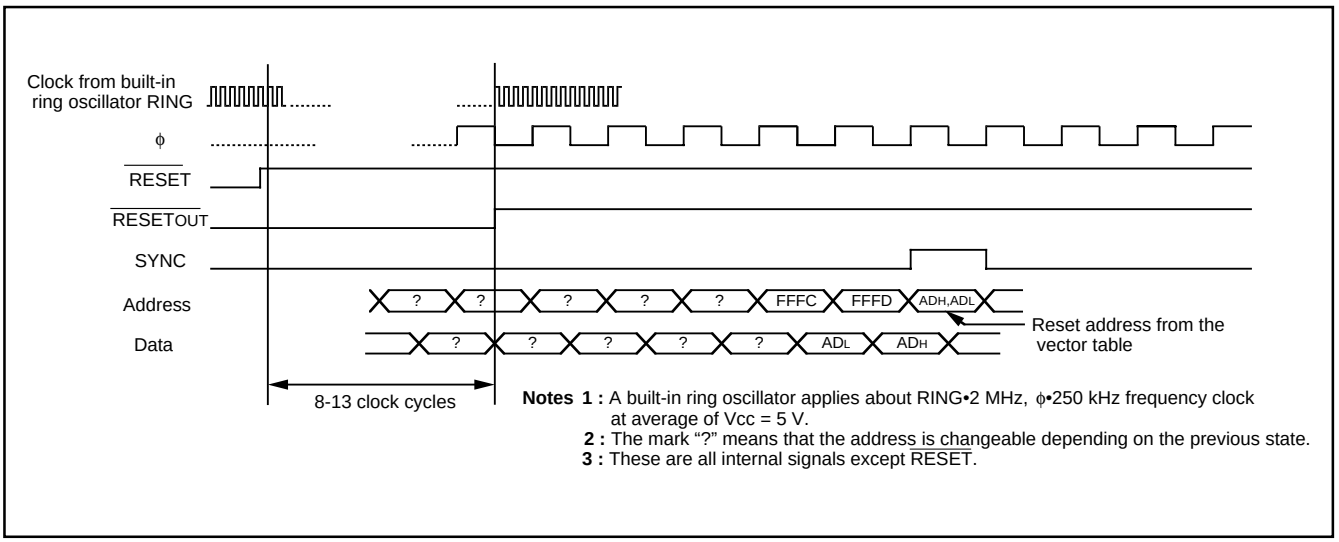


Fig. 44 Timing diagram at reset

	Address	Register contents
(1) Port P0 direction register	0001_{16}	00_{16}
(2) Port P1 direction register	0003_{16}	X X X 0 0 0 0 0
(3) Port P2 direction register	0005_{16}	00_{16}
(4) Port P3 direction register	0007_{16}	00_{16}
(5) Pull-up control register	0016_{16}	00_{16}
(6) Port P1P3 control register	0017_{16}	00_{16}
(7) Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
(8) Serial I/O1 control register	$001A_{16}$	00_{16}
(9) UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(10) Timer A mode register	$001D_{16}$	00_{16}
(11) Timer A (low-order)	$001E_{16}$	FF_{16}
(12) Timer A (high-order)	$001F_{16}$	FF_{16}
(13) Timer Y, Z mode register	0020_{16}	00_{16}
(14) Prescaler Y	0021_{16}	FF_{16}
(15) Timer Y secondary	0022_{16}	FF_{16}
(16) Timer Y primary	0023_{16}	FF_{16}
(17) Timer Y, Z waveform output control register	0024_{16}	00_{16}
(18) Prescaler Z	0025_{16}	FF_{16}
(19) Timer Z secondary	0026_{16}	FF_{16}
(20) Timer Z primary	0027_{16}	FF_{16}
(21) Prescaler 1	0028_{16}	FF_{16}
(22) Timer 1	0029_{16}	01_{16}
(23) One-shot start register	$002A_{16}$	00_{16}
(24) Timer X mode register	$002B_{16}$	00_{16}
(25) Prescaler X	$002C_{16}$	FF_{16}
(26) Timer X	$002D_{16}$	FF_{16}
(27) Timer count source set register	$002E_{16}$	00_{16}
(28) Serial I/O2 control register	0030_{16}	00_{16}
(29) Serial I/O2 register	0031_{16}	00_{16}
(30) A-D control register	0034_{16}	10_{16}
(31) MISRG	0038_{16}	00_{16}
(32) Watchdog timer control register	0039_{16}	0 0 1 1 1 1 1 1
(33) Interrupt edge selection register	$003A_{16}$	00_{16}
(34) CPU mode register	$003B_{16}$	1 0 0 0 0 0 0 0
(35) Interrupt request register 1	$003C_{16}$	00_{16}
(36) Interrupt request register 2	$003D_{16}$	00_{16}
(37) Interrupt control register 1	$003E_{16}$	00_{16}
(38) Interrupt control register 2	$003F_{16}$	00_{16}
(39) Processor status register	(PS)	X X X X X 1 X X
(40) Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$

Note X : Undefined

Fig. 45 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip.

Set the constants of the resistor and capacitor when an RC oscillator is used, so that a frequency variation due to LSI variation and resistor and capacitor variations may not exceed the standard input frequency.

(1) Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock ϕ stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "01_{16}" and prescaler 1 is set to "FF_{16}" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. f(XIN)/16 is forcibly connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock ϕ remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock ϕ is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable.

Also, the STP instruction cannot be used while CPU is operating by a ring oscillator.

• Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

●Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

●Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

●CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37540RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

●Clock division ratio, XIN oscillation control, ring oscillator control

The state transition shown in Fig. 52 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 52.

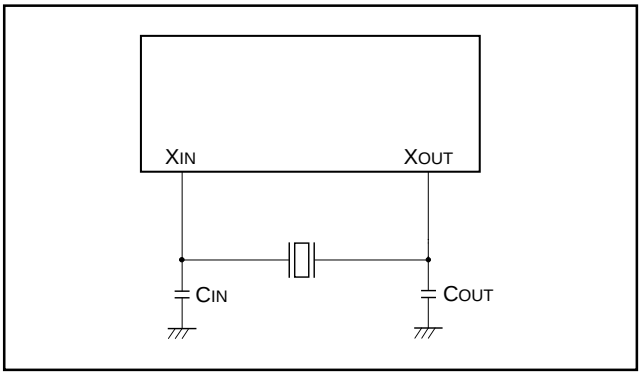


Fig. 46 External circuit of ceramic resonator

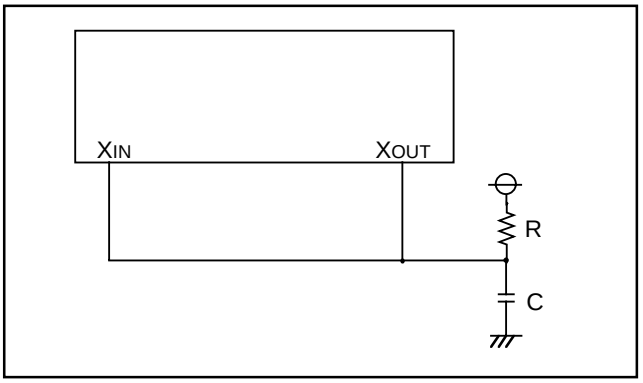


Fig. 47 External circuit of RC oscillation

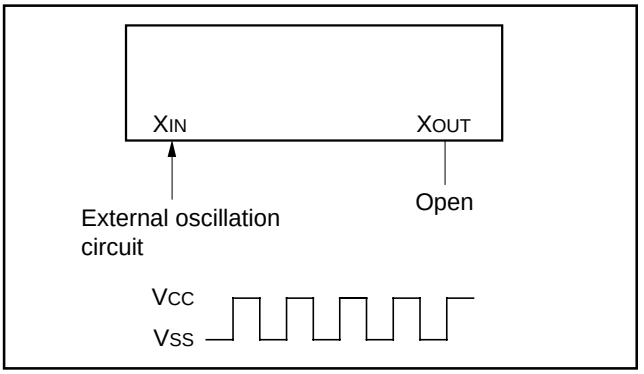


Fig. 48 External clock input circuit

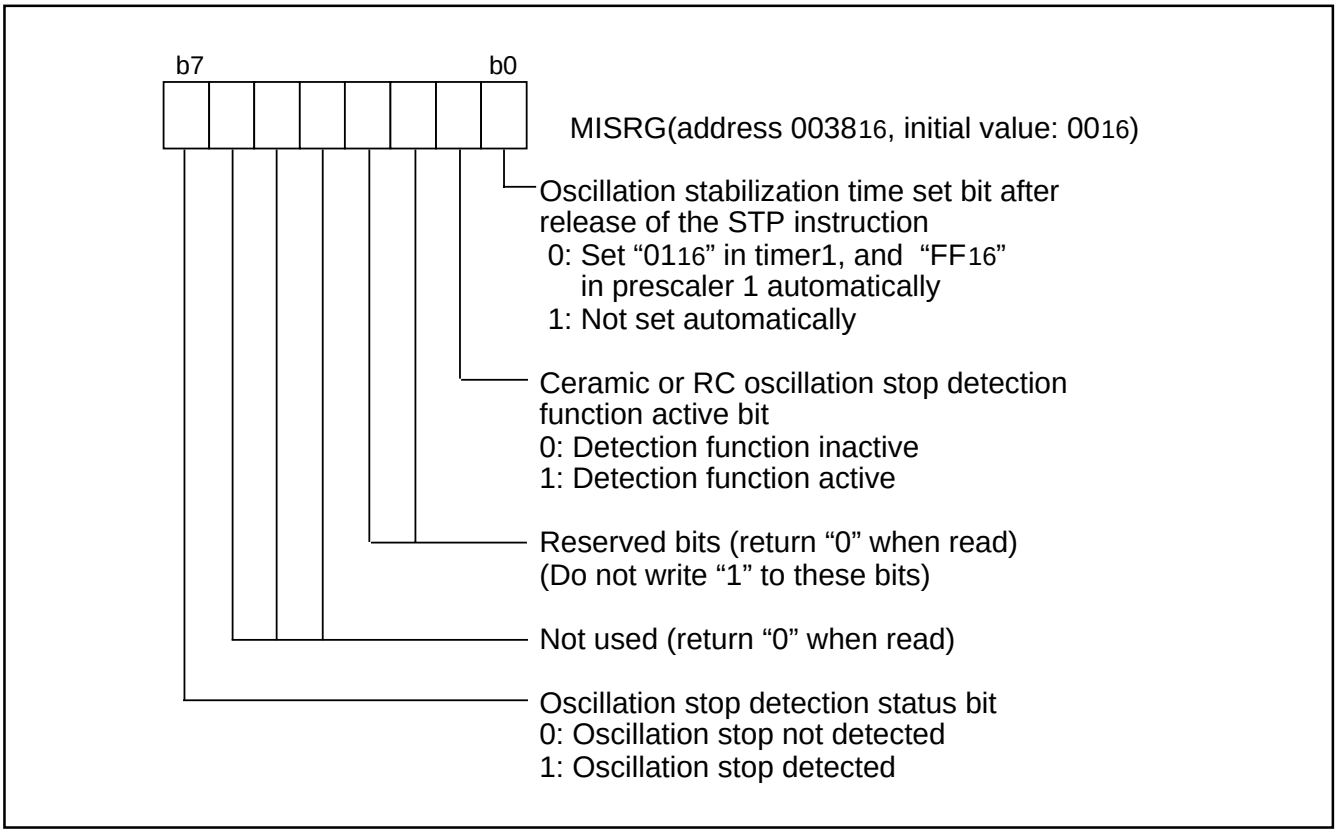


Fig. 49 Structure of MISRG

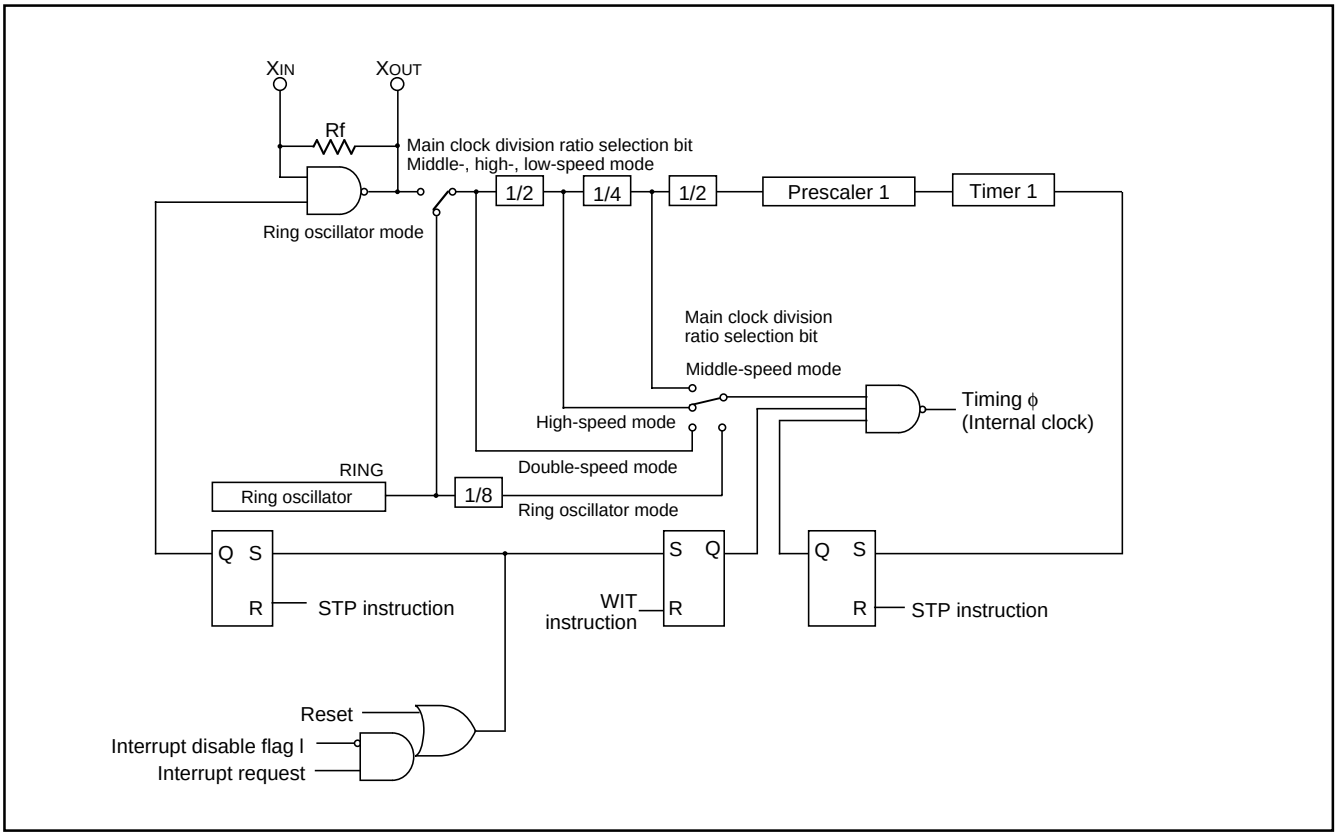


Fig. 50 Block diagram of internal clock generating circuit (for ceramic resonator)

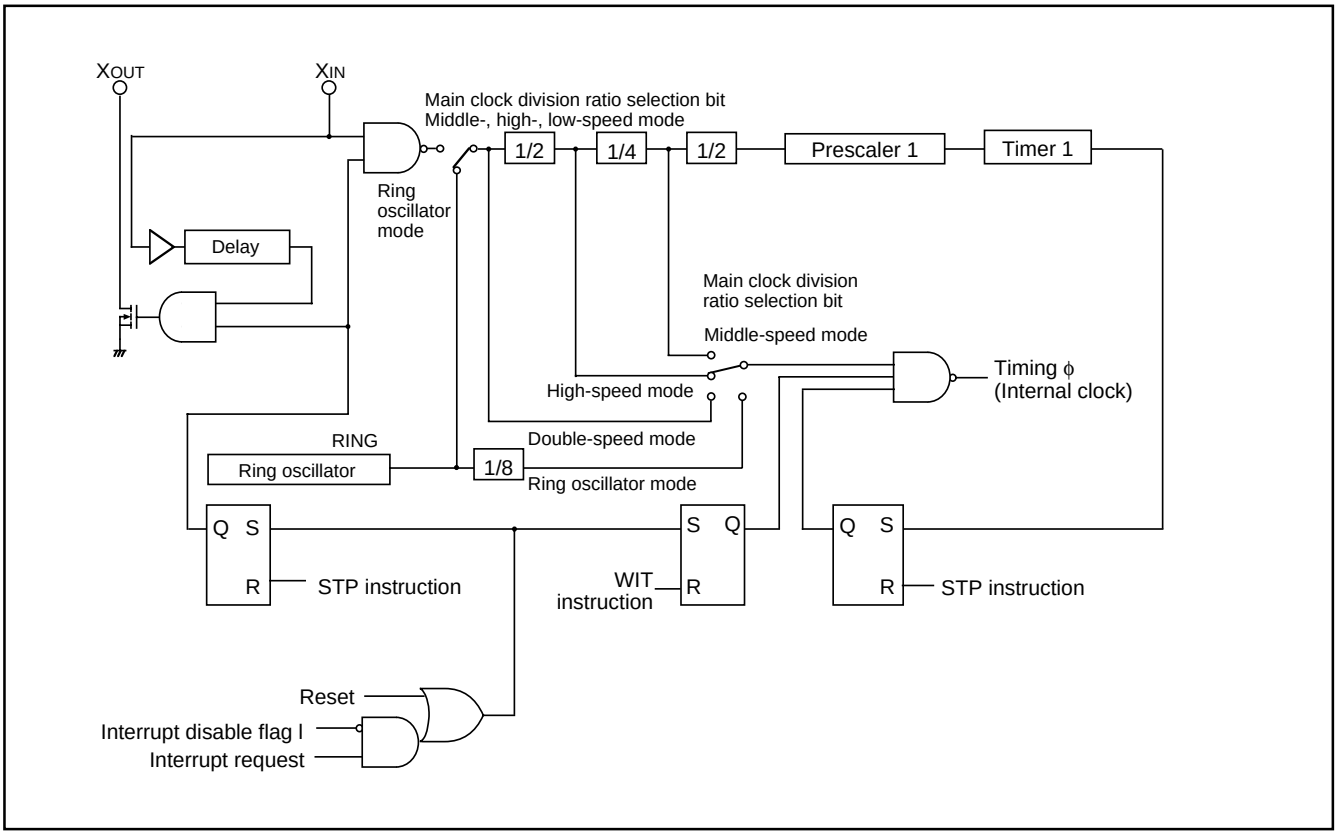


Fig. 51 Block diagram of internal clock generating circuit (for RC oscillation)

● Oscillation stop detection circuit

The oscillation stop detection circuit is used for reset occurrence when a ceramic resonator or an oscillation circuit stops by disconnection. When internal reset occurs, reset because of oscillation stop can be detected by setting “1” to the oscillation stop detection status bit.

Also, when using the oscillation stop detection circuit, a built-in ring oscillator is required.

Figure 52 shows the state transition.

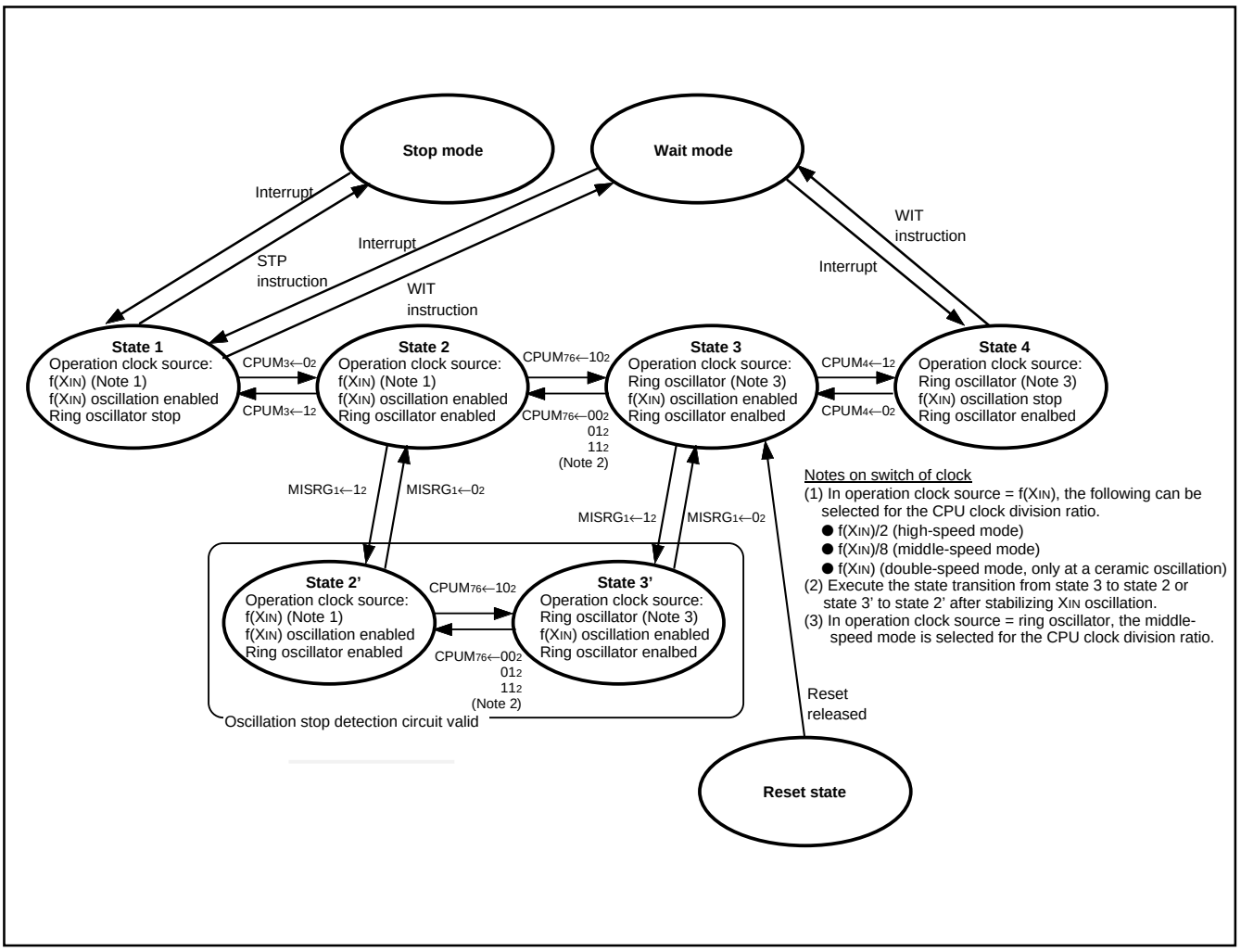


Fig. 52 State transition

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

• For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.

• In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Timers

• When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

• When a count source of timer X, timer Y or timer Z is switched, stop a count of timer X.

Ports

• The values of the port direction registers cannot be read.

That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.

It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.

For setting direction registers, use the LDM instruction, STA instruction, etc.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that f(XIN) is 500kHz or more during A-D conversion.

Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock ϕ is the same as that of the XIN in double-speed mode, twice the XIN cycle in high-speed mode and 8 times the XIN cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)

When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON USE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF to 0.1 μF is recommended.

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (VPP pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 7 Special programming adapter

Package	Name of Programming Adapter
32P4B	PCA7435SPG02
32P6U-A	PCA7435GPG02
36P2R-A	PCA7435FPG02

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 53 is recommended to verify programming.

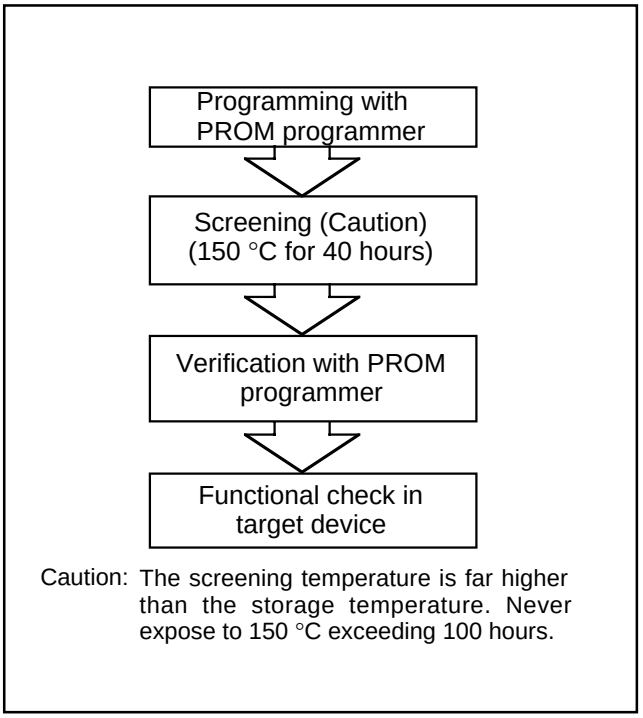


Fig. 53 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

1.7540Group (General purpose)

Applied to: M37540M4-XXXFP/SP/GP, M37540E8FP/SP/GP

Absolute Maximum Ratings (General purpose)

Table 8 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	300 (Note 2)	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Note 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: 200 mW for the 32P6U package product.

Recommended Operating Conditions (General purpose)

Table 9 Recommended operating conditions (1) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(X_{IN}) = 6 MHz (Double-speed mode)	4.5	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (RC)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected) $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)		2.0		V_{CC}	V
V_{IH}	“H” input voltage $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$		0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected) $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)		0		0.8	V
V_{IL}	“L” input voltage $\overline{RESET}$, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	“L” input voltage X_{IN}		0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$				–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$				80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2) $P3_0$–$P3_6$				60	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$				–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$				40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2) $P3_0$–$P3_6$				30	mA

Note 1: V_{CC} = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (General purpose)(continued)

Table 10 Recommended operating conditions (2) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.5 to 5.5 V Double-speed mode			6	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (General purpose)

Table 11 Electrical characteristics (1) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA V_{CC} = 2.2 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{OL}	"L" output voltage $P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 10 mA V_{CC} = 2.2 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1(Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD_1, $SCLK_1$, $SCLK_2$, $SDATA_2$ (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V
R_{OSC}	Ring oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
D_{OSC}	Oscillation stop detection circuit detection frequency	V_{CC} = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes 1: $P1_1$ is measured when the $P1_1/TxD_1$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: RxD_1, $SCLK_1$, $SCLK_2$, $SDATA_2$, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Electrical Characteristics (General purpose)(continued)

Table 12 Electrical characteristics (2) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	One Time PROM version	High-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			5.0	8.0	mA
			High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V Output transistors “off”			0.5	1.5	mA
			Double-speed mode, f(X_{IN}) = 6 MHz Output transistors “off”			6.0	10.0	mA
			Middle-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			2.0	5.0	mA
			Ring oscillator operation mode, V_{CC} = 5 V Output transistors “off”			350	1000	µA
			f(X_{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors “off”			1.6	3.2	mA
			f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.2		mA
			Ring oscillator operation mode, V_{CC} = 5V (in WIT state), functions except timer 1 disabled, Output transistors “off”			150	450	µA
			Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.5		mA
			All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			10	µA
		Mask ROM version	High-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			3.5	6.5	mA
			High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V Output transistors “off”			0.4	1.2	mA
			Double-speed mode, f(X_{IN}) = 6 MHz Output transistors “off”			4.5	8.0	mA
			Middle-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			2.0	5.0	mA
			Ring oscillator operation mode, V_{CC} = 5 V Output transistors “off”			300	900	µA
			f(X_{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors “off”			1.6	3.2	mA
			f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.2		mA
			Ring oscillator operation mode, V_{CC} = 5V (in WIT state), functions except timer 1 disabled, Output transistors “off”			150	450	µA
			Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.5		mA
			All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			10	µA

A-D Converter Characteristics (General purpose)

Table 13 A-D Converter characteristics (One Time PROM version)
(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	Vcc = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	Vcc = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
VOT	Zero transition voltage	Vcc = VREF = 5.12 V	0	5	20	mV
		Vcc = VREF = 3.072 V	0	3	15	mV
VFST	Full scale transition voltage	Vcc = VREF = 5.12 V	5105	5115	5125	mV
		Vcc = VREF = 3.072 V	3060	3069	3075	mV
tCONV	Conversion time				122	tc(XIN)
RLADDER	Ladder resistor			55		kΩ
IVREF	Reference power source input current	VREF = 5.0 V	50	150	200	µA
		VREF = 3.0 V	30	70	120	
II(AD)	A-D port input current				5.0	µA

Table 14 A-D Converter characteristics (Mask ROM version)
(Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	Vcc = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	Vcc = 2.7 to 5.5 V Ta = 25 °C			±1.5	LSB
VOT	Zero transition voltage	Vcc = VREF = 5.12 V	0	15	35	mV
		Vcc = VREF = 3.072 V	0	9	21	mV
VFST	Full scale transition voltage	Vcc = VREF = 5.12 V	5105	5125	5150	mV
		Vcc = VREF = 3.072 V	3060	3075	3090	mV
tCONV	Conversion time				122	tc(XIN)
RLADDER	Ladder resistor			55		kΩ
IVREF	Reference power source input current	VREF = 5.0 V	50	150	200	µA
		VREF = 3.0 V	30	70	120	
II(AD)	A-D port input current				5.0	µA

Timing Requirements (General purpose)

Table 15 Timing requirements (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	80			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	80			ns
$t_{C(CNTR1)}$	$CNTR_1$ input cycle time	2000			ns
$t_{WH(CNTR1)}$	$CNTR_1$ input “H” pulse width	800			ns
$t_{WL(CNTR1)}$	$CNTR_1$ input “L” pulse width	800			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1 input set up time	220			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1 input hold time	100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	200			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Table 16 Timing requirements (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	500			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	230			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	230			ns
$t_{C(CNTR1)}$	$CNTR_1$ input cycle time	4000			ns
$t_{WH(CNTR1)}$	$CNTR_1$ input “H” pulse width	1600			ns
$t_{WL(CNTR1)}$	$CNTR_1$ input “L” pulse width	1600			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1 input set up time	400			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	400			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	400			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Table 17 Timing requirements (3) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	500			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	200			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	200			ns
$t_{C(CNTR0)}$	CNTR0 input cycle time	1000			ns
$t_{WH(CNTR0)}$	CNTR0, INT0, INT1, input “H” pulse width	460			ns
$t_{WL(CNTR0)}$	CNTR0, INT0, INT1, input “L” pulse width	460			ns
$t_{C(CNTR1)}$	CNTR1 input cycle time	8000			ns
$t_{WH(CNTR1)}$	CNTR1 input “H” pulse width	3200			ns
$t_{WL(CNTR1)}$	CNTR1 input “L” pulse width	3200			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	4000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	1900			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	1900			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1 input set up time	800			ns
$t_{h(SCLK1–RxD1)}$	Serial I/O1 input hold time	400			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	4000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	1900			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	1900			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	800			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	800			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Switching Characteristics (General purpose)

Table 18 Switching characteristics (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK1)	Serial I/O1 clock output “H” pulse width	t_C(SCLK1)/2–30			ns
t_{WL}(SCLK1)	Serial I/O1 clock output “L” pulse width	t_C(SCLK1)/2–30			ns
t_d(SCLK1–TxD1)	Serial I/O1 output delay time			140	ns
t_v(SCLK1–TxD1)	Serial I/O1 output valid time	–30			ns
t_r(SCLK1)	Serial I/O1 clock output rising time			30	ns
t_f(SCLK1)	Serial I/O1 clock output falling time			30	ns
t_{WH}(SCLK2)	Serial I/O2 clock output “H” pulse width	t_C(SCLK2)/2–30			ns
t_{WL}(SCLK2)	Serial I/O2 clock output “L” pulse width	t_C(SCLK2)/2–30			ns
t_d(SCLK2–SDATA2)	Serial I/O2 output delay time			140	ns
t_v(SCLK2–SDATA2)	Serial I/O2 output valid time	0			ns
t_r(SCLK2)	Serial I/O2 clock output rising time			30	ns
t_f(SCLK2)	Serial I/O2 clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 19 Switching characteristics (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

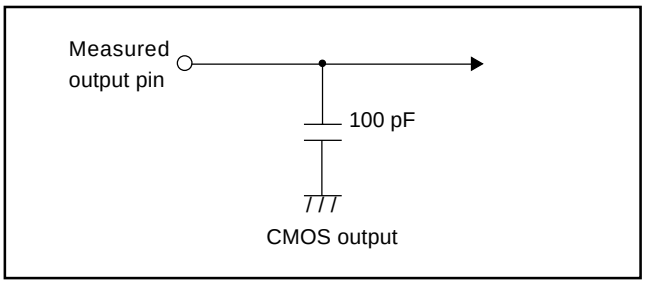
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK1)	Serial I/O1 clock output “H” pulse width	t_C(SCLK1)/2–50			ns
t_{WL}(SCLK1)	Serial I/O1 clock output “L” pulse width	t_C(SCLK1)/2–50			ns
t_d(SCLK1–TxD1)	Serial I/O1 output delay time			350	ns
t_v(SCLK1–TxD1)	Serial I/O1 output valid time	–30			ns
t_r(SCLK1)	Serial I/O1 clock output rising time			50	ns
t_f(SCLK1)	Serial I/O1 clock output falling time			50	ns
t_{WH}(SCLK2)	Serial I/O2 clock output “H” pulse width	t_C(SCLK2)/2–50			ns
t_{WL}(SCLK2)	Serial I/O2 clock output “L” pulse width	t_C(SCLK2)/2–50			ns
t_d(SCLK2–SDATA2)	Serial I/O2 output delay time			350	ns
t_v(SCLK2–SDATA2)	Serial I/O2 output valid time	0			ns
t_r(SCLK2)	Serial I/O2 clock output rising time			50	ns
t_f(SCLK2)	Serial I/O2 clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.

Table 20 Switching characteristics (3) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_C(S_{CLK1})/2–70$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_C(S_{CLK1})/2–70$			ns
$t_d(S_{CLK1}–T_xD_1)$	Serial I/O1 output delay time			450	ns
$t_v(S_{CLK1}–T_xD_1)$	Serial I/O1 output valid time	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			70	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			70	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_C(S_{CLK2})/2–70$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_C(S_{CLK2})/2–70$			ns
$t_d(S_{CLK2}–S_{DATA2})$	Serial I/O2 output delay time			450	ns
$t_v(S_{CLK2}–S_{DATA2})$	Serial I/O2 output valid time	0			ns
$t_r(S_{CLK2})$	Serial I/O2 clock output rising time			70	ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			70	ns
t_r(CMOS)	CMOS output rising time (Note 1)		25	70	ns
t_f(CMOS)	CMOS output falling time (Note 1)		25	70	ns

Note 1: Pin X_{OUT} is excluded.



Switching characteristics measurement circuit diagram (General purpose)

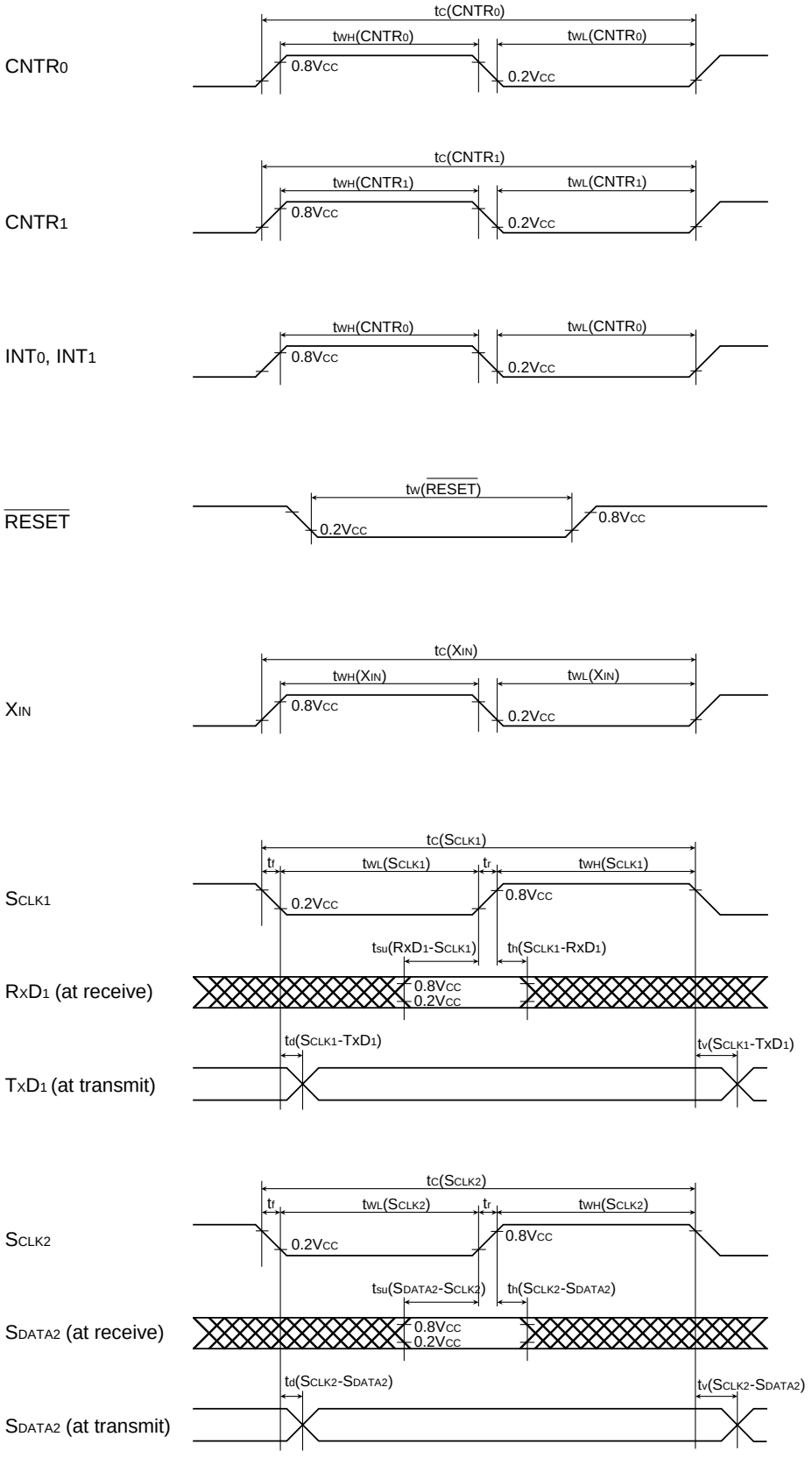


Fig. 54 Timing chart (General purpose)

ELECTRICAL CHARACTERISTICS

2.7540Group (Extended operating temperature version)

Applied to: M37540M4T-XXXFP/GP

Absolute Maximum Ratings (Extended operating temperature version)

Table 21 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	Ta = 25°C	300 (Note)	mW
T_{opr}	Operating temperature		–40 to 85	°C
T_{stg}	Storage temperature		–65 to 150	°C

Note: 200 mW for the 32P6U package product.

Recommended Operating Conditions (Extended operating temperature version)

Table 22 Recommended operating conditions (1) (V_{CC} = 2.4 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 6 MHz (Double-speed mode)	4.5	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (RC)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected) $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)		2.0		V_{CC}	V
V_{IH}	“H” input voltage $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$		0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected) $P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)		0		0.8	V
V_{IL}	“L” input voltage $\overline{RESET}$, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	“L” input voltage X_{IN}		0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$				–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$				80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2) $P3_0$–$P3_6$				60	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$				–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2) $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$				40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2) $P3_0$–$P3_6$				30	mA

Note 1: V_{CC} = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (Extended operating temperature version)(continued)

Table 23 Recommended operating conditions (2) (V_{CC} = 2.4 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
f(X_{IN})	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.5 to 5.5 V Double-speed mode			6	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (Extended operating temperature version)

Table 24 Electrical characteristics (1) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA V_{CC} = 2.4 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{OL}	"L" output voltage $P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 10 mA V_{CC} = 2.4 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1(Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD_1, $SCLK_1$, $SCLK_2$, $SDATA_2$ (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V
R_{OSC}	Ring oscillator oscillation frequency	V_{CC} = 5.0 V, Ta = 25 °C	1000	2000	3000	kHz
D_{OSC}	Oscillation stop detection circuit detection frequency	V_{CC} = 5.0 V, Ta = 25 °C	62.5	125	187.5	kHz

Notes 1: $P1_1$ is measured when the $P1_1/TxD_1$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: $RxD1$, $SCLK_1$, $SCLK_2$, $SDATA_2$, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

Electrical Characteristics (Extended operating temperature version)(continued)

Table 25 Electrical characteristics (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Test conditions		Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	High-speed mode, f(X_{IN}) = 8 MHz Output transistors “off”			3.5	6.5	mA
	High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V Output transistors “off”			0.4	1.2	mA
	Double-speed mode, f(X_{IN}) = 6 MHz, Output transistors “off”			4.5	8.0	mA
	Middle-speed mode, f(X_{IN}) = 8 MHz, Output transistors “off”			2.0	5.0	mA
	Ring oscillator operation mode, V_{CC} = 5 V Output transistors “off”			300	900	µA
	f(X_{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors “off”			1.6	3.2	mA
	f(X_{IN}) = 2 MHz, V_{CC} = 2.4 V (in WIT state), functions except timer 1 disabled, Output transistors “off”			0.2		mA
	Ring oscillator operation mode, V_{CC} = 5V (in WIT state), functions except timer 1 disabled, Output transistors “off”			150	450	µA
	Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.5		mA
	All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
		Ta = 85 °C			10	µA

A-D Converter Characteristics (Extended operating temperature version)

Table 26 A-D Converter characteristics (One Time PROM version)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±1.5	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	15	35	mV
		V_{CC} = V_{REF} = 3.072 V	0	9	21	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5125	5150	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3075	3090	mV
t_{CONV}	Conversion time				122	tc(X_{IN})
R_{LADDER}	Ladder resistor			55		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	70	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Timing Requirements (Extended operating temperature version)

Table 27 Timing requirements (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	80			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	80			ns
$t_{C(CNTR1)}$	$CNTR_1$ input cycle time	2000			ns
$t_{WH(CNTR1)}$	$CNTR_1$ input “H” pulse width	800			ns
$t_{WL(CNTR1)}$	$CNTR_1$ input “L” pulse width	800			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{su(RXD1–SCLK1)}$	Serial I/O1 input set up time	220			ns
$t_{h(SCLK1–RXD1)}$	Serial I/O1 input hold time	100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	200			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Table 28 Timing requirements (2) (V_{CC} = 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	500			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	230			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	230			ns
$t_{C(CNTR1)}$	$CNTR_1$ input cycle time	4000			ns
$t_{WH(CNTR1)}$	$CNTR_1$ input “H” pulse width	1600			ns
$t_{WL(CNTR1)}$	$CNTR_1$ input “L” pulse width	1600			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(RXD1–SCLK1)}$	Serial I/O1 input set up time	400			ns
$t_{h(SCLK1–RXD1)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	400			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	400			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Switching Characteristics (Extended operating temperature version)

Table 29 Switching characteristics (1) (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

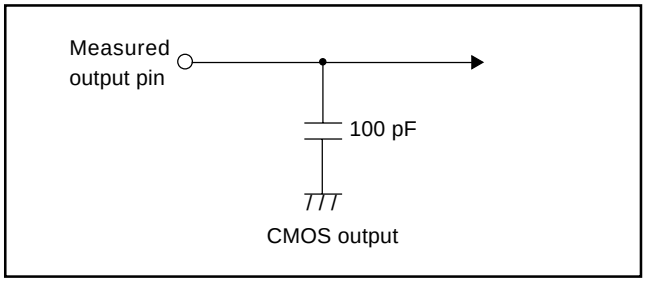
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_C(S_{CLK1})/2–30$			ns
$t_d(S_{CLK1}–TxD_1)$	Serial I/O1 output delay time			140	ns
$t_v(S_{CLK1}–TxD_1)$	Serial I/O1 output valid time	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			30	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_C(S_{CLK2})/2–30$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_C(S_{CLK2})/2–30$			ns
$t_d(S_{CLK2}–S_{DATA2})$	Serial I/O2 output delay time			140	ns
$t_v(S_{CLK2}–S_{DATA2})$	Serial I/O2 output valid time	0			ns
$t_r(S_{CLK2})$	Serial I/O2 clock output rising time			30	ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin X_{OUT} is excluded.

Table 30 Switching characteristics (2) (Vcc = 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output “H” pulse width	$t_C(S_{CLK1})/2–50$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output “L” pulse width	$t_C(S_{CLK1})/2–50$			ns
$t_d(S_{CLK1}–T_xD_1)$	Serial I/O1 output delay time			350	ns
$t_v(S_{CLK1}–T_xD_1)$	Serial I/O1 output valid time	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			50	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			50	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	$t_C(S_{CLK2})/2–50$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	$t_C(S_{CLK2})/2–50$			ns
$t_d(S_{CLK2}–S_{DATA2})$	Serial I/O2 output delay time			350	ns
$t_v(S_{CLK2}–S_{DATA2})$	Serial I/O2 output valid time	0			ns
$t_r(S_{CLK2})$	Serial I/O2 clock output rising time			50	ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin X_{OUT} is excluded.



Switching characteristics measurement circuit diagram (General purpose)

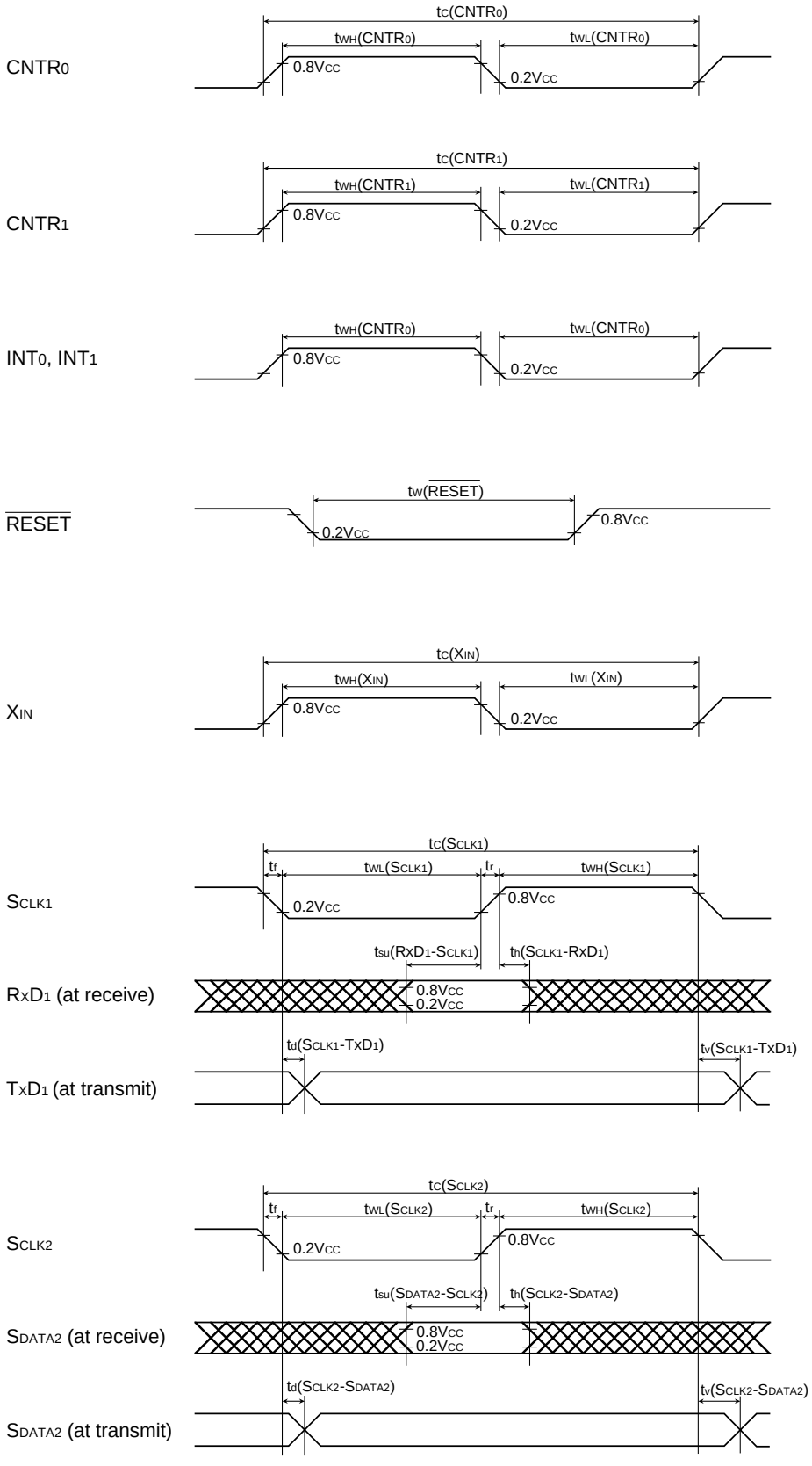


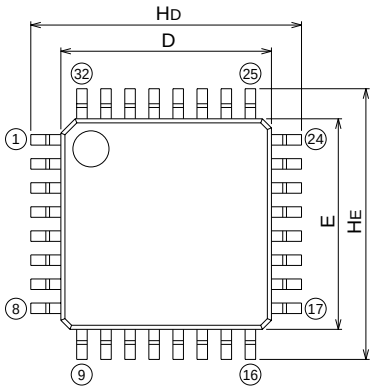
Fig. 55 Timing chart (Extended operating temperature version)

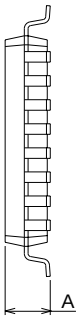
PACKAGE OUTLINE

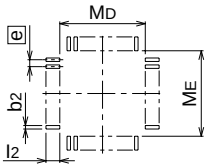
32P6U-A (MMP)

Plastic 32pin 7×7mm body LQFP

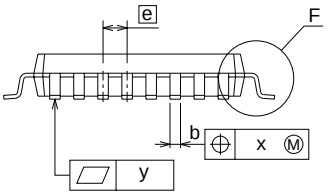
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-0707-0.80	–		Cu Alloy

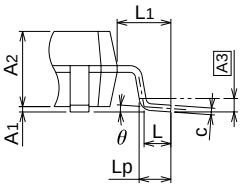






Recommended Mount Pad





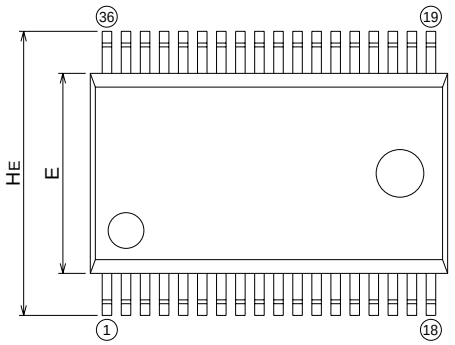
Detail F

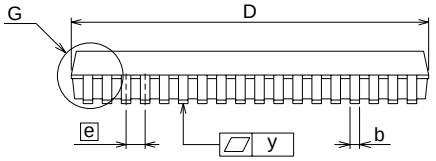
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.32	0.37	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
l2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

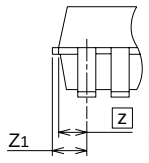
36P2R-A (MMP)

Plastic 36pin 450mil SSOP

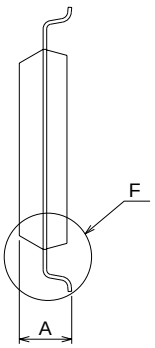
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	–	0.53	Alloy 42

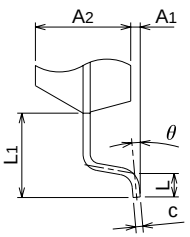




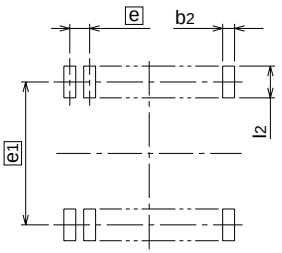


Detail G





Detail F



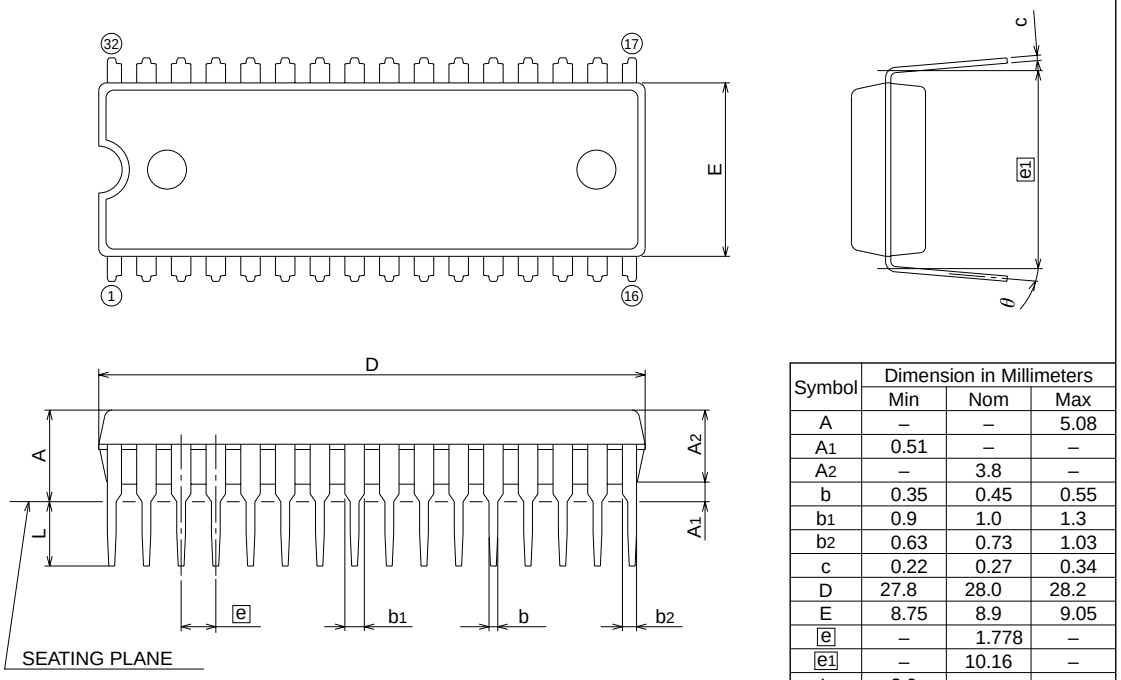
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A1	0.05	–	–
A2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	–	0.8	–
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	–	1.765	–
z	–	0.7	–
Z1	–	–	0.85
y	–	–	0.15
θ	0°	–	10°
b2	–	0.5	–
e1	–	11.43	–
l2	1.27	–	–

32P4B (MMP)

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	–	2.2	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
e_1	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

MITSUBISHI MICROCOMPUTERS

7540 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

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MITSUBISHI ELECTRIC

REVISION DESCRIPTION LIST	7540 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	991122
2.0	Page 1: FEATURES • The minimum instruction execution time revised; 0.34 μs (at 6 MHz oscillation frequency, double-speed mode for the shortest instruction) • Power source voltage added; XIN oscillation frequency at ceramic oscillation , in high-speed mode At 6 MHz.....4.5 to 5.5 V • Power dissipation revised; Mask ROM version.....22.5 mW (standard) One Time PROM version.....30 mW (standard) PIN CONFIGURATION Fig. 1 revised; Package type → 32P6U-A, Product name “M37540M4T-XXXGP” added Page 2: Fig. 2 revised; Product name “M37540M4T-XXXFP” added Page 3: Fig. 4 M37540RSS pin configuration (42S1M) added Page 4: Fig. 5 Functional block diagram revised; Package type → 32P6U Page 7: PIN DESCRIPTION revised; Notes 1 to 3 added Page 8: Package type revised; → 32P6U-A.....0.8 mm-pitch plastic molded LQFP → 36P2R-A.....0.8 mm-pitch plastic molded SSOP Table 2 revised; Package type → 32P6U-A Pages 9 to 11: Structure of CPU added Page 12: Fig. 11 Initial value added, Fig. 12 Description revised Page 16: Table 5 Non-port function of port P0 revised, Notes 2 and 3 added Page 17: Fig. 17 Port P0 revised Page 18: Fig. 18 Note added Page 19: Note revised Page 20: Fig. 20 Initial values added, Interrupt enable bit of ICON1; Note added	010115

REVISION DESCRIPTION LIST	7540 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
2.0	(continued) Page 21: Fig. 21 Port $P0_0$ key-on wakeup selection bit added Pages 22 to 30: Description of timers revised all Page 31: Fig. 25 to Fig. 27 Initial values added Page 33: Fig. 29 Reference of Figure revised → Fig. 50, 51 Page 36: Description of SIO1STS revised; "All bits" → "Bits 0 to 6" Description of UARTCON revised; "$P1_2$/S_{CLK1}" pin eliminated Notes added Page 37: Fig. 34 Initial value added Page 38: Fig. 35 Initial value added Page 39: Fig. 37 Note revised Page 40: Fig. 38 Initial value added Page 41: Fig. 42 Initial value added Page 42: Description in the case of 6 MHz added Page 43: Fig. 45 Contents of (7), (8) revised Page 45: Fig. 49 Functions of b1 and b7 revised, Initial value added Page 46: Fig. 50 A resistor of X_{OUT} pin eliminated Page 47: Description of oscillation stop detection circuit added, Fig. 52 revised Page 48: Notes on Ports revised Pages 50 to 68: Electrical characteristics revised all Page 69: Package type revised; 32P6U-A	010115