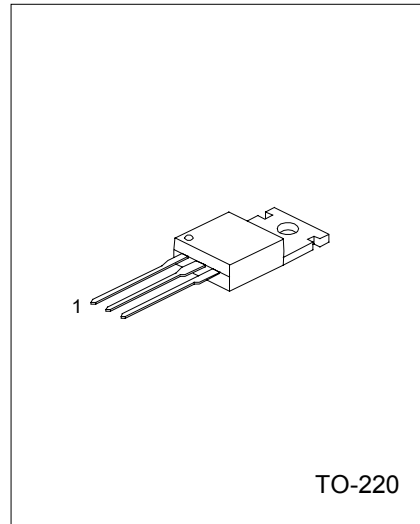


## SCRs

### DESCRIPTION

The UTC US108S/N is suitable to fit all modes of control, found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, inrush current limiting circuits, capacitive discharge ignition and voltage regulation circuits.



TO-220

1: CATHODE    2: ANODE    3: GATE

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING		UNIT
		US108S	US108N	
Repetitive peak off-state voltages US108S/N-4 US108S/N-6 US108S/N-8	V <sub>DRM</sub> V <sub>RRM</sub>	400 600 800		V
RMS on-state current (180° conduction angle) (T <sub>c</sub> = 110°C)	I <sub>T(RMS)</sub>	8		A
Average on-state current (180° conduction angle) (T <sub>c</sub> = 110°C)	I <sub>T(AV)</sub>	5		A
Non repetitive surge peak on-state current (T <sub>j</sub> = 25°C) tp=8.3ms tp=10ms	I <sub>TSM</sub>	73 70	100 95	A
I <sup>2</sup> t Value for fusing (tp = 10 ms ,T <sub>j</sub> = 25°C)	I <sup>2</sup> t	24.5	45	A <sup>2</sup> S
Critical rate of rise of on-state current (I <sub>G</sub> = 2 x I <sub>GT</sub> , tr ≤ 100 n s, T <sub>j</sub> = 125°C, F = 60 Hz)	dI/dt	50		A/μs
Peak gate current (tp=20μs, T <sub>j</sub> = 125°C)	I <sub>GM</sub>	4		A
Maximum peak reverse gate voltage	V <sub>RGM</sub>		5	V
Average gate power dissipation (T <sub>j</sub> = 125°C)	P <sub>G(AV)</sub>	1		W
Storage junction temperature range	T <sub>stg</sub>	-40 ~ +150		°C
Operating junction temperature range	T <sub>j</sub>	-40 ~ +125		°C

## UTC US108S(SENSITIVE) ELECTRICAL CHARACTERISTICS

(Tj=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 140Ω		200	μA
Gate trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 140Ω		0.8	V
Gate non-trigger voltage	V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 kΩ, R <sub>GK</sub> = 220Ω T <sub>J</sub> = 125°C	0.1		V
Reverse gate voltage	V <sub>RG</sub>	I <sub>RG</sub> = 10 μA	8		V
Holding Current	I <sub>H</sub>	I <sub>T</sub> = 50 mA, R <sub>GK</sub> = 1 kΩ		5	mA
Latching Current	I <sub>L</sub>	I <sub>G</sub> = 1 mA, R <sub>GK</sub> = 1 kΩ		6	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V <sub>D</sub> = 65 % V <sub>DRM</sub> , R <sub>GK</sub> = 220 Ω T <sub>J</sub> = 125°C	5		V/μs
On-state voltage	V <sub>TM</sub>	I <sub>TM</sub> = 16A, t <sub>p</sub> = 380 μs T <sub>J</sub> = 25°C		1.6	V
Threshold Voltage	V <sub>t0</sub>	T <sub>J</sub> = 125°C		0.85	V
Dynamic Resistance	R <sub>d</sub>	T <sub>J</sub> = 125°C		46	mΩ
Off-state Leakage Current	I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> , R <sub>GK</sub> = 220 Ω T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C		5 1	μA mA

## UTC US108N(STANDARD) ELECTRICAL CHARACTERISTICS

(Tj=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX.	UNIT
Gate trigger Current	I <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 33Ω	2	15	mA
Gate trigger Voltage	V <sub>GT</sub>	V <sub>D</sub> = 12 V, R <sub>L</sub> = 33Ω		1.3	V
Gate non-trigger voltage	V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 kΩ, T <sub>J</sub> = 125°C	0.2		V
Holding Current	I <sub>H</sub>	I <sub>T</sub> = 100 mA, Gate open		30	mA
Latching Current	I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>		70	mA
Circuit Rate Of Change Of off-state Voltage	dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> , Gate open, T <sub>J</sub> = 125°C	150		V/μs
On-state voltage	V <sub>TM</sub>	I <sub>TM</sub> = 16A, t <sub>p</sub> = 380 μs, T <sub>J</sub> = 25°C		1.6	V
Threshold Voltage	V <sub>t0</sub>	T <sub>J</sub> = 125°C		0.85	V
Dynamic Resistance	R <sub>d</sub>	T <sub>J</sub> = 125°C		46	mΩ
Off-state Leakage Current	I <sub>DRM</sub> I <sub>RRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C		5 2	μA mA

## THERMAL RESISTANCES

PARAMETER	SYMBOL	VALUE	UNIT
Junction to case (DC)	R <sub>th(j-c)</sub>	20	K/W
Junction to ambient (DC)	R <sub>th(j-a)</sub>	60	K/W

Fig.1:Maximum average power dissipation vs average on-state current

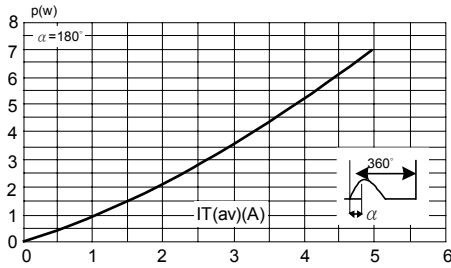


Figure.2:Average and D.C. on-state current vs case temperature

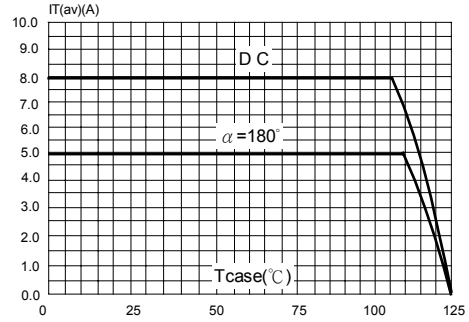


Figure.3: Relative variation of thermal impedance juncto to case vs pulse duration

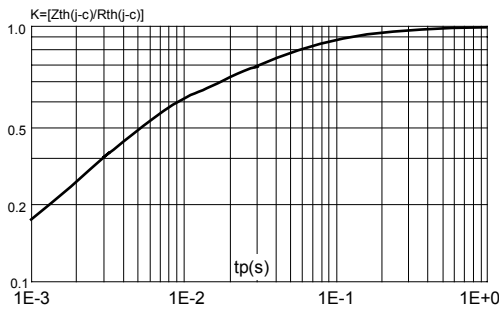


Figure.4:Relative variation of gate trigger current,holding current and latching vs junction temperature .(US108S)

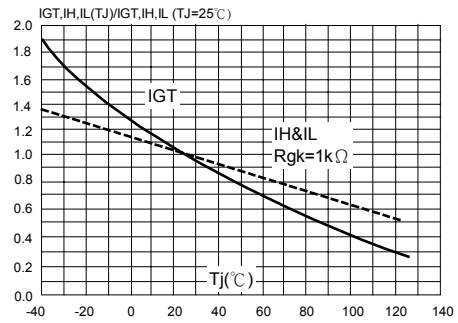


Figure.4-2:Relative variation of gate trigger current,holding current and latching vs junction temperature .(US108N)

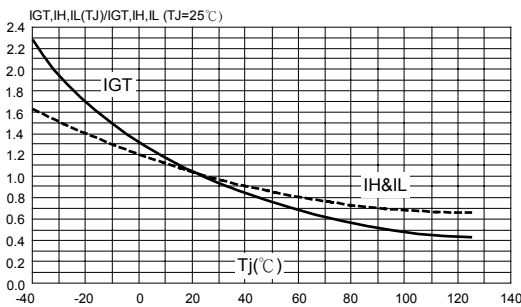


Figure.5:Relative variation of holding current vs gate-cathode resistance(typical values) (US108S)

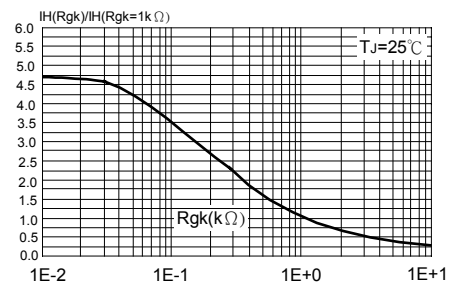


Fig.6: Relative variation of dV/dt immunity vs gate-cathode resistance (typical values) (US108S)

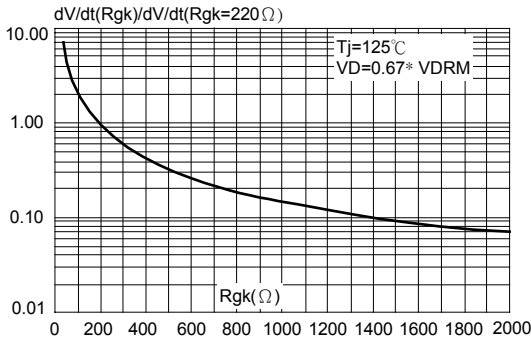


Fig.7: Relative variation of dV/dt immunity vs gate-cathode resistance (typical values) (US108S)

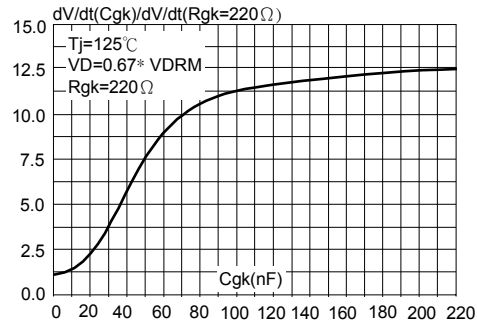


Figure.8: Surge peak on-state current vs number of cycles.

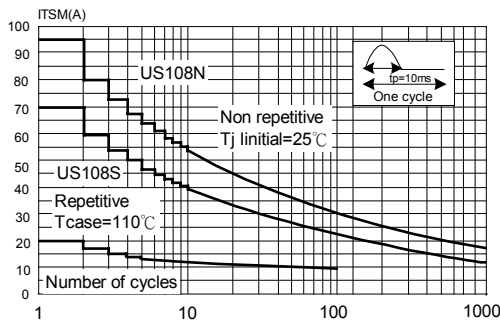


Fig.9: Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10ms$ , and corresponding values of  $I^2t$ .

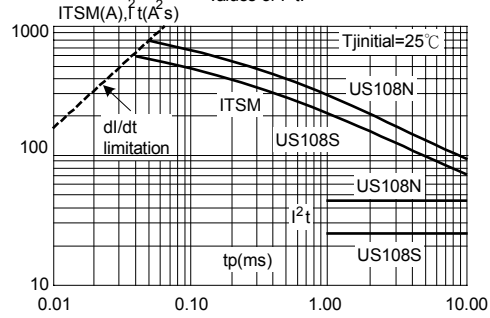
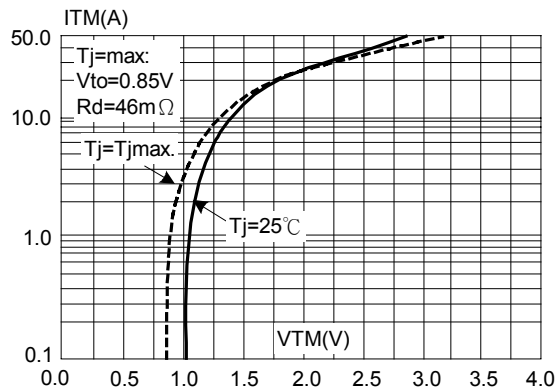


Fig.10: On-state characteristics (maximum values).



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