microelectronics group

Lucent Technologies
Bell Labs Innovations

LU3X34FT
Quad 3 V 10/100 Ethernet Transceiver TX/FX

Overview

The LU3X34FT is a fully integrated 4-port
10/100 Mbits/s physical layer device with transceiver.
This part was designed specifically for
10/100 Mbits/s switches. These applications typically
require stringent functionality in addition to very tight
board space, power, and cost requirements. The
LU3X34FT supports MII interface. The LU3X34FT
was designed to conform fully with all pertinent spec-
ifications, from the ISO/IEC 11801 and EIA/TIA 568
cabling guidelines to ANSI X3.263 TP-PMD to
IEEE* 802.3 Ethernet specifications.

Features

- 4-port, single-chip integrated physical layer and
  transceivers for 10Base-T, 100Base-TX, or
  100Base-FX functions

- *IEEE* 802.3 compatible 10Base-T and 100Base-T
  physical layer interface and ANSI X3.263 TP-PMD
  compatible transceiver

- Interface support for MII

- Autonegotiation pin configurability on a per-port
  basis

- Combined TX, 10Base-T, FX drivers, receivers,
  and signal detect circuit

- Built-in, analog 10 Mbits/s receive filter, removing
  the need for external filters

- Built-in 10 Mbits/s transmit filter

- 10 Mbits/s PLL exceeding tolerances for both pre-
  amble and data jitter

- 100 Mbits/s PLL, combined with the digital adap-
  tive equalizer, robustly handles variations in rise-
  fall time, excessive attenuation due to channel
  loss, duty-cycle distortion, crosstalk, and baseline
  wander

- Transmit rise-fall time manipulated to provide lower
  emissions, amplitude fully compatible for proper
  interoperability

- Programmable scrambler seed for better FCC
  compliancy

- *IEEE* 802.3u Clause 28 compliant autonegotiation
  for full 10 Mbits/s and 100 Mbits/s control

- Extended management support with interrupt
  capabilities

- PHY MIB support

- Low-power, 480 mA max

- Low-cost, 160 PQFP packaging

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  Electronics Engineers, Inc.

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124 RXCLK_0
123 IOVDD2
122 IOGND2
121 1OFD_1
1OFD_2

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160 PQFP

Left side pins (1–40):

Pin	Signal
1	10FD_0
2	RXVDD0
3	RX+_0
4	RX−_0
5	RXGND0
6	REF100_0
7	TX+_0
8	TX−_0
9	TXVDD0
10	TXVDD1
11	TX−_1
12	TX+_1
13	REF100_1
14	RXGND1
15	RX−_1
16	RX+_1
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35	REF100_3
36	RXGND3
37	RX−_3
38	RX+_3
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40	10FD_3

Right side pins (120–81):

Pin	Signal
120	TXCLK_1
119	TXEN_1
118	TXD_1[0]
117	TXD_1[1]
116	TXD_1[2]
115	TXD_1[3]
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113	IO_GND3
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111	CRS_1/PHY_AD[2]
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109	RXDV_1
108	RXD_1[0]
107	DIGVDD1
106	DIGGND1
105	RXD_1[1]
104	RXD_1[2]
103	RXD_1[3]
102	RXER_1
101	RXCLK_1
100	IOVDD4
99	IOGND4
98	RXCLK_2
97	RXER_2
96	RXD_2[3]
95	DIGVDD2
94	DIGGND2
93	RXD_2[2]
92	RXD_2[1]
91	RXD_2[0]
90	RXDV_2
89	COL_2/100FD_2
88	CRS_2/PHY_AD[3]
87	TXER_2
86	TXD_2[3]
85	TXD_2[2]
84	TXD_2[1]
83	TXD_2[0]
82	TXEN_2
81	TXCLK_2

Bottom side pins (41–80):

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42 PAUSE
43 TPTXTR
44 ISOLATE
45 ANEN_2/SD+_2/LED100_2
46 10HD_2/SD−_2/LEDFD_2
47 100HD_2/LEDFD_2
48 FOSEL_2/LEDLNK_2
49 LEDGND2
50 LEDVDD2
51 ANEN_3/SD+_3/LED100_3
52 10HD_3/SD−_3/LEDFD_3
53 100HD_3/LEDFD_3
54 FOSEL_3/LEDLNK_3
55 TXEN_3
56 TXD_3[0]
57 TXD_3[1]
58 TXD_3[2]
59 TXD_3[3]
60 TXER_3
61 COL_3/100FD_3
62 CRS_3/PHY_AD[4]
63 MDC
64 MDIO
65 SUBGND2
66 HSVDD2
67 HSGND2
68 TMVDD1
69 IOGND6
70 TXCLK_3
71 IOVDD6
72 RXDV_3
73 RXD_3[0]
74 RXD_3[1]
75 RXD_3[2]
76 RXD_3[3]
77 RXER_3
78 RXCLK_3
79 IOGND5
80 IOVDD5

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Figure 2. Pin Diagram

Pin Descriptions

Table 1. Twisted-Pair Magnetic Interface

Pin No.	Pin Name	I/O	Pin Description
7, 12, 29, 34 8, 11, 30, 33	TX+_[0:3] TX–_[0:3]	O	**Transmit Driver Pairs**. These pins are used to send 100Base-T MLT-3 signals across category 5 UTP, 10Base-T Manchester signals across category 3/5 UTP cable in twisted-pair operation, or PECL data in fiber mode.
3, 16, 25, 38 4, 15, 26, 37	RX+_[0:3] RX–_[0:3]	I	**Receive Pair**. These pins receive 100Base-T MLT-3 data, 10Base-T Manchester data from the UTP cable in twisted-pair mode, or PECL data in fiber mode.

Table 2. Twisted-Pair Transceiver Control/Transmitter Control

Pin No.	Pin Name	I/O	Pin Description
6, 13, 28, 35	REF100[0:3]	I	**Reference Pin for 100 Mbits/s Twisted-Pair Driver**. The value of the connected resistor is **TBD** Ω.
23	REF10	I	**Reference Pin for 10 Mbits/s Twisted-Pair Driver**. The value for the connected resistor is **TBD** Ω.
160	ER	I	**Transmit Driver Edge Rate Control**. When set to 1, the rise time of the transmit data will be less than **TBD** ns. This pin is latched at powerup and reset.
43	TPTXTR	I	**Network Interface Tri-State Control**. When high, the transmit drivers for all four ports are tri-stated.

Table 3. MII Interface

Pin No.	Pin Name	I/O	Pin Description
1, 122, 121, 40	10FD[0:3]	I	**10 Mbits/s Full-duplex Capability Configuration Input**. It is latched into bit 6 of register 04h (autonegotiation ability register) at reset. It is also used to configure a port to 10 Mbits/s full-duplex mode if autonegotiation is disabled. Each of these pins has an internal 40 kΩ pull-up.
135, 110, 89, 61	COL_[0:3]/ 100FD_[0:3]	I/O	**100 Mbits/s Full-duplex Capability Configuration Input**. During reset, it is latched into bit 8 of register 04h (autonegotiation ability register) at reset. It is also used to configure a port to 100 Mbits/s full-duplex mode if autonegotiation is disabled. Each of these pins has an internal 40 kΩ pull-up. After reset: In half-duplex mode, these pins are an output indicating collision status.
138, 120, 81, 70	TXCLK_[0:3]	O	**MII Transmit Clock For Ports 0 Through 2**. Its frequency is 2.5 MHz in 100 Mbit mode, 25 MHz in 10 Mbit nibble mode, and 10 MHz in 10 Mbit serial mode.
146, 119, 82, 55	TXEN_[0:3]	I	**Transmit Enable**. Ports 0 through 3.

Pin Descriptions (continued)

Table 3. MII Interface (continued)

Pin No.	Pin Name	I/O	Pin Description
142, 143, 144, 145	TXD_0[3:0]	I	**MII Transmit Data for Port 0**.
115, 116, 117, 118	TXD_1[3:0]	I	**MII Transmit Data for Port 1**.
86, 85, 84, 83	TXD_2[3:0]	I	**MII Transmit Data for Port 2**.
59, 58, 57, 56	TXD_3[3:0]	I	**MII Transmit Data for Port 3**.
141, 112, 87, 60	TXER_[0:3]	I	**Transmit Error Signal for Each Port**.
127, 128, 129, 133	RXD_0[3:0]	O	**MII Receive Data for Port 0**.
103, 104, 105, 108	RXD_1[3:0]	O	**MII Receive Data for Port 1**.
96, 93, 92, 91	RXD_2[3:0]	O	**MII Receive Data for Port 2**.
76, 75, 74, 73	RXD_3[3:0]	O	**MII Receive Data for Port 3 in Switch Mode**.
102, 97, 77, 126	RXER_[0:3]	O	**Receive Error Condition for Ports 0—3**.
62	CRS_3/ PHY_AD[4]	I/O	**PHY Address 4**. During reset, this pin is input pin for PHY_ADDRESS[4] configuration. This pin has an internal 40 kΩ pull-down. **CRS Output**. After reset, this is the CRS output for port 3. It is asserted only during receive activity.
88	CRS_2/ PHY_AD[3]	I/O	**PHY Address 3**. During reset, this is an input pin for PHY_ADDRESS[3] configuration. This pin has an internal 40 kΩ pull-down. **CRS Output**. After reset, this is the CRS output for port 2. It is asserted only during receive activity.
111	CRS_1/ PHY_AD[2]	I/O	**PHY Address 2**. During reset, this is an input pin for PHY_ADDRESS[2] configuration. This pin has an internal 40 kΩ pull-down. **CRS Output**. After reset, this is the CRS output for port 1. It is asserted only during receive activity.
136	CRS_0/ SERSEL	I/O	**Serial Select**. During reset, this is an input pin, serial select for 10 Mbits/s mode. This pin has an internal 40 kΩ pull-down. **CRS Output**. After reset, this is the CRS output for port 0. It is asserted only during receive activity.
134, 109, 90, 72	RXDV_[0:3]	O	**Receive Data Valid Signal for Ports 0—3**.
125, 101, 98, 78	RXCLK_[0:3]	O	**Receive Clock Output for Ports 0—3**. Its frequency is 25 MHz in 100 Mbit mode, 2.5 MHz in 10 Mbit nibble mode, and 10 MHz in 10 Mbit serial mode.
64	MDIO	I/O	**Management Data Port**. An external resistive pull-up is needed on this pin.
63	MDC	I	**Management Clock**. Max clock rate is 2.5 MHz.

Pin Descriptions (continued)

Table 4. Autonegotiation/LED Configuration

Pin No.	Pin Name	I/O	Pin Description
148, 154, 45, 51	ANEN_[0:3] LED100_[0:3] SD+_[0:3]	I/O	**Autonegotiation Enable**. During reset, if the FOSEL pin detects logic low during reset, these are input pins to configure ports 0—3 to enable autonegotiation and sets bit 12 in register 0. Each of these pins has an internal 40 kΩ pull-up. **Speed LED Output**. After reset and in twisted-pair mode, these are LED outputs indicating 100 Mbits/s line speed for ports 0—3. **Signal Detect Input**. After reset and in fiber mode, these pins are signal detect + inputs.
149, 155, 46, 52	10HD_[0:3] LEDFD_[0:3] SD–_[0:3]	I/O	**10 Mbits/s Half-duplex**. During reset, these are 10 Mbits/s half-duplex configuration inputs for ports 0—3. The logic level of this pin is latched into bit 5 of register 4 at reset. If autonegotiation is disabled, this pin also affects the initial speed and duplex registers of register 0. Each of these pins has an internal 40 kΩ pull-up. **LED Full-Duplex Status**. After reset and in twisted-pair mode, these are the LED outputs indicating full-duplex status for ports 0—3. **Signal Detect Input**. After reset and in fiber mode, these pins are the signal detect input from the fiber transceiver.
150, 156, 47, 53	100HD_[0:3] LEDACT_[0:3]	I/O	**100 Mbit Half-duplex**. 100 Mbit half-duplex configuration inputs for ports 0—3. During reset, the logic level of this pin is latched into bit 7 of register 4 at reset. If autonegotiation is disabled, this pin also affects the initial speed and duplex registers of register 0. Each of these pins has an internal 40 kΩ pull-up. **LED Activity**. After reset and in twisted-pair mode, these are the LED outputs indicating transmit or receive activity for ports 0—3. **Signal Detect Input**. After reset and in fiber mode, these pins are the signal detect input from the fiber transceiver.
151, 157, 48, 54	FOSEL [0:3] LEDLNK_[0:3]	I/O	**FOSEL**. These are input pins to configure ports 0—3 into fiber-optic mode. Each of these pins has an internal 40 kΩ pull-down. **LED Link Status**. After reset, these are the LED outputs indicating link status for ports 0—3.

Pin Descriptions (continued)

Table 5. Special Mode Configurations

Pin No.	Pin Name	I/O	Pin Description
42	PAUSE	I	**Pause**. During reset: Logic level of this pin is latched into register 4, bit 10 of all four ports. It is used for informing the autonegotiation link partner that the MAC sublayer has pause/flow control capability of operation when set in full-duplex mode. This must **not** be set to 1 unless FD is also set. A weak resistive pull-up/pull-down is required to program this function.
41	INTZ	I/O	**Open-Drain Output**. This pin has open-drain output. Its active-low output indicates interrupt condition.
158	TESTMSEL	I	**Test Mode Select**. To allow parallel access to this register. Users should connect it to low. 1 = test mode. 0 = normal operation.
44	ISOLATE	I	**Isolate**. This is an input pin that controls MII isolate mode. In isolate mode, all MII inputs are ignored and MII outputs are tri-stated.

Table 6. Clock and Chip Reset

Pin No.	Pin Name	I/O	Pin Description
147	CLK_25	I	**25 MHz Reference Clock Input**.
159	RSTZ	I	**Reset**. A hardware reset is accomplished by applying a negative pulse, with a duration of at least 1 ms.

Pin Descriptions (continued)

Table 7. Power and Ground

Plane	Vcc Pin		Associated Ground Pin	
	Name	**Pin No.**	**Name**	**Pin No.**
RX Analog	RXV$_{DD}$0	2	RXGND0	5
	RXV$_{DD}$1	17	RXGND1	14
	RXV$_{DD}$2	24	RXGND2	27
	RXV$_{DD}$3	39	RXGND3	36
			REFGND	18
TX Analog	TXV$_{DD}$0	9	—	—
	TXV$_{DD}$1	10		
	TXV$_{DD}$2	31		
	TXV$_{DD}$3	32		
CS	CSV$_{DD}$10	19	CSGND10	20
	CSV$_{DD}$100	22	CSGND100	21
Digital	DIGV$_{DD}$1	107	DIGGND1	106
	DIGV$_{DD}$2	95	DIGGND2	94
	TMV$_{DD}$	130	TMGND1	68
	IOV$_{DD}$1	140	IOGND1	139
	IOV$_{DD}$2	124	IOGND2	123
	IOV$_{DD}$3	114	IOGND3	113
	IOV$_{DD}$4	100	IOGND4	99
	IOV$_{DD}$5	80	IOGND5	79
	IOV$_{DD}$6	71	IOGND6	69
	HSV$_{DD}$1	132	HSGND1	131
	HSV$_{DD}$2	66	HSGND2	67
	LEDV$_{DD}$1	153	LEDGND1	152
	LEDV$_{DD}$2	50	LEDGND2	49
			SUBGND1	137
			SUBGND2	65

Functional Description

The LU3X34FT integrates four 100Base-X physical sublayer (PHY), 100Base-TX physical medium dependent (PMD) transceiver, and four complete 10Base-T modules into a single-chip for both 10 Mbits/s and 100 Mbits/s Ethernet operation. It also supports 100Base-FX operation through external fiber-optic transceivers. This device provides an *IEEE* 802.3u compliant media independent interface (MII) to communicate between the physical signaling and the medium access control (MAC) layers for both 100Base-X and 10Base-T operations. The device is capable of operating in either full-duplex mode or half-duplex mode in either 10 Mbits/s or 100 Mbits/s operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip autonegotiation logic.

The 10Base-T section of the device consists of the 10 Mbits/s transceiver module with filters and a Manchester ENDEC module.

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sublayer (PCS)

- 100Base-X physical medium attachment (PMA)

- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module (CSM)

- MII registers

- *IEEE* 802.3u autonegotiation

Each of these functional blocks is described below.

Media Independent Interface (MII)

The LU3X34FT implements *IEEE* 802.3u Clause 22 compliant MII interface as described below.

Interface Signals

Transmit Data Interfaces. Each MII transmit data interface comprises seven signals: TXD[3:0] are the nibble size data path, TXEN signals the presence of data on TXD, TXER indicates substitution of data with the HALT symbol, and TXCLK carries the transmit clock that synchronizes all the transmit signals. TXCLK is supplied by the on-chip clock synthesizer.

Receive Data Interfaces. Each receive data interface also comprises seven signals: RXD[3:0] are the nibble size data path, RXDV signals the presence of data on RXD, RXER indicates the validity of data, and RXCLK carries the receive clock. Depending upon the operation mode, RXCLK signal is generated by the clock recovery module of either the 100Base-X or 10Base-T receiver.

Status Interface. Two status signals, COL and CRS, are generated in each of the four channels to indicate collision status and carrier sense status to the MAC. COL is asserted asynchronously whenever the respective channel of LU3X34FT is transmitting and receiving at the same time in a half-duplex operation mode. CRS is asserted asynchronously whenever there is activity on either the transmitter or the receiver. In full-duplex mode, CRS is asserted only when there is activity on the receiver.

Operation Modes

Each channel of the LU3X34FT supports three operation modes and an isolate mode as described below.

100 Mbits/s Mode. For 100 Mbits/s operation, the MII operates in nibble mode with a clock rate of 25 MHz. In normal operation, the MII data at RXD[3:0] and TXD[3:0] are 4 bits wide. In bypass mode (either BYP_4B5B or BYP_ALIGN option selected), the MII data takes the form of 5-bit code-groups. The least significant 4 bits appear on TXD[3:0] and RXD[3:0] as usual, and the most significant bits (TXD[4] and RXD[4]) appear on the TXER and RXER pins, respectively.

10 Mbits/s Nibble Mode. For 10 Mbits/s nibble mode operation, the TXCLK and RXCLK operate at 2.5 MHz. The data paths are 4 bits wide using TXD[3:0] and RXD[3:0] signal lines.

10 Mbits/s Serial Mode. This mode is selected by strapping the SERSEL pin (pin 136) to logic high level during powerup or reset. When operating in this mode, the LU3X34FT accepts NRZ serial data on the TXD[0] input and provides NRZ serial data output on RXD[0] with a clock rate of 10 MHz. The unused MII inputs and outputs (TXD[3:1] and RXD[3:1]) are ignored during serial mode. The PCS control signals, CRS and COL, continue to function normally. RXDV, RXER, and TXER signals are also ignored.

MII Isolate Mode. The LU3X34FT implements an MII isolate mode that is controlled by bit 10 of each one of the four control registers (register 0h). At reset, LU3X34FT will initialize this bit to the logic level of the ISOLATE pin (pin 44). After reset, content of this register follows the logic level of the ISOLATE pin. Setting the bit to a 1 will also put the port in MII isolate mode.

Functional Description (continued)

When in isolate mode, the specified port on the LU3X34FT does not respond to packet data present at TXD[3:0], TXEN, and TXER inputs and presents a high impedance on the TXCLK, RXCLK, RXDV, RXER, RXD[3:0], COL, and CRS outputs. The LU3X34FT will continue to respond to all management transactions while the PHY is in isolate mode.

Serial Management Interface

The serial management interface (SMI) is used to both obtain status from and to configure the PHY. This mechanism corresponds to the MII specifications for 100Base-X (Clause 22), and supports registers 0 through 6. Additional vendor-specific registers are implemented within the range of 16 to 31. All the registers are described in the register section.

Management Register Access. The SMI consists of two pins, management data clock (MDC) and management data input/output (MDIO). The LU3X34FT is designed to support an MDC frequency ranging up to the *IEEE* specification of 2.5 MHz. The MDIO line is bidirectional and may be shared by up to 32 devices.

The MDIO pin requires a pull-up resistor which, during IDLE and turnaround periods, will pull MDIO to a logic one state. Each MII management data frame is 64 bits long. The first 32 bits are preamble consisting of 32 contiguous logic one bits on MDIO and 32 corresponding cycles on MDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates READ from MII management register operation, and <01> indicates WRITE to MII management register operation. The next two fields are PHY device address and MII management register address. Both of them are 5 bits wide and the most significant bit is transferred first.

During READ operation, a 2-bit turnaround (TA) time spacing between register address field and data field is provided for the MDIO to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the MII management registers of the LU3X34FT.

The LU3X34FT supports a preamble suppression mode as indicated by a 1 in bit 6 of the basic mode status register (BMSR, address 01h). If the station management entity (i.e., MAC or other management controller) determines that all PHYs in the system support preamble suppression by reading a 1 in this bit, then the station management entity need not generate preamble for each management transaction. The

LU3X34FT requires a single initialization sequence of 32 bits of preamble following powerup/hardware reset. This requirement is generally met by the mandatory pull-up resistor on MDIO or the management access made to determine whether preamble suppression is supported. While the LU3X34FT will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required as specified in *IEEE* 802.3u.

The PHY device address for LU3X34FT is stored in the PHY address register (register address 19h). Upper 3 bits of the PHY address are initialized by the three I/O pins designated as PHY_AD[4:2] during powerup or hardware reset and can be changed afterward by writing into register address 19h. The lower 2 bits of the PHY address are initialized to the port number of the PHY during powerup or hardware reset.

MDIO Interrupt. The LU3X34FT implements interrupt capability that can be used to notify the management station of certain events. Interrupt requested by any of the four PHYs is combined in this pin. It generates an active-low interrupt on the INTZ output pin whenever one of the interrupt status registers (register address 1Eh) becomes set while its corresponding interrupt mask register (register address 1Dh) is unmasked. Reading the interrupt status register (register 1Eh) shows the source of the interrupt and clears the interrupt output signal.

In addition to the INTZ pin, the LU3X34FT can also support the interrupt scheme used by the TI Thunder-LAN MAC. This option can be enabled by setting bit 11 of register 17h. Whenever this bit is set, the interrupt is signaled through the INTZ pin and embedded in the MDIO signal.

100Base-X Module

The LU3X34FT implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 3. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100 Mbits/s PHY loopback is included for diagnostic purposes.

Functional Description (continued)
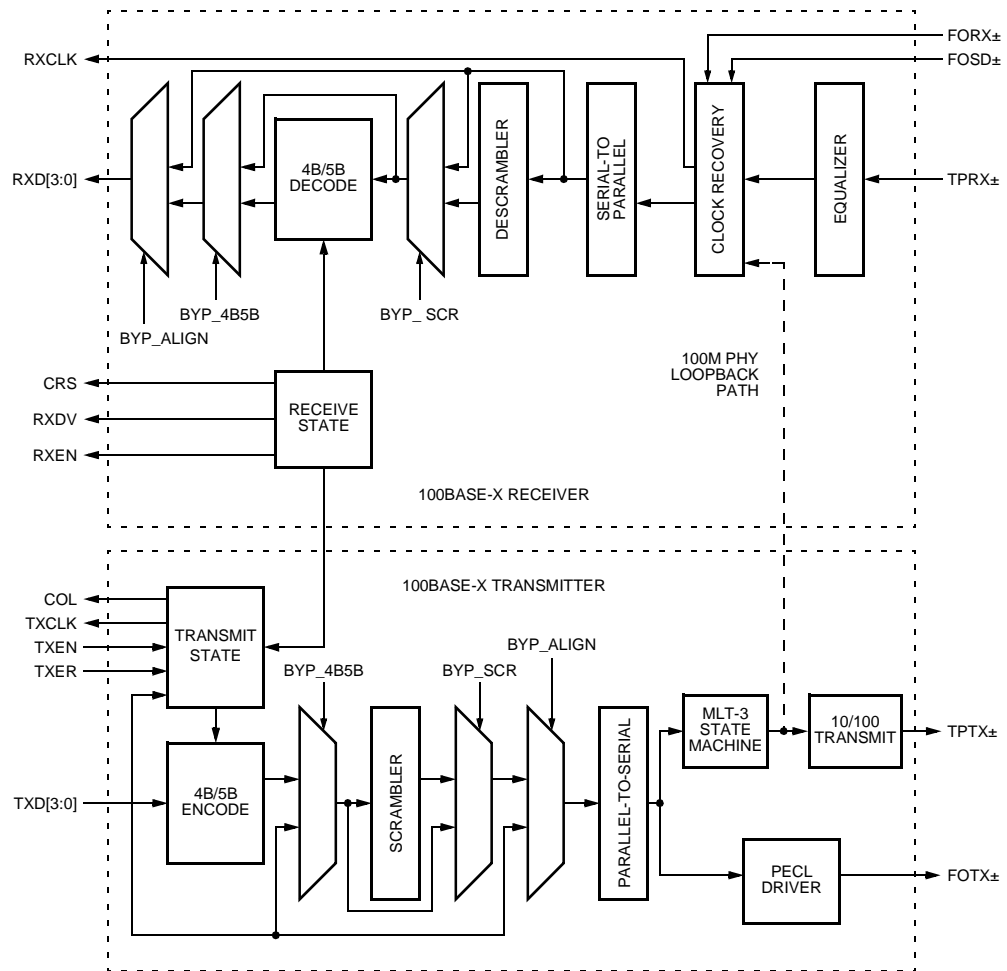
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Figure 3. 100Base-X Data Path

Functional Description (continued)

100Base-X Transmitter

The 100Base-X transmitter consists of functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a 125 Mbits/s serial data stream. This data stream may be routed either to the on-chip twisted-pair PMD for 100Base-TX signaling, or to an external fiber-optic PMD for 100Base-FX applications. The LU3X34FT implements the 100Base-X transmit state machine as specified in the *IEEE* 802.3u standard, Clause 24 and comprises the following functional blocks in its data path:

■ Symbol encoder

■ Scrambler block

■ Parallel/Serial converter and NRZ/NRZI encoder block

Symbol Encoder. The symbol encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) symbols for transmission. This conversion is required to allow control symbols to be combined with data symbols. Refer to the table below for 4B to 5B symbol mapping.

Following onset of the TXEN signal, the 4B/5B symbol encoder replaces the first two nibbles of the preamble from the MAC frame with a /J/K code-group pair (11000 10001) start-of-stream delimiter (SSD). The symbol encoder then replaces subsequent 4B codes with corresponding 5B symbols. Following negation of the TXEN signal, the encoder substitutes the first two IDLE symbols with a /T/R code-group pair (01101 00111) end-of-stream delimiter (ESD) then continuously injects IDLE symbols into the transmit data stream until the next transmit packet is detected.

Assertion of the TXER input while the TXEN input is also asserted will cause the LU3X34FT to substitute HALT code-groups for the 5B code derived from data present at TXD[3:0]. However, the SSD (/J/K) and ESD (/T/R) will not be substituted with HALT code-groups. As a result, the assertion of TXER while TXEN is asserted will result in a frame properly encapsulated with the /J/K and /T/R delimiters which contains HALT code-groups in place of the data code-groups.

The 100 Mbit symbol decoder translates all invalid code-groups into 0Eh by default. In case the ACCEPT HALT register is set (bit 5 of register 18h), the HALT code-group (00100) is translated into 05h instead.

Table 8. Symbol Coding Table

Symbol Name	5B Code [4:0]	4B Code [3:0]	Interpretation
0	11110	0000	Data 0
1	01001	0001	Data 1
2	10100	0010	Data 2
3	10101	0011	Data 3
4	01010	0100	Data 4
5	01011	0101	Data 5
6	01110	0110	Data 6
7	01111	0111	Data 7
8	10010	1000	Data 8
9	10011	1001	Data 9
A	10110	1010	Data A
B	10111	1011	Data B
C	11010	1100	Data C
D	11011	1101	Data D
E	11100	1110	Data E
F	11101	1111	Data F
I	11111	undefined	IDLE: interstream fill code
J	11000	0101	First start-of-stream delimiter
K	10001	0101	Second start-of-stream delimiter
T	01101	undefined	First end-of-stream delimiter
R	00111	undefined	Second end-of-stream delimiter

Functional Description (continued)

Table 8. Symbol Coding Table (continued)

Symbol Name	5B Code [4:0]	4B Code [3:0]	Interpretation
H	00100	undefined	HALT: transfer error
V	00000	undefined	Invalid code
V	00001	undefined	Invalid code
V	00010	undefined	Invalid code
V	00011	undefined	Invalid code
V	00101	undefined	Invalid code
V	00110	undefined	Invalid code
V	01000	undefined	Invalid code
V	01100	undefined	Invalid code
V	10000	undefined	Invalid code
V	11001	undefined	Invalid code

Scrambler Block. For 100Base-TX applications, the scrambler is required to control the radiated emissions at the media connector and on the twisted-pair cable.

The LU3X34FT implements a data scrambler as defined by the TP-PMD stream cipher function. The scrambler uses an 11-bit ciphering linear feedback shift register (LFSR) with the following recursive linear function:

$$X[n] = X[n - 11] + X[n - 9] \text{ (modulo 2)}$$

The output of the LFSR is combined with data from the encoder via an exclusive-OR logic function. By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range.

A seed value for the scrambler function can be loaded by setting bit 4 of register 18h. When this bit is set, the content of bits 10 through 0 of register 19h that compose the 5-bit PHY address and a 6-bit user seed, will be loaded into the LFSR. By specifying unique seed value for each PHY in a system, the total EMI energy produced by a repeater type application can be reduced.

Parallel to Serial and NRZ-NRZI Conversion. After the transmit data stream is scrambled, data is loaded into a shift register and clocked out with a 125 MHz clock into a serial bit stream. The serialized data is further converted from NRZ to NRZI format, which produces a transition on every Logic 1 and no transition on Logic 0.

Collision Detect. During 100 Mbits/s half-duplex operation, collision condition is detected if the transmitter and receiver become active simultaneously. Collision detection is indicated by the COL pin of the MII. For full-duplex applications, the COL signal is never asserted. A collision test register exists at address 0, bit 7. When this bit is high, COL is asserted if TXEN is high.

100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125 Mbits/s receive data stream. The LU3X34FT implements the 100Base-X receive state machine diagram as given in ANSI/*IEEE* Standard 802.3u, Clause 24. The 125 Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional blocks:

- Clock recovery module
- NRZI/NRZ and serial/parallel decoder
- Descrambler
- Symbol alignment block
- Symbol decoder
- Collision detect block
- Carrier sense block
- Stream decoder block

Functional Description (continued)

Clock Recovery. The clock recovery module accepts 125 Mbits/s scrambled NRZI data stream from either the on-chip 100Base-TX receiver or from an external 100Base-FX transceiver. The LU3X34FT uses an onboard digital phase-locked loop (PLL) to extract clock information of the incoming NRZI data, which is then used to retime the data stream and set data boundaries.

After power-on or reset, the PLL locks to a free-running 25 MHz clock derived from the external clock source. When initial lock is achieved, the PLL switches to lock to the data stream, extracts a 125 MHz clock from the data and use it for bit framing of the recovered data.

NRZI/NRZ and Serial/Parallel Conversion

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code-group's boundary.

Data Descrambling. The descrambler acquires synchronization with the data stream by recognizing IDLE bursts of 40 or more bits and locking its deciphering linear feedback shift register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and descrambled.

In order to maintain synchronization, the descrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler, the hold timer starts a 722 μs countdown. Upon detection of sufficient IDLE symbols within the 722 μs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled IDLE symbols within the 722 μs period, the descrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization. Register 18h, bit 3, can be used to extend the timer to 2 ms.

Symbol Alignment. The symbol alignment circuit in the LU3X34FT determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the descrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

Symbol Decoding. The symbol decoder functions as a look-up table that translates incoming 5B symbols

into 4B nibbles. The symbol decoder first detects the /J/K symbol pair preceded by IDLE symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end-of-stream delimiter (ESD). The translated data is presented on the RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

Valid Data Signal. The data valid signal (RXDV) indicates that recovered and decoded nibbles are being presented on the RXD[3:0] outputs synchronous to RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the media independent interface (MII). It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is deasserted.

Receiver Errors. The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will HALT both transmit and receive operations until such time that a valid link is detected.

The LU3X34FT performs the link integrity test as outlined in *IEEE* 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10 Mbits/s link status to form the reportable link status bit in serial management register 1, and driven to the LEDLNK pins.

When persistent signal energy is detected on the network, the logic moves into a link-ready state after approximately 500 μs, and waits for an enable from the autonegotiation module. When received, the link-up state is entered, and the transmit and receive logic blocks become active. Should autonegotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

Carrier Sense. Carrier sense (CRS) for 100 Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the receive data stream.

Functional Description (continued)

The carrier sense function is independent of symbol alignment. CRS is asserted during either packet transmission or reception. When the IDLE symbol pair is detected in the receive data stream, CRS is deasserted. CRS is intended to encapsulate RXDV.

Bad SSD Detection

A bad start-of-stream delimiter (bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-groups (SSD) is not received.

If this condition is detected, then the LU3X34FT will assert RXER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected. In addition, the false carrier counter (address 13h) will be incremented by one. Once at least two IDLE code-groups are detected, RXER and CRS become deasserted.

Far-End Fault Indication. Autonegotiation provides a mechanism for transferring information from the local station to the link partner that a remote fault has occurred for 100Base-TX. As autonegotiation is not currently specified for operation over fiber, the far-end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted IDLE stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI IDLE pattern.

The FEFI function is controlled by bit 11 of register 18h. It is initialized to 1 (enabled) if the FOSEL pin is at logic high level during powerup or reset. If the FEFI function is enabled the LU3X34FT will HALT all current operations and transmit the FEFI IDLE pattern when FOSD signal is deasserted following a good link indication from the link integrity monitor. FOSD signal is generated internally from the FORX± circuit. Transmission of the FEFI IDLE pattern will continue until FORX± signal is asserted. If three or more FEFI IDLE patterns are detected by the LU3X34FT, then bit 4 of the basic mode status register (address 01h) is set to one until read by management. Additionally, upon detection of

far end fault, all receive and transmit MII activity is disabled/ignored.

100Base-TX Transceiver

LU3X34FT implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetics for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmit output driver section.

Transmit Drivers. The LU3X34FT 100Base-TX transmit driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

Twisted-Pair Receiver. For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that comprises the differential line receiver, an adaptive equalizer and baseline wander compensation circuits.

The LU3X34FT uses an adaptive equalizer which changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.
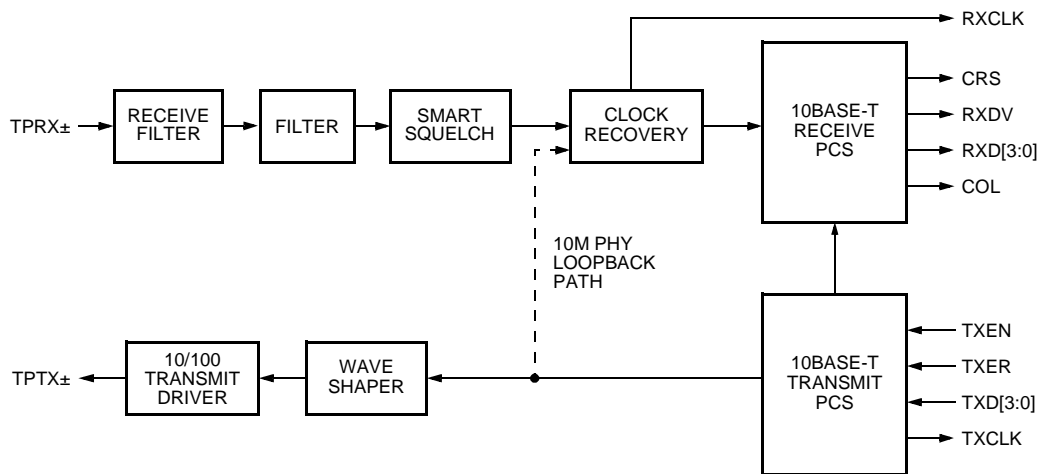
10Base-T Module

The 10Base-T transceiver module is *IEEE* 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, waveshaper, and link integrity functions, as defined in the standard. Figure 4 provides an overview for the 10Base-T module.

The LU3X34FT 10Base-T module is comprised of the following functional blocks:

■ Manchester encoder and decoder

■ Collision detector

■ Link test function

■ Transmit driver and receiver

■ Serial and parallel interface

■ Jabber & SQE test functions

■ Polarity detection and correction

Functional Description (continued)

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Figure 4. 10Base-T Module Data Path

Operation Modes

The LU3X34FT 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode the LU3X34FT functions as an *IEEE* 802.3 compliant transceiver with fully integrated filtering. The COL pin signals squelch jabber, and the CRS is asserted during transmit and receive. In full-duplex mode the LU3X34FT can simultaneously transmit and receive data.

Manchester Encoder/Decoder. Data encoding and transmission begins when the transmit enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmit enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separates the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more midbit transitions are detected. Within one and a half bit times after the last bit, carrier sense is deasserted.

Transmit Driver and Receiver. LU3X34FT integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only an isolation transformer and impedance

matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated properly.

Smart Squelch. The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The LU3X34FT implements an intelligent receive squelch on the TPRX± differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the *IEEE* 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally, the signal must exceed the original squelch level within a further 150 ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Functional Description (continued)

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected the squelch levels are reduced to minimize the effect of noise causing premature end of packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 11 of register address 1Ah.

Carrier Sense. Carrier sense (CRS) may be asserted due to receive activity once valid data is detected via the smart squelch function.

For 10 Mbits/s half-duplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mbits/s full-duplex operation, the CRS is asserted only due to receive activity. CRS is deasserted following an end of packet.

Collision Detection. For half-duplex operation, a 10Base-T collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII. If the ENDEC is transmitting when a collision is detected. The COL signal remains set for the duration of the collision.

SQE Test Function. Approximately 1 μs after the transmission of each packet, a signal quality error (SQE) signal of approximately 10-bit times is generated (internally) to indicate successful transmission. SQE is reported as a pulse on the COL signal of the MII. This function can be disabled by setting bit 12 of register 1Ah. The SQE test function is disabled in full-duplex mode.

Jabber Function. The jabber function monitors the LU3X34FT's output and disables the transmitter if it attempts to transmit a longer than legal-sized packet. If TXEN is high for greater than 24 ms, the 10Base-T transmitter will be disabled and COL will go active-high.

Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be deasserted for approximately 256 ms (the unjab time) before the jabber function re-enables the transmit outputs and deasserts COL signal.

The jabber function can be disabled by setting bit 10 of register 1Ah.

Link Test Function. A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in the *IEEE* 802.3 10Base-T standard. Each link pulse is nominally 100 ns in duration and is transmitted every 16 ms, in the absence of transmit data.

Automatic Link Polarity Detection. The LU3X34FT's 10Base-T transceiver module incorporates an automatic link polarity detection circuit. The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive receive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 15 of register 1Ch.

The automatic link polarity detection function can be disabled by setting bit 3 of register 1Ah.

Clock Synthesizer

The LU3X34FT implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz ± 50 ppm.

Autonegotiation

The autonegotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast link pulse (FLP) bursts provide the signaling used to communicate autonegotiation abilities between two devices at each end of a link segment. For further detail regarding autonegotiation, refer to clause 28 of the *IEEE* 802.3u specification. The LU3X34FT supports four different Ethernet protocols, so the inclusion of autonegotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The autonegotiation function within the LU3X34FT can be controlled either by internal register access or by the use of configuration pins. At powerup and at device reset, the configuration pins are sampled. If disabled, autonegotiation will not occur until software enables bit 12 in register 0. If autonegotiation is enabled, the negotiation process will commence immediately.

Functional Description (continued)

When autonegotiation is enabled, the LU3X34FT transmits the abilities programmed into the autonegotiation advertisement register at address 04h via FLP bursts. Any combination of 10 Mbits/s, 100 Mbits/s, half-duplex, and full-duplex modes may be selected. Autonegotiation controls the exchange of configuration information. Upon successful autonegotiation, the abilities reported by the link partner are stored in the auto-negotiation link partner ability register at address 05h.

The contents of the autonegotiation link partner ability register are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by autonegotiation by comparing the contents of register 04h and 05h and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.

1. 100Base-TX full duplex (highest priority)

2. 100Base-TX half duplex

3. 10Base-T full duplex

4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 00h provides control of enabling, disabling, and restarting of the autonegotiation function. When autonegotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbits/s or 100 Mbits/s operation, while the duplex mode bit (bit 8) controls switching between full-duplex operation and half-duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the autonegotiation enable bit (bit 12) is set.

The basic mode status register at address 01h indicates the set of available abilities for technology types (bits 15 to 11), autonegotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the LU3X34FT. The BMSR also provides status on the following:

1. Whether autonegotiation is complete (bit 5).

2. Whether the link partner is advertising that a remote fault has occurred (bit 4).

3. Whether a valid link has been established (bit 2).

The autonegotiation advertisement register at address 04h indicates the autonegotiation abilities to be advertised by the LU3X34FT. All available abilities are transmitted by default, but any ability can be suppressed by writing to this register or configuring external pins.

The autonegotiation link partner ability register at address 5h indicates the abilities of the link partner as indicated by autonegotiation communication. The contents of this register are considered valid when the autonegotiation complete bit (bit 5, register address 01h) is set.

Reset Operation

The LU3X34FT can be reset either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with a duration of at least 1 ms, to the RSTZ pin of the LU3X34FT during normal operation. A software reset is activated by setting the RESET bit in the basic mode control register (bit 15, register 00h). This bit is self-clearing and, when set, will return a value of 1 until the software reset operation has completed.

Hardware reset operation samples the pins and initializes all registers to their default values. This process includes re-evaluation of all hardware configurable registers. A hardware reset affects all four PHYs in the device.

A software reset can reset an individual PHY. It latches all configuration pins dedicated to the corresponding PHY but does not latch the external pins common to all four PHYs.

Logic levels on several I/O pins are detected during the hardware and software reset period to determine the initial functionality of LU3X34FT. Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to Vcc or ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled-up or weakly pulled-down through resistors. Configuration pins multiplexed with LED outputs should be set up with one of the following circuits shown in Figure 5.

Functional Description (continued)

LOGIC 1 CONFIGURATION   LOGIC 0 CONFIGURATION
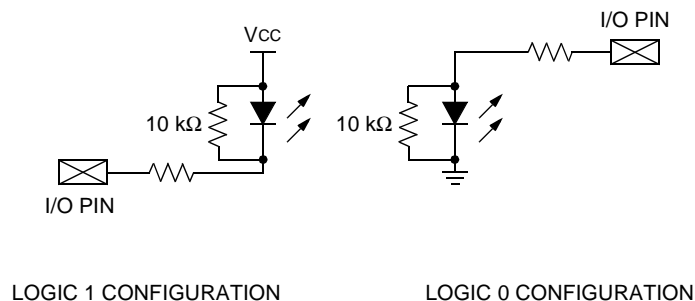
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Figure 5. Hardware RESET Configurations

PHY Address

The PHY device address is stored in bits [4:0] of the PHY address register (register address 19h). The upper 3 bits of this field are initialized by the three I/O pins designated as PHY[4:2] during powerup or hardware reset and can be changed afterward by writing into this register address (19h). The lower 2 bits are initialized to the port number of the PHY. These unique 5-bit addresses are used during serial management interface communication.

LED Configuration

The LU3X34FT provides four LED output pins for each of its four ports. In addition to the default functions associated with their pin names, there are several registers that allow users to customize LED operations.

Register 11h (programmable LED register) at PHY address 2 implement even more flexible LED configurations. Via the programmable LED register, each of the LEDs may be configured to operate in one the following modes: link, speed, duplex, receive, transmit, solid when link is up and blinks during activity, remote fault, and collision. Bits [0:3] in these registers allow the user to invert the on/off logic for each of these four programmable LEDs individually.

Note that all LED circuits are switched under the control of the programmable LED register whenever the content of register 11h differs from its default value.

Register 17h implements more LED configuration funcitons. With these registers, unused LED can be individually turned off to reduce power consumption.

Fiber Mode Select

A logic 1 level on pin 151, 157, 48, or 54 sets each channel in fiber mode individually. These pins are latched during reset operation. Pin 54 sets channel 3, pin 48 sets channel 2, pin 157 sets channel 1, and pin 151 sets channel 0 of the quad.

Autonegotiation and Speed Configuration

The four sets of five pins listed in Table 9 configure the speed capability of each channel of LU3X34FT. The logic state of these pins, at powerup or reset, are latched into the advertisement register (register address 04h) for autonegotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 00h) according to the following table.

Functional Description (continued)

Table 9. Initial Values for Autonegotiation Registers

Configuration Pins at RESET					Registers Initial Value		
ANEN **Pin 51[3]** **Pin 45[2]** **Pin 154[1]** **Pin 148[0]**	**100FD** **Pin 61[3]** **Pin 89[2]** **Pin 110[1]** **Pin 135[0]** **(bit 4.8)**	**100HD** **Pin 53[3]** **Pin 47[2]** **Pin156[1]** **Pin 150[0]** **(bit 4.7)**	**10FD** **Pin 40 [3]** **Pin 121[2]** **Pin 122[1]** **Pin1[0]** **(bit 4.6)**	**10HD** **Pin 52[3]** **Pin 46[2]** **Pin 155[1]** **Pin 149[0]** **(bit 4.5)**	**AUTONEG** **reg 0.12**	**SPEED** **reg 0.13**	**DUPLEX** **reg 0.8**
0	1	X	X	X	0	1	1
0	0	1	1	X	0	1	1
0	0	1	0	X	0	1	0
0	0	0	1	X	0	0	1
0	0	0	0	1	0	0	0
1	X	X	X	X	1	0	0

100Base-X PCS Configuration

The logic state of BPSCR, BP4B5B, and BPALIGN can be attained through bit configuration.

MII Registers

The LU3X34FT has four independant PHYs in it. Each PHY has its own identical set of registers as tabulated below. The PHY address differentiates which PHY to be read or written into. The following tables of registers are applicable to each register.

Table 10. MII Management Registers

Address	Register Name	Basic/Extended
0h	Control Register	B
1h	Status Register	B
2h—3h	PHY Identifier Register	E
4h	Autonegotiation Advertisement Register	E
5h	Autonegotiation Link Partner Ability Register	E
6h	Autonegotiation Expansion Register	E
7h—Fh	*IEEE* Reserved	E
11h	Programmable LED	E
13h	False Carrier Counter	E
15h	Receive Error Counter	E
17h	PHY Control/Status Register	E
18h	Config 100 Register	E
19h	PHY Address Register	E
1Ah	Config 10 Register	E
1Bh	Status 100 Register	E
1Ch	Status 10 Register	E
1Dh	Interrupt Mask Register	E
1Eh	Interrupt Status Register	E

Note:
Legends:
RO—Read only
R/W—Read and write capable
SC—Self-clearing
LL—Latching low, unlatch on read
LH—Latching high, unlatch on read
COR—Clear on read

Table 11. Control Register (Register 0h)

Bit(s)	Name	Description	R/W	Default
15	Reset	1—PHY reset 0—Normal operation Setting this bit initiates the software reset function that resets the entire LU3X34FT device, except for the phase-locked loop circuit. It will relatch in autonegotiation configuration pin values (ANEN, FOSEL, 100FD, 100HD, 10FD, 10HD) and set all registers to their default values. The software reset process takes 25 μs to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.	R/W SC	0h

MII Registers (continued)

Table 11. Control Register (Register 0h) (continued)

Bit(s)	Name	Description	R/W	Default
14	Loopback	1—Enable loopback mode 0—Disable loopback mode This bit controls the PHY loopback operation that isolates the network transmitter outputs (TX±) and routes the MII transmit data to the MII receive data path. This function should only be used when auto-negotiation is disabled (bit 12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register.	R/W	0h
13	Speed Selection	1—100 Mbits/s 0—10 Mbits/s Link speed is selected by this bit or by autonegotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). At powerup or reset, this bit will be set unless ANEN detects a logic 1 or both 100 FD and 100 HD pins detects logic 0 state.	R/W	Pin
12	Autonegotiation Enable	1—Enable autonegotiation process 0—Disable autonegotiation process This bit determines whether the link speed should be set up by the autonegotiation process. It is set at powerup or hardware/software reset, if the ANEN pin detects a logic 1 input level.	R/W	Pin
11	Powerdown	1—Powerdown 0—Normal operation Setting this bit puts the LU3X34FT into powerdown mode. During the powerdown mode, the MII interface are isolated and TXEN signal is ignored. The management interface remains active and can be used to reset this bit in order to exit the power-down mode.	R/W	0h
10	Isolate	1—Isolate PHY from MII 0—Normal operation Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the LU3X34FT does not respond to TXD[3:0], TXEN, and TXER inputs, and it presents a high impedance on its TXCLK, RXCLK, RXDV, RXER, RXD[3:0], COL, and CRS outputs. This bit is initialized to the logic level of ISOLATE pin at powerup or hard reset. Value of this bit also follows the ISOLATE pin transition.	R/W	Pin

MII Registers (continued)

Table 11. Control Register (Register 0h) (continued)

Bit(s)	Name	Description	R/W	Default
9	Restart Autonegotiation	1—Restart autonegotiation process 0—Normal operation Setting this bit while autonegotiation is enabled forces a new autonegotiation process to start. This bit is self-clearing and returns to 0 after the autonegotiation process has commenced.	R/W, SC	0h
8	Duplex Mode	1—Full-duplex mode 0—Half-duplex mode If autonegotiation is disabled, this bit determines the duplex mode for the link. At powerup or reset, this bit is set to 1 only if ANEN pin detects a logic 0 and either 100FD or 10FD pin detects a logic 1.	R/W	Pin
7	Collision Test (only applicable while in PHY loopback mode)	1—Enable COL signal test 0—Disable COL signal test When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN	R/W	0h
6:0	Reserved	Not used.	RO	0h

Table 12. Status Register Bit Definitions (Register 1h)

Bit(s)	Name	Description	R/W	Default
15	100Base-T4	1—Capable of 100Base-T4 0—Not capable of 100Base-T4 This bit is hardwired to 0, indicating that the LU3X34FT does not support 100Base-T4.	RO	0h
14	100Base-X Full Duplex	1—Capable of 100Base-X full-duplex mode 0—Not capable of 100Base-X full-duplex mode This bit is hardwired to 1, indicating that the LU3X34FT supports 100Base-X full-duplex mode.	RO	1h
13	100Base-X Half Duplex	1—Capable of 100Base-X half-duplex mode 0—Not capable of 100Base-X half-duplex mode This bit is hardwired to 1, indicating that the LU3X34FT supports 100Base-X half-duplex mode.	RO	1h
12	10 Mbits/s Full Duplex	1—Capable of 10 Mbits/s full-duplex mode 0—Not capable of 10 Mbits/s full-duplex mode This bit is hardwired to 1, indicating that the LU3X34FT supports 10Base-T full-duplex mode.	RO	1h

MII Registers (continued)

Table 12. Status Register Bit Definitions (Register 1h) (continued)

Bit(s)	Name	Description	R/W	Default
11	10 Mbits/s Half Duplex	1—Capable of 10 Mbits/s half-duplex mode 0—Not capable of 10 Mbits/s half-duplex mode This bit is hardwired to 1, indicating that the LU3X34FT supports 10Base-T half-duplex mode.	RO	1h
10	100Base-T2	1—Capable of 100Base-T2 0—Not capable of 100Base-T2 This bit is hardwired to 0, indicating that the LU3X34FT does not support 100Base-T2.	RO	0h
9:7	Reserved	Ignore when read.	RO	0h
6	MF Preamble Suppression	1—Accepts management frames with preamble suppressed 0—Will not accept management frames with preamble suppressed This bit is hardwired to 1, indicating that the LU3X34FT accepts management frame without preamble. A minimum of 32 preamble bits are required following power-on or hardware reset. One IDLE bit is required between any two management transactions as per *IEEE* 802.3u specification.	RO	1h
5	Autonegotiation Complete	1—Autonegotiation process completed 0—Autonegotiation process not completed If autonegotiation is enabled, this bit indicates whether the autonegotiation process has been completed.	RO	0h
4	Remote Fault	1—Remote fault detected 0—Remote fault not detected This bit is latched to 1 if the RF bit in the autonegotiation link partner ability register (bit 13, register 05h) is set or the receive channel meets the far-end fault indication function criteria. It is unlatched when this register is read.	RO, LH	0h
3	Autonegotiation Ability	1—Capable of autonegotiation 0—Not capable of autonegotiation This bit defaults to 1, indicating that LU3X34FT is capable of autonegotiation.	RO	1h

MII Registers (continued)

Table 12. Status Register Bit Definitions (Register 1h) (continued)

Bit(s)	Name	Description	R/W	Default
2	Link Status	1—Link is up 0—Link is down This bit reflects the current state of the link-test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface.	RO, LL	0h
1	Jabber Detect	1—Jabber condition detected 0—Jabber condition not detected During 10Base-T operation, this bit indicates the occurrence of a jabber condition. It is implemented with a latching function so that it becomes set until it is cleared by a read.	RO, LH	0h
0	Extended Capability	1—Extended register set 0—No extended register set This bit defaults to 1, indicating that the LU3X34FT implements extended registers.	RO	1h

Table 13. PHY Identifier (Register 2h)

Bit(s)	Name	Description	R/W	Default
15:0	PHY-ID[15:0]	*IEEE* Address	RO	0043h

Table 14. PHY Identifier (Register 3h)

Bit(s)	Name	Description	R/W	Default
15:10	PHY-ID[15:0]	*IEEE* Address/ Model No./ Rev. No.	RO	7440h

Table 15. Advertisement (Register 4h)

Bit(s)	Name	Description	R/W	Default
15	Next Page	1—Capable of next page function 0—Not capable of next page function This bit is defaults to 0, indicating that LU3X34FT is not next page capable.	RO	0h
14	Reserved	Reserved.	RO	0h
13	Remote Fault	1—Remote fault has been detected 0—No remote Fault has been detected This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto-negotiation link partner.	R/W	0h
12:11	*IEEE* Reserved	These 2 bits default to 0.	R/W	0h

MII Registers (continued)

Table 15. Advertisement (Register 4h) (continued)

Bit(s)	Name	Description	R/W	Default
10	Flow Control	1—MAC sublayer is capable of pause-based flow control 0—MAC sublayer not capable of pause-based flow control This bit advertises the MAC sublayer has pause/flow control capability of operation when set in full-duplex mode. This must be set only when the PHY is advertising 10FD/100FD modes. At hardware reset, this bit is set to 1 if the PAUSE pin detects logic 1.	R/W	Pin
9	Technology Ability Field for 100Base-T4	This bit defaults to 0, indicating that the LU3X34FT does not support 100Base-T4.	RO	0h
8:5	Technology Ability Field	This 4-bit field contains the advertised ability of this PHY. At powerup or reset, the logic level of 100FD, 100HD, 10FD, and 10HD pins are latched into bits 8 through 5, respectively.	R/W	Pin
4:0	Selector Field	These 5 bits are hardwired to 00001h, indicating that the LU3X34FT supports *IEEE* 802.3 CSMA/CD.	R/W	01h

Table 16. Autonegotiation Link Partner Ability (Register 5h)

Bit(s)	Name	Description	R/W	Default
15	Next Page	1—Capable of next page function 0—Not capable of next page function	RO	0h
14	Acknowledge	1—Link partner acknowledges reception of the ability data word 0—Not acknowledged	RO	0h
13	Remote Fault	1—Remote fault has been detected 0—No remote fault has been detected	RO	0h
12:5	Technology Ability Field	Supported technologies.	RO	0h
4:0	Selector Field	Encoding definitions.	RO	0h

Table 17. Autonegotiation Expansion Register (Register 6h)

Bit(s)	Name	Description	R/W	Default
15:5	Reserved	Reserved.	RO	0h
4	Parallel Detection Fault	1—Fault has been detected 0—No fault detected This bit is set if the parallel detection fault state of the autonegotiation arbitration state machine is visited during the auto-negotiation process. It will remain set until this register is read.	RO, LH	0h

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MII Registers (continued)

Table 17. Autonegotiation Expansion Register (Register 6h) (continued)

Bit(s)	Name	Description	R/W	Default
3	Link Partner Next Page Capable	1—Link partner is next page capable 0—Link partner is not next page capable This bit indicates whether the link partner is next page capable. It is meaningful only when the autonegotiation complete bit (bit 5, register 1) is set.	RO	0h
2	Next Page Capable	1—Local device is next page capable 0—Local device is not next page capable This bit defaults to 0, indicating that LU3X34FT is not next page capable.	RO	0h
1	Page Received	1—A new page has been received 0—No new page has been received This bit is latched to 1 when a new link code word page has been received. This bit is automatically cleared when the autonegotiation link partner ability register (register 05h) is read by management interface.	RO, LH	0h
0	Link Partner Autonegotiable	1—Link partner is autonegotiable 0—Link partner is not autonegotiable	RO	0h

Table 18. Programmable LED (Register 11h) Only Under PHY Address for Port 2

Bit(s)	Name	Description	R/W	Default
15:13	Function of LEDACT Pin	Programable LED output with the following settings: [000]: link [001]: speed [010]: duplex [011]: receive [100]: transmit [101]: solid when link is up, blinks during activity [110]: remote fault [111]: collision	R/W	100
12:10	Function of LEDFD Pin	Programable LED output with the following settings: [000]: link [001]: speed [010]: duplex [011]: receive [100]: transmit [101]: solid when link is up, blinks during activity [110]: remote fault [111]: collision	R/W	010

MII Registers (continued)

Table 18. Programmable LED [Register 11h] Only Under PHY Address for Port 2 (continued)

Bit(s)	Name	Description	R/W	Default
9:7	Function of LED100 Pin	Programable LED output with the following settings: [000]: link [001]: speed [010]: duplex [011]: receive [100]: transmit [101]: solid when link is up, blinks during activity [110]: remote fault [111]: collision	R/W	001
4:6	Function of LEDLNK Pin	Programable LED output with the following settings: [000]: link [001]: speed [010]: duplex [011]: receive [100]: transmit [101]: solid when link is up, blinks during activity [110]: remote fault [111]: collision	R/W	000
3:0	LED Inversion Modes	Each bit controls the inversion option for one LED. If set to 1, LED is OFF when the programmed activity is true and ON when the programmed activity is false. Listed below are the relationship between the control bits and LED. bit 3: link LED bit 2: activity LED bit 1: full-duplex LED bit 0: speed 100 LED	R/W	0000

Table 19. False Carrier Counter (Register 13h)

Bit(s)	Name	Description	R/W	Default
15:0	False Carrier Count	Number of false carrier conditions since reset or read. The counter is incremented once for each packet that has false carrier condition detected. This counter may roll over depending on value of CSMODE bit (bit 13 of register 17h).	RO, COR	0h

MII Registers (continued)

Table 20. Receive Error Counter (Register 15h)

Bit(s)	Name	Description	R/W	Default
15:0	RX Error Count	Number of receive errors since last reset. The counter is incremented once for each packet that has receive error condition detected. This counter may roll over depending on value of the CSMODE bit (bit 13 of register 17h).	RO, COR	0h

Table 21. PHY Control/Status Register (Register 17h)

Bit(s)	Name	Description	R/W	Default
15	Reserved	Reserved.	RO	0h
14	FOSEL	1—Fiber mode 0—TX mode For 100Base-X operation, this bit determines whether LU3X34FT interfaces with the network through the internal 100Base-TX transceiver or using external fiber-optic transceiver. It is initialized to the logic level of FOSEL pin at powerup, hardware, or software reset.	RO	Pin
13	CSMODE	1—Counter sticks at FFFFh 0—Counters roll over This bit controls the operation of false carrier counter, and receive error counters.	R/W	0h
12	TPTXTR	1—Tri-state transmit pairs 0—Normal operation When this bit is set, the twisted-pair transmitter outputs af all four ports are tri-stated. Note that the twisted-pair transmit driver can be tri-stated by either this bit or the TPTXTR pin (pin 43).	R/W	0h
11	ThunderLAN Interrupt Enable	1—MDIO ThunderLAN interrupt enabled 0—MDIO ThunderLAN interrupt disabled This bit enables/disables the TI ThunderLAN interrupt mechanism.	R/W	0h
10	MF Preamble Suppression Enable	1—MDIO preamble suppression enabled 0—MDIO preamble suppression disabled LU3X34FT can accept management frames without preamble as described in bit 6 of register 1h. This bit allows the user to enable or disable the preamble suppression function.	R/W	1h
9	Speed Status	1—PHY is in 100 Mbits/s mode 0—PHY is in 10 Mbits/s mode This value is not defined during the auto-negotiation period.	RO	0h

MII Registers (continued)

Table 21. PHY Control/Status Register (Register 17h) (continued)

Bit(s)	Name	Description	R/W	Default
8	Duplex Status	1—PHY is in full-duplex mode 0—PHY is in half-duplex mode This value is not defined during the auto-negotiation period.	RO	0h
7:6	Reserved	Reserved.	R/W	0h
5	LEDACT off	1—Tri-state LEDACT output 0—Normal operation	R/W	0
4	LEDLNK off	1—Tri-state LEDLNK output 0—Normal operation (nonpulse stretched)	R/W	0
3	Reserved	Reserved.	R/W	0
2	LEDFD off	1—Tri-state LEDFD output 0—Normal operation	R/W	0
1	LED100 off	1—Tri-state LED100 output 0—Normal operation (nonpulse stretched)	R/W	0
0	LED Pulse Stretching Disable	1—LED pulse stretching disabled 0—LED pulse stretching enabled When set to 0 LEDFD and LEDACT outputs are stretched 48 ms—72 ms.	R/W	0

Table 22. Config 100 Register (Register 18h)

Bit(s)	Name	Description	R/W	Default
15	BPSCR	1—Disable scrambler/descrambler 0—Enable scrambler/descrambler	R/W	FOSEL
14	BP4B5B	1—Disable 4B/5B encoder/decoder 0—Enable 4B/5B encoder/decoder	R/W	0h
13	Reserved	Reserved.	RO	0h
12	BPALIGN	1—Pass unaligned data to MII 0—Pass aligned data to MII	R/W	0h
11	Enable FEFI	1—Enable FEFI 0—Disable FEFI This bit enables/disables far-end fault indicator function for 100Base-FX and 10Base-T operation. It is initialized to the logic level of FOSEL pins at powerup or reset. After reset, this bit is writable if and only if the FOSEL register (bit 14 of register 17h) is set.	R/W	Pin
10	Reserved	Reserved.	R/W	1h
9	Force Good Link 100	1—Force good link in 100 Mbits/s mode 0—Normal operation	R/W	0h
8:6	Reserved	Reserved.	R/W	01h
5	Accept HALT	1—Passes HALT symbols to the MII 0—Normal operation	R/W	0h

MII Registers (continued)

Table 22. Config 100 Register (Register 18h) (continued)

Bit(s)	Name	Description	R/W	Default
4	Load Seed	1—Loads the scrambler seed 0—Normal operation Setting this bit loads the user seed stored in register 19h into the 100Base-X scrambler. The content of this bit returns to 0 after the loading process is completed and no transmit is active.	R/W, SC	0h
3	Burst Mode	1—Burst mode 0—Normal operation Setting this bit expands the 722 μs scrambler time-out period to 2,000 μs.	R/W	0h
2:0	Reserved	Reserved.	RO	0h

Table 23. PHY Address Register (Register 19h)

Bit(s)	Name	Description	R/W	Default
15:11	Reserved	Reserved.	RO	0h
10:5	User Seed	User-modifiable seed data. When the load seed bit (bit 4 of register 18h) is set, bits 10 through 0 of this register are loaded into the 100Base-X scrambler.	R/W	21h
4:0	PHY Address	These 5 bits store the part address used by the serial management interface. Upper three of these bits are latched from the pins during pwerup or hard reset. Lower two bits are assigned automatically.	R/W	Pin

MII Registers (continued)

Table 24. Config 10 Register (Register 1Ah)

Bit(s)	Name	Description	R/W	Default
15	10 Mbits/s Serial Mode	1—10 Mbits/s serial mode 0—10 Mbits/s nibble mode During 10Base-T operation, this bit determines whether the MII will be operating in nibble mode or serial mode. It is initialized to the logic level of SERSEL pin (pin 136).	RO	Pin
14	Force 10 Mbits/s Good Link	1—Force 10 Mbits/s good link 0—Normal operation	R/W	0h
13	Reserved	Reserved.	R/W	0h
12	SQE_EN	1—Signal quality error test enabled 0—Default SQE is disabled	R/W	0h
11	Low Squelch Select	1—Low squelch level selected 0—Normal squelch level selected	R/W	0h
10	Jabber Disable	1—Jabber function disabled 0—Normal operation	R/W	0h
9	100 Mbits/s Detect	1—Detect mode switching in 10 Mbit mode 0—Normal operation When set to 1, the part will restart auto-negotiation when it is in 10 Mbit mode and detects 100 Mbit data reception.	R/W	0h
8	Reserved	Reserved.	RO	0h
7	Digital Filter Disable	1—Disable digital filter 0—Normal operation	R/W	0h
6:4	Reserved	Reserved.	R/W	0h
3	Autopolarity Disable	1—Disable autopolarity function 0—Enable autopolarity function	R/W	0h
2:0	Reserved	Reserved.	R/W	0h

Table 25. Status 100 Register (Register 1Bh)

Bit(s)	Name	Description	R/W	Default
15:14	Reserved	Reserved.	RO	0h
13	PLL Lock Status	1—100 Mbits/s PLL locked 0—100 Mbits/s PLL not locked	RO	0h
12	False Carrier Status	1—False carrier detected 0—Normal operation	RO, LH	0h
11:0	Reserved	Reserved.	RO	0h

Table 26. Status 10 Register (Register 1Ch)

Bit(s)	Name	Description	R/W	Default
15	Polarity	1—Polarity of cable is swapped 0—Polarity of cables is correct	RO	0h
14:0	Reserved	Reserved.	RO	0h

MII Registers (continued)

Table 27. Interrupt Mask Register (Register 1Dh)

Bit(s)	Name	Description	R/W	Default
15	False Carrier Status	0—Enable interrupt 1—Disable interrupt	R/W	0h
14	Receiver Error Counter Full	0—Enable interrupt 1—Disable interrupt	R/W	0h
13	Reserved	Reserved.	R/W	0h
12	Remote Fault	0—Enable interrupt 1—Disable interrupt	R/W	0h
11	Autonegotiation Complete	0—Enable interrupt 1—Disable interrupt	R/W	0h
10	Link Up	0—Enable interrupt 1—Disable interrupt	R/W	0h
9	Link Down	0—Enable interrupt 1—Disable interrupt	R/W	0h
8	Data Recovery 100 Lock Up	0—Enable interrupt 1—Disable interrupt	R/W	0h
7	Data Recovery Lock Down	0—Enable interrupt 1—Disable interrupt	R/W	0h
6:0	Reserved	Reserved.	RO	0h

Table 28. Interrupt Status Register (Register 1Eh)

Bit(s)	Name	Description	R/W	Default
15	False Carrier Counter Full	1—False carrier counter has rolled over 0—False carrier counter has not rolled over	RO, LH	0h
14	Receiver Error Counter Full	1—Receive error counter has rolled over 0—Receive error counter has not rolled over	RO, LH	0h
13	Reserved	Reserved.	RO, LH	0h
12	Remote Fault	1—Remote fault observed by PHY 0—Remote fault not observed by PHY	RO, LH	0h
11	Autonegotiation Complete	1—Autonegotiation has completed 0—Autonegotiation has not completed	RO, LH	0h
10	Link Up	1—Link is up 0—No change on link status	RO, LH	0h
9	Link Down	1—Link has gone down 0—No change on link status	RO, LH	0h
8	Data Recovery 100 Lock Up	1—Data recovery has locked 0—Data recovery is not locked	RO, LH	0h
7	Data Recovery 100 Lock Down	1—Data recovery is not locked 0—Data recovery has locked	RO, LH	0h
6:0	Reserved	Reserved.	RO	0h

dc and ac Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 29. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	−65	150	°C
Voltage on Any Pin with Respect to Ground	—	−0.5	5	V
Maximum Supply Voltage	—	—	5	V

Table 30. Operating Conditions

Parameter	Symbol	Min	Typ*	Max	Unit
Operating Supply Voltage	—	3.135	3.3	3.46	V
Power Dissipation:					
100 Mbits/s TX with LEDs	P_D	—	—	480	mA
100 Mbits/s FX with LEDs	P_D	—	—	450	mA
10 Mbits/s with LEDs	P_D	—	—	480	mA
Autonegotiating with LEDs	P_D	—	—	200	mA

* Typical power dissipations are specified at 3.3 V and 25 °C. This is the power dissipated by the LU3X34FT.

Table 31. dc Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Recommended Power Supply	—	3.0	3.6	V
V_{SS}			0.0	0.0	V
I_{DD}	Supply Current 100Base-TX	V_{DD} = 3.3 V, V_{SS} = 0.0 V full-duplex traffic	—	480	mA
I_{DD}	Supply Current 10Base-TX	V_{DD} = 3.3 V, V_{SS} = 0.0 V full-duplex traffic	—	480	mA
I_{DD}	Supply Current Autonegotiation Mode	V_{DD} = 3.3 V, V_{SS} = 0.0 V no link	—	200	mA
I_{DD}	Supply Current 100Base-FX	V_{DD} = 3.3 V, V_{SS} = 0.0 V full-duplex traffic	—	450	mA
V_{IH}	TTL Input High Voltage	V_{DD} = 3.3 V, V_{SS} = 0.0 V	2.0	—	V
V_{IL}	TTL Input Low Voltage	V_{DD} = 3.3 V, V_{SS} = 0.0 V	—	0.8	V
V_{OH}	TTL Output High Voltage	V_{DD} = 3.3 V, V_{SS} = 0.0 V	2.4	—	V
V_{OL}	TTL Output Low Voltage	V_{DD} = 3.3 V, V_{SS} = 0.0 V	—	0.4	V
I_{OLL}	Output Low Current LED Pins	—	—	10	mA
I_{OHL}	Output High Current LED Pins	—	—	10	mA
I_{OLM}	Output Low Current MII Pins	—	—	4	mA

dc and ac Specifications (continued)

Table 31. dc Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
I$_{OHM}$	Output High Current MII Pins	—	—	4	mA
V$_{IH}$	PECL Input High Voltage	—	V$_{DD}$ – 1.16	V$_{DD}$ – 0.88	V
V$_{IL}$	PECL Input Low Voltage	—	V$_{DD}$ – 1.81	V$_{DD}$ – 1.47	V
V$_{OH}$	PECL Output High Voltage	—	V$_{DD}$ – 1.02	—	V
V$_{OL}$	PECL Output Low Voltage	—	—	V$_{DD}$ – 1.62	V
MII C$_{IN}$	Input Capacitance	—	—	8	pF

Clock Timing

Table 32. Clock Timing

Symbol	Parameter	Min	Max	Unit
t1	Clock High Pulse Width	17	23	ns
t2	Clock Low Pulse Width	17	23	ns
t3	Clock Period*	40	40	ns

* Specified at ±50 ppm.
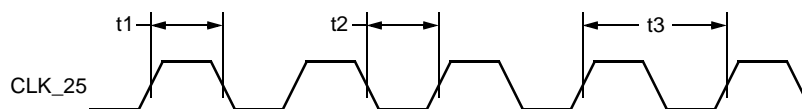
5-7912(F).r1

Figure 6. Clock Timing

Clock Timing (continued)

Table 33. Transmit Clock (Input and Output)

Symbol	Parameter	Min	Max	Unit
t1	TXCLK High Pulse Width (100 Mbits/s)	14	26	ns
	TXCLK High Pulse Width (10 Mbits/s MII)	140	260	ns
	TXCLK High Pulse Width (10 Mbits/s serial)	35	65	ns
t2	Xin Rise to TXCLK Rise (100 Mbits/s)	—	—	ns
	Xin Rise to TXCLK Rise (10 Mbits/s MII)	—	—	ns
	Xin Rise to TXCLK Rise (10 Mbits/s serial)	—	—	ns
t3	TXCLK Low Pulse Width (100 Mbits/s)	14	26	ns
	TXCLK Low Pulse Width (10 Mbits/s MII)	140	260	ns
	TXCLK Low Pulse Width (10 Mbits/s serial)	35	65	ns
t4	TXCLK Period (100 Mbits/s)*	40	40	ns
	TXCLK Period (10 Mbits/s MII)*	400	400	ns
	TXCLK Period (10 Mbits/s serial)*	100	100	ns

* Specified at ±100 ppm.
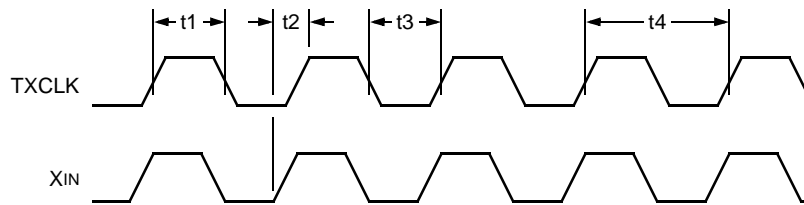
5-7913(F)

Figure 7. Transmit Clock (Input and Output)

Clock Timing (continued)

Table 34. Management Clock

Symbol	Parameter	Min	Max	Unit
t1	MDC Low Pulse Width	200	—	ns
t2	MDC High Pulse Width	200	—	ns
t3	MDC Period	400	—	ns
t4	MDIO(I) Setup to MDC Rising Edge	10	—	ns
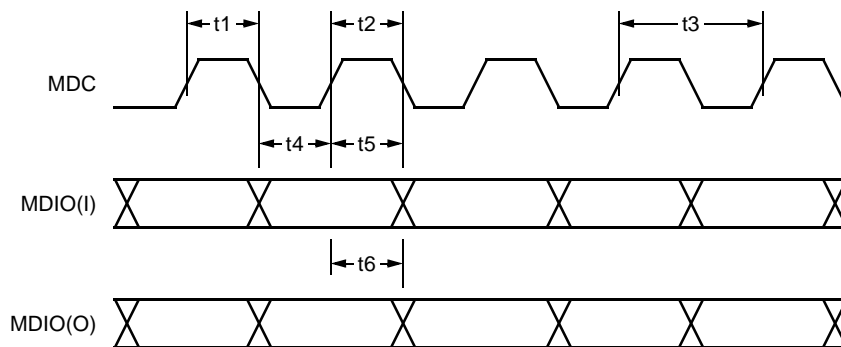
5-7914(F)

Figure 8. Management Clock

Clock Timing (continued)

Table 35. MII Receive Timing

Symbol	Parameter	Min	Max	Unit
t1	RXER, RXDV, RXD[3:0] Setup to RXCLK Rise	10	—	ns
t2	RXER, RXDV, RXD[3:0] Hold After RXCLK Rise	10	—	ns
t3	RXCLK High Pulse Width (100 Mbits/s)	14	26	ns
	RXCLK High Pulse Width (10 Mbits/s MII)	200	200	ns
	RXCLK High Pulse Width (10 Mbits/s serial)	50	50	ns
t4	RXCLK Low Pulse Width (100 Mbits/s)	14	26	ns
	RXCLK Low Pulse Width (10 Mbits/s MII)	140	260	ns
	RXCLK Low Pulse Width (10 Mbits/s serial)	35	65	ns
t5	RXCLK Period (100 Mbits/s)	40	40	ns
	RXCLK Period (10 Mbits/s MII)	400	400	ns
	RXCLK Period (10 Mbits/s serial)	100	100	ns
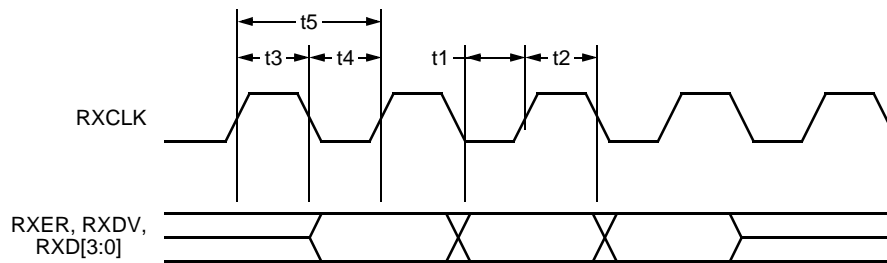
5-7915(F).r1

Figure 9. MII Receive Timing

Clock Timing (continued)

Table 36. MII Transmit Timing

Symbol	Parameter	Min	Max	Unit
t1	TXER, TXEN, TXD[3:0] Setup to TXCLK Rise	10	—	ns
t2	TXER, TXEN, TXD[3:0] Delay After TXCLK Rise	0	25	ns
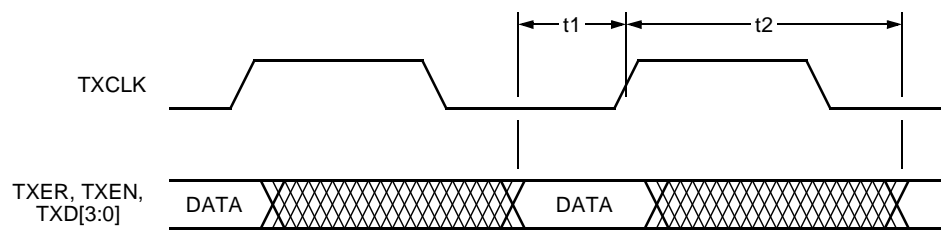
5-7916(F)

Figure 10. MII Transmit Timing

Clock Timing (continued)

Table 37. Transmit Timing

Symbol	Parameter	Min	Max	Unit
t1	TXEN Sampled to CRS High (100 Mbits/s)	0	4	bits
	TXEN Sampled to CRS High (10 Mbits/s)	—	1.5	bits
t2	TXEN Sampled to CRS Low (100 Mbits/s)	0	16	bits
	TXEN Sampled to CRS Low (10 Mbits/s)	—	16	bits
t3	Transmit Latency (100 Mbits/s)	6	14	bits
	Transmit Latency (10 Mbits/s)	4	—	bits
t4	Sampled TXEN Inactive to End of Frame (100 Mbits/s)	—	17	bits
	Sampled TXEN Inactive to End of Frame (10 Mbits/s)	—	5	bits
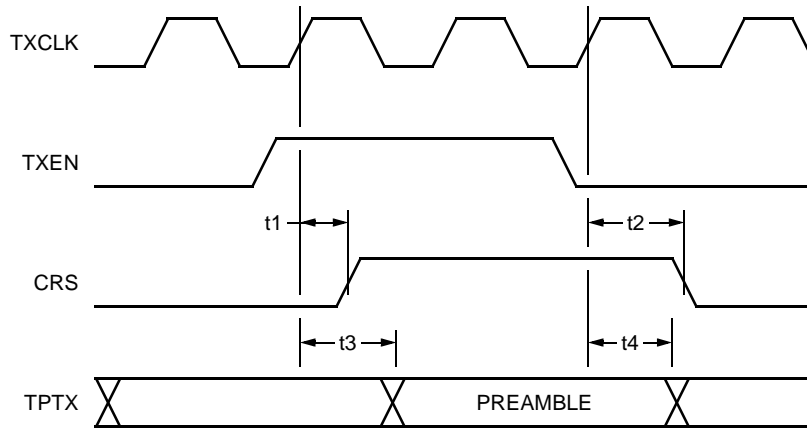
5-7917(F)

Figure 11. Transmit Timing

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Clock Timing (continued)

Table 38. Receive Timing

Symbol	Parameter	Min	Max	Unit
t1	Receive Frame to Sampled Edge of RXDV (100 Mbits/s)	—	15	bits
	Receive Frame to Sampled Edge of RXDV (10 Mbits/s)	—	22	bits
t2	Receive Frame to CRS High (100 Mbits/s)	—	13	bits
	Receive Frame to CRS High (10 Mbits/s)	—	5	bits
t3	End of Receive Frame to Sampled Edge of RXDV (100 Mbits/s)	—	12	bits
	End Receive Frame to Sampled Edge of RXDV (10 Mbits/s)	—	4	bits
t4	End of Receive Frame to CRS Low (100 Mbits/s)	13	24	bits
	End of Receive Frame to CRS Low (10 Mbits/s)	—	4.5	bits
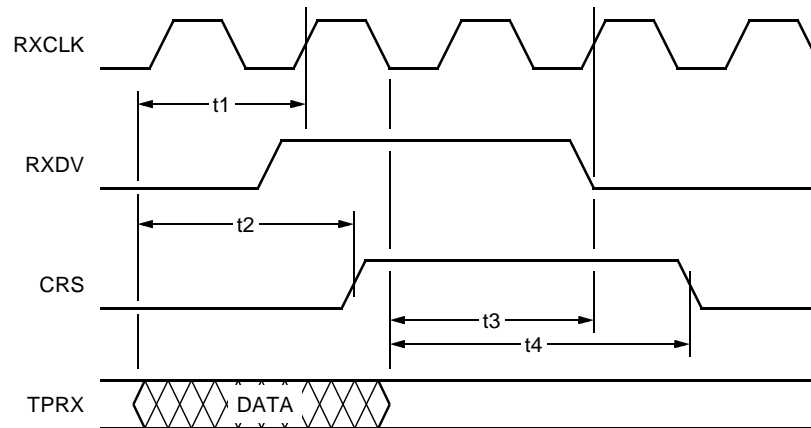
5-7918(F)

Figure 12. Receive Timing

Clock Timing (continued)

Table 39. Reset and Configuration Timing

Symbol	Parameter	Min	Max	Unit
t1	Power on to Reset High	0.5	—	ms
t2	Reset Pulse Width	0.5	—	ms
t3	Configuration Pin Setup	0.5	—	ms
t4	Configuration Pin Hold	0.5	—	ms
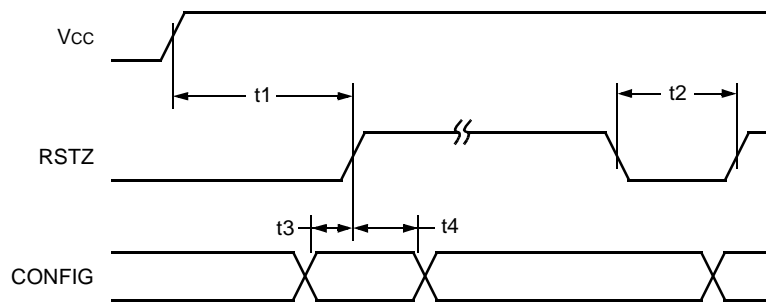
5-7919(F)

Figure 13. Reset and Configuration Timing

Clock Timing (continued)

Table 40. PMD Characteristics

Symbol	Parameter	Min	Max	Unit
t1	TPTX+/TPTX– Rise Time	3	5	ns
t2	TPTX+/TPTX– Fall Time	3	5	ns
t3	TP Skew	0	0.5	ns
t4	FOTX+/FOTX– Rise Time	—	—	ns
t5	FOTX+/FOTX– Fall Time	—	—	ns
t6	FO Skew	—	—	ps
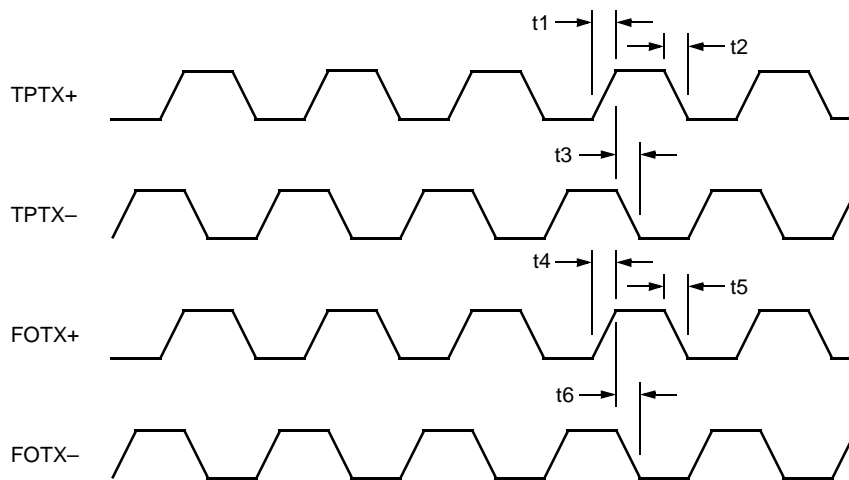
5-7920(F)

Figure 14. PMD Characteristics

Clock Timing (continued)
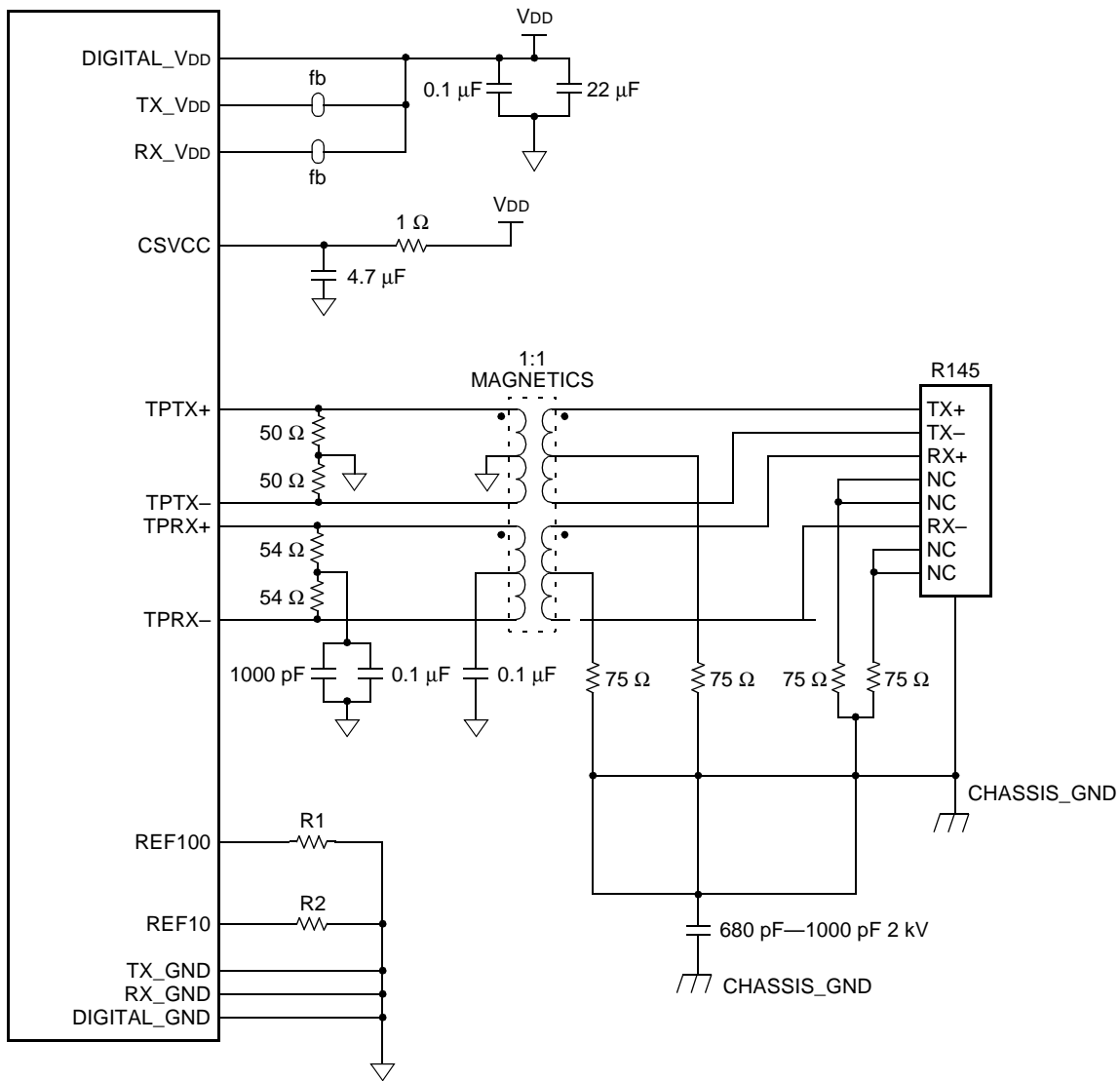
5-7510(F).r4

Figure 15. Connection Diagrams (10/100Base-TX Operation)

Outline Diagram

160-Pin PQFP 28 mm x 28 mm (measured in mm).

5-2132F).r13

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