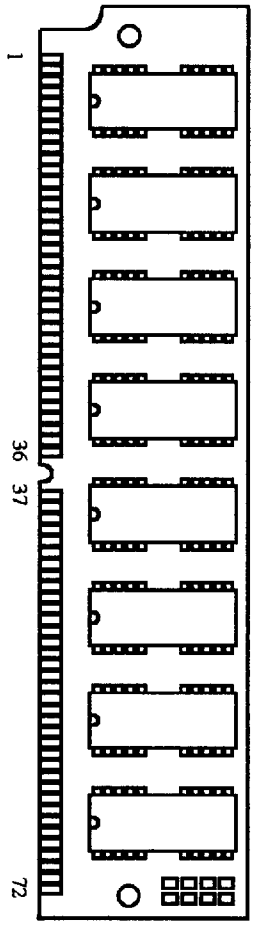
Description

The GMM7322010DS/SG is a 2M x 32 bits Dynamic RAM MODULE which is assembled 16 pieces of 1M x 4bit EDO DRAMs in 24 pin SOJ package on both sides the printed circuit board with decoupling capacitors. The GMM7322010DS/SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. The GMM7322010DS/SG provides common data inputs and Extended Data outputs.

• **GMM7322010DS/SG** (Both Side)



Features

- 72 pins Single In-Line Package
  - GMM7322010DS : Solder plating
  - GMM7322010DSG : Gold plating
- Extended Data Out(EDO) Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

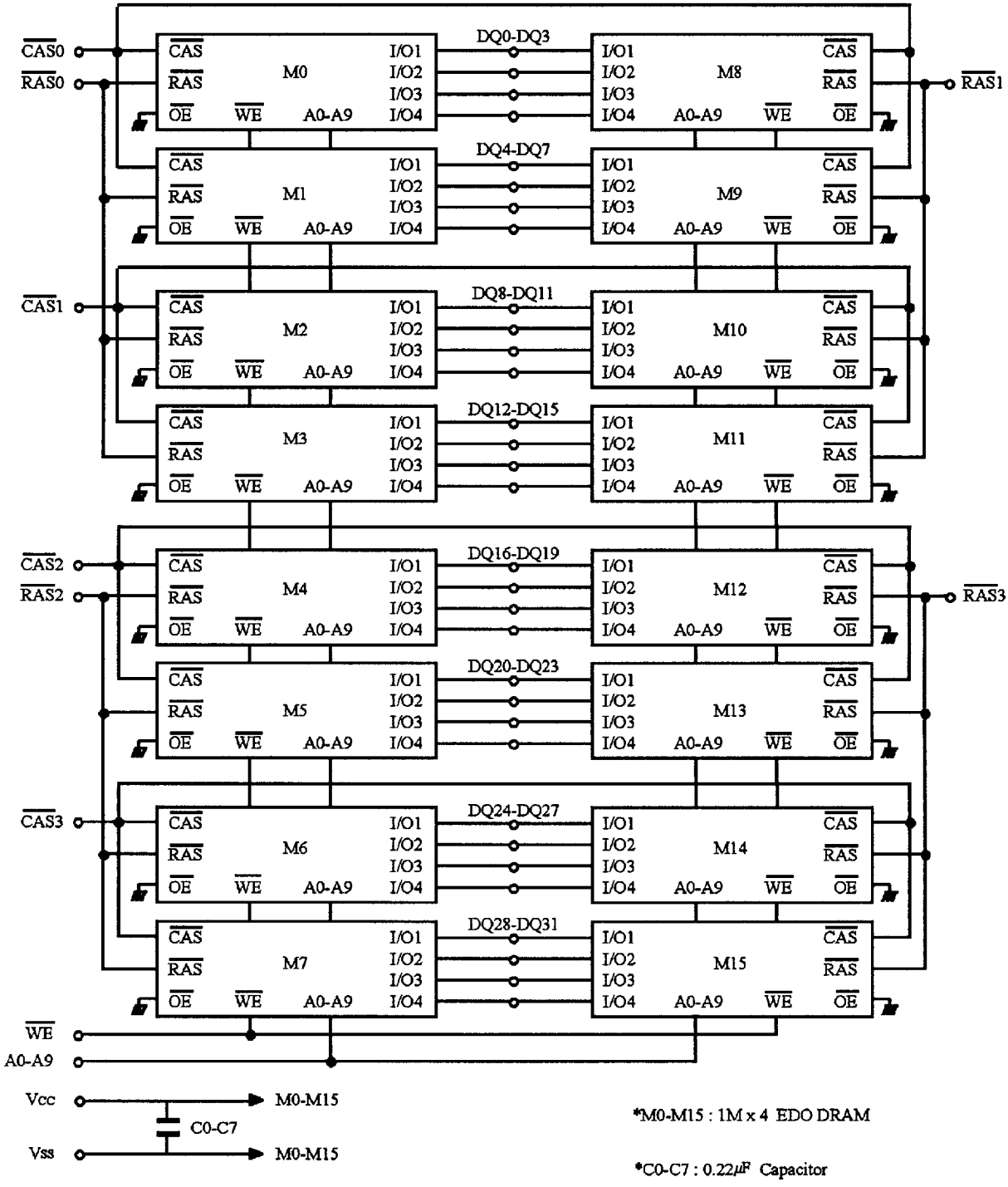
	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GMM7322010DS/SG-60	60	15	104	25
GMM7322010DS/SG-70	70	18	124	30
GMM7322010DS/SG-80	80	20	144	35

- Low Power
  Active : 3,564/3,124/2,904 mW (MAX)
  Standby : 88mW (CMOS level : MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/ 16㎳

Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS_2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS_3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS_1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS_1}$	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	PD_1
14	A_2	32	A_9	50	DQ_{24}	68	PD_2
15	A_3	33	$\overline{RAS_3}$	51	DQ_9	69	PD_3
16	A_4	34	$\overline{RAS_2}$	52	DQ_{25}	70	PD_4
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

Block Diagram



*M0-M15 : 1M x 4 EDO DRAM

*C0-C7 : 0.22μF Capacitor

Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	PD1-PD4	Presence Detect
DQ0-DQ31	Data Input/Output	Vcc	Power (+5V)
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe	Vss	Ground
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable		

Presence Detect Pins (Optional)

Pin	60ns	70ns	80ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	Vss	NC
PD4	NC	NC	Vss

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to Vss	-1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	16	W

*Note: 1. Stress greater than above "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended DC Operating Conditions ($T_A = 0 \sim 70℃$)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	-	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	1

*Note: 1. All voltages referenced to Vss.

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	-	648	mA	1, 2
		70ns	-	568		
		80ns	-	528		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		-	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	-	648	mA	2
		70ns	-	568		
		80ns	-	528		
I_{CC4}	Extended Data Out Mode Current Average Power Supply Current Extended Data Out Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	60ns	-	648	mA	1, 3
		70ns	-	568		
		80ns	-	528		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}-0.2V)		-	16	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	648	mA	
		70ns	-	568		
		80ns	-	528		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	80	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		-160	160	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		-20	20	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, T_A = 25℃, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (A0~A9)	-	100	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$)	-	132	pF	1, 2
C_{I3}	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	-	36	pF	1, 2
C_{I4}	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	-	36	pF	1, 2
$C_{I/O}$	I/O Capacitance (DQ0~DQ31)	-	30	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃, Notes 1, 15)

The GMM7322010DS/SG writes data only in early write cycle (twcs ≥ twcs(min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	GMM7322010 DS/SG-60		GMM7322010 DS/SG-70		GMM7322010 DS/SG-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	144	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	12	10,000	15	10,000	15	10,000	ns	
t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Coumn Address Setup Time	0	-	0	-	0	-	ns	
t_{CAH}	Coumn Address Hold Time	10	-	13	-	15	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	9
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	48	-	58	-	68	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	8
t_{REF}	Refresh Period (1024 Cycles)	-	16	-	16	-	16	ms	

Read Cycle

Symbol	Parameter	GMM7322010 DS/SG-60		GMM7322010 DS/SG-70		GMM7322010 DS/SG-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	3, 4
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	3, 5, 14
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	6
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	0	-	ns	6
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	18	-	23	-	28	-	ns	
t_{OFF}	Output Buffer Turn-off Time from $\overline{CAS}$	-	15	-	20	-	20	ns	7
t_{OFR}	Output Buffer Turn-off Time to $\overline{RAS}$	-	15	-	15	-	15	ns	7,17
t_{WEZ}	Output BufferTurn-off Time to $\overline{WE}$	-	15	-	15	-	15	ns	7
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	ns	
t_{OHR}	Output Data Hold Time form $\overline{RAS}$	5	-	5	-	5	-	ns	
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{RCHA}	Read Command Hold Time from Column Address	30	-	35	-	40	-	ns	

Write Cycle

Symbol	Parameter	GMM7322010 DS/SG-60		GMM7322010 DS/SG-70		GMM7322010 DS/SG-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	13	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	12
t_{DH}	Data-in Hold Time	10	-	13	-	15	-	ns	12

Refresh Cycle

Symbol	Parameter	GMM7322010 DS/SG-60		GMM7322010 DS/SG-70		GMM7322010 DS/SG-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time in Normal Mode	10	-	10	-	10	-	ns	

Extended Data Out (EDO) Mode Cycle

Symbol	Parameter	GMM7322010 DS/SG-60		GMM7322010 DS/SG-70		GMM7322010 DS/SG-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPC}	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
t_{CP}	EDO Mode $\overline{CAS}$ Precharge Time	8	-	10	-	15	-	ns	
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	60	100,000	70	100,000	80	100,000	ns	16
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	3,14
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{RCHC}	Read Command Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{DOH}	Output Data Hold Time from $\overline{CAS}$ Low	5	-	5	-	5	-	ns	

Notes:

1. AC measurements assume t_T = 2ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
7. $t_{OFF}(max)$, $t_{OFR}(max)$ and $t_{WEZ}(max)$ defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
10. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
11. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
13. t_{RASC} is defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
16. t_{RASP} defines $\overline{RAS}$ pulse width in extended data out mode cycles.
17. t_{OFF} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.

Timing Waveforms

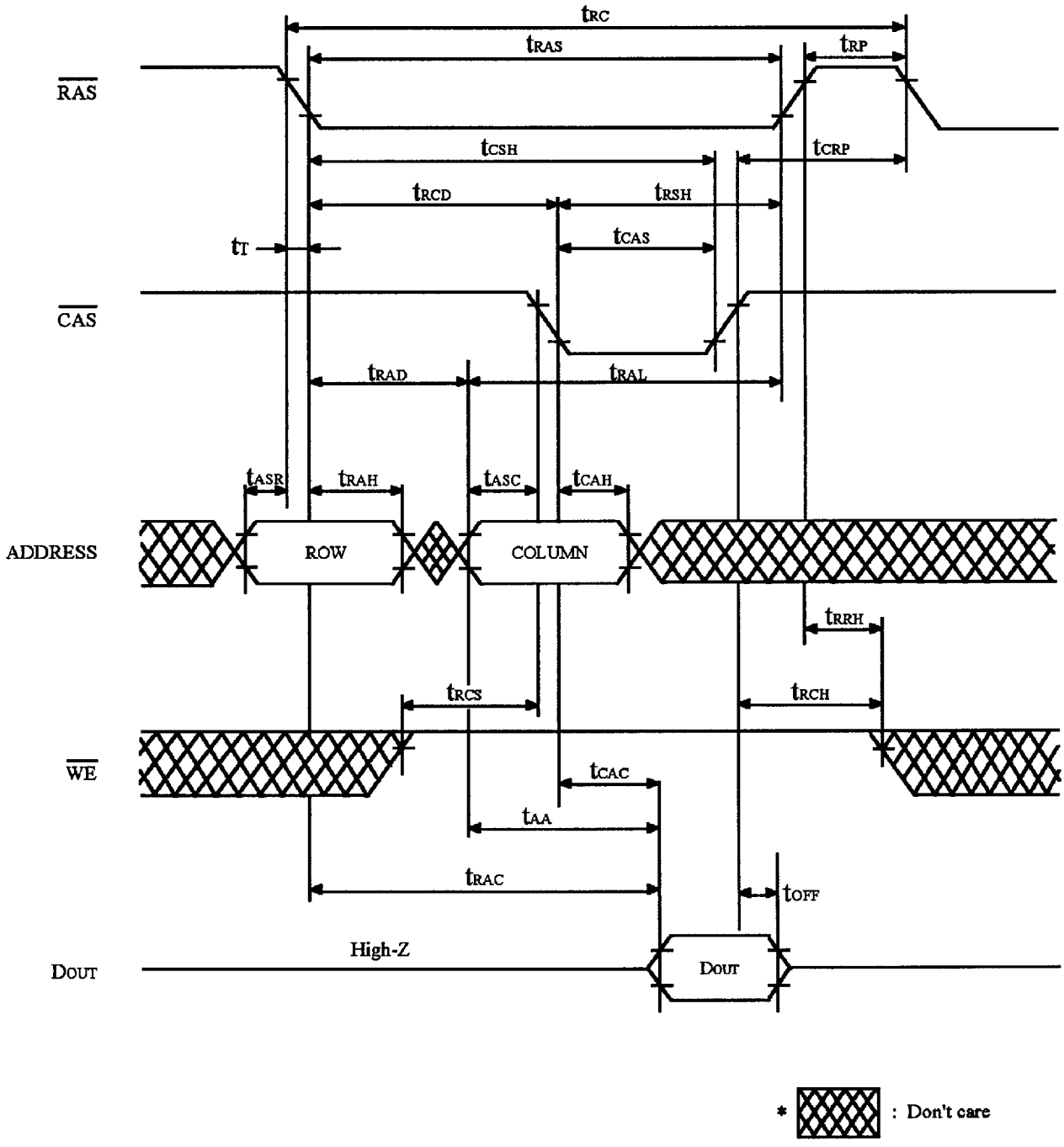


FIGURE 1. READ CYCLE

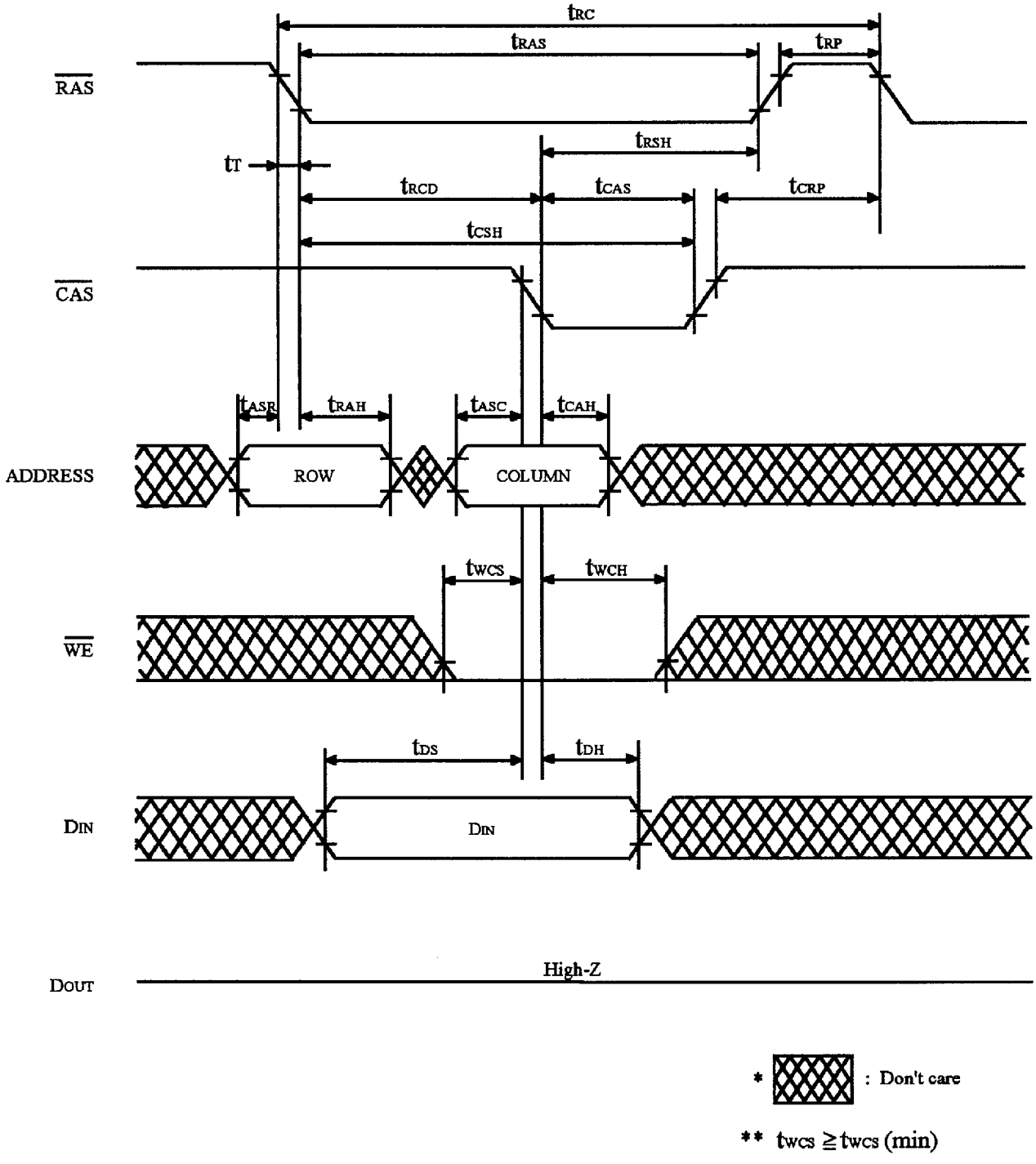


FIGURE 2. EARLY WRITE CYCLE

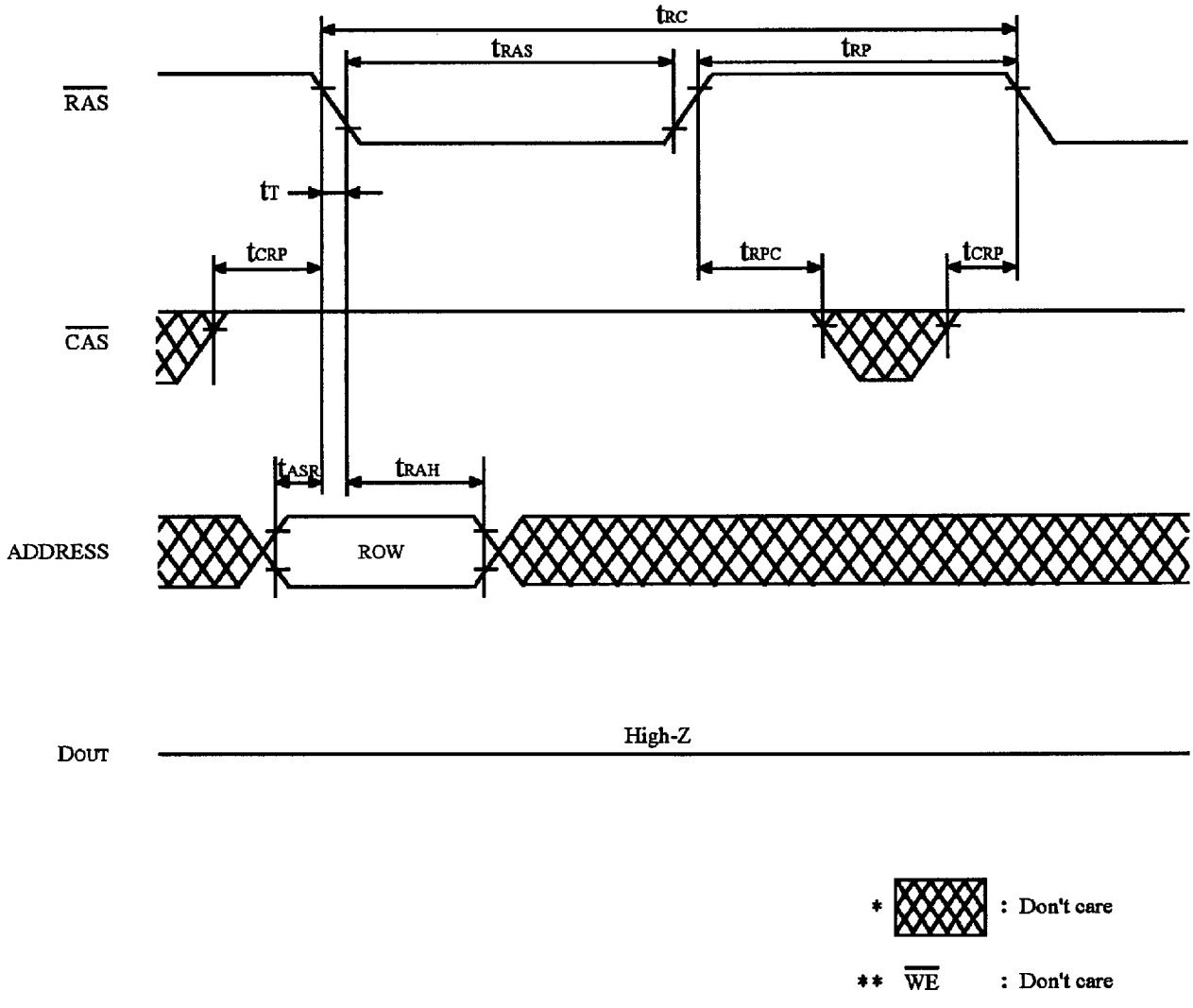
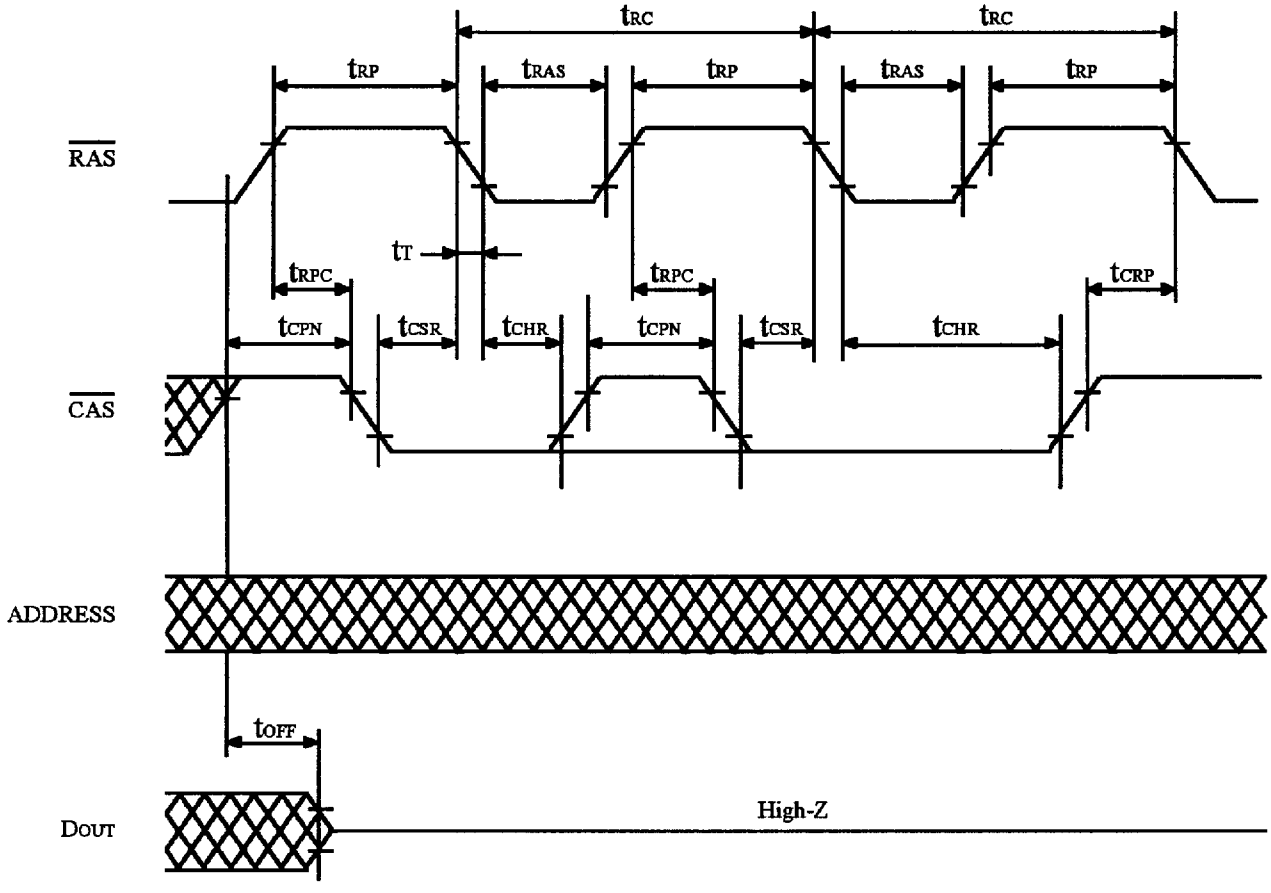


FIGURE 3. $\overline{RAS}$ ONLY REFRESH CYCLE



* : Don't care

* * $\overline{WE}$: V_{IH}

FIGURE 4. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

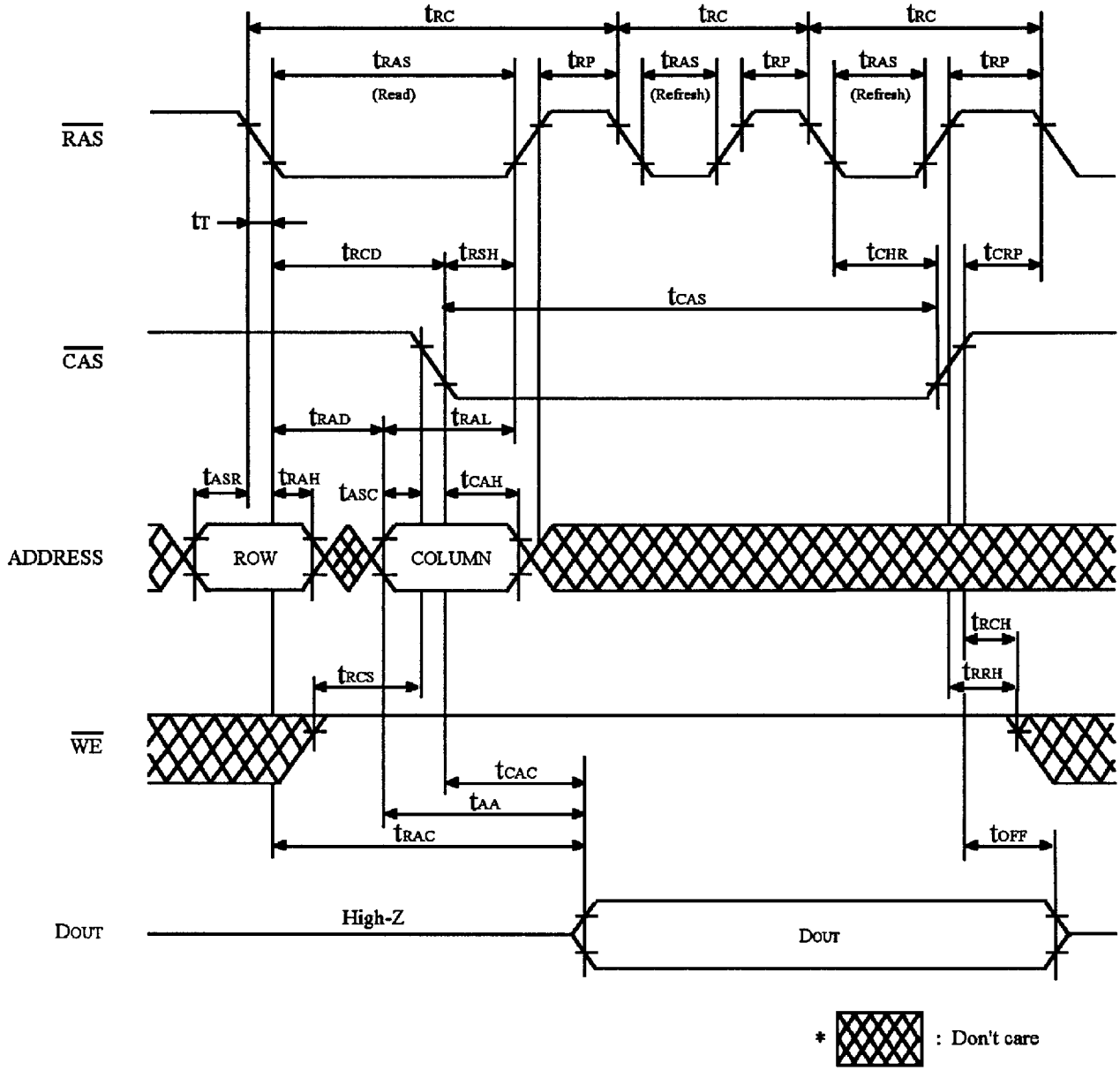


FIGURE 5. HIDDEN REFRESH CYCLE

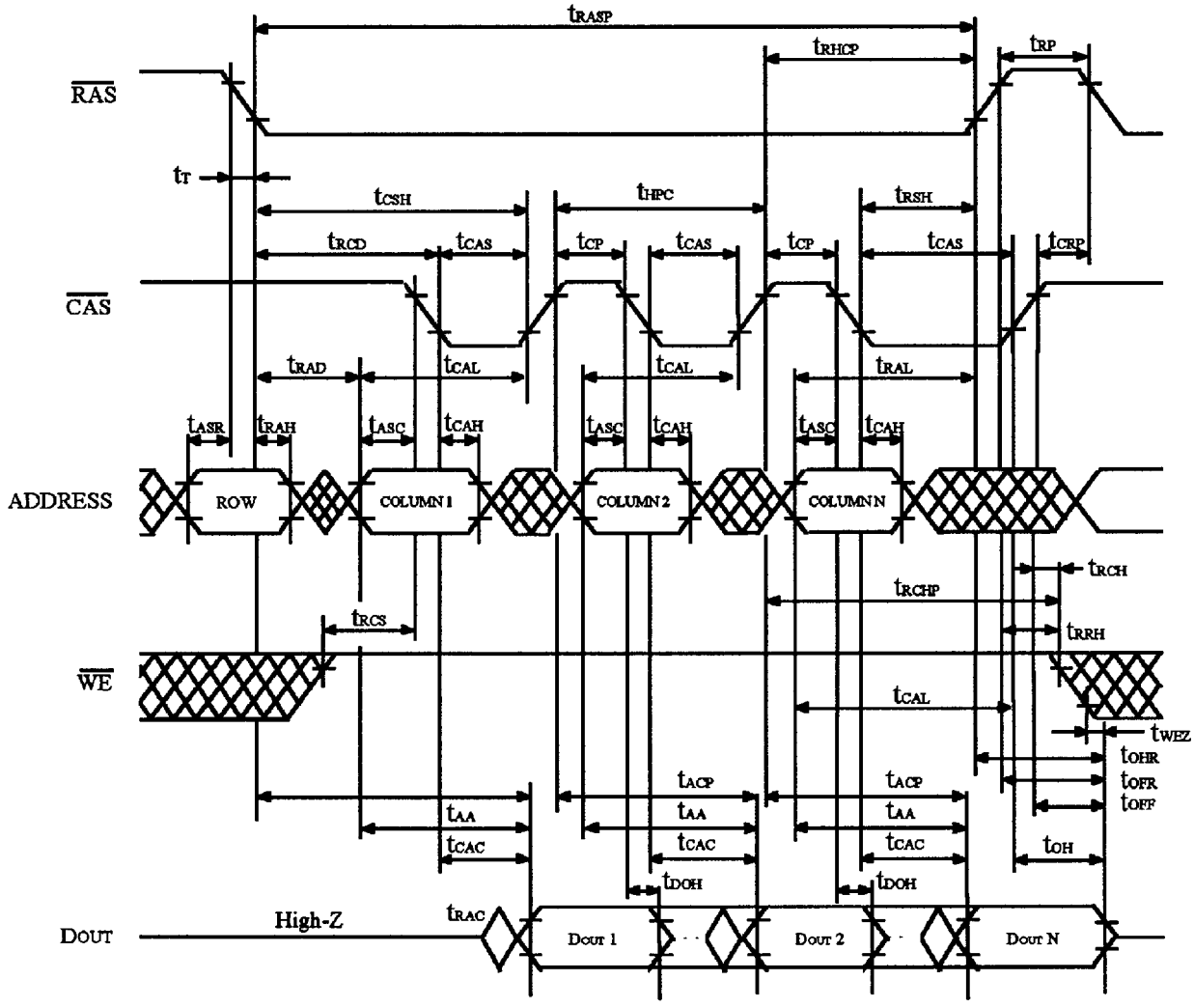


FIGURE 6. EXTENDED DATA OUT MODE READ CYCLE

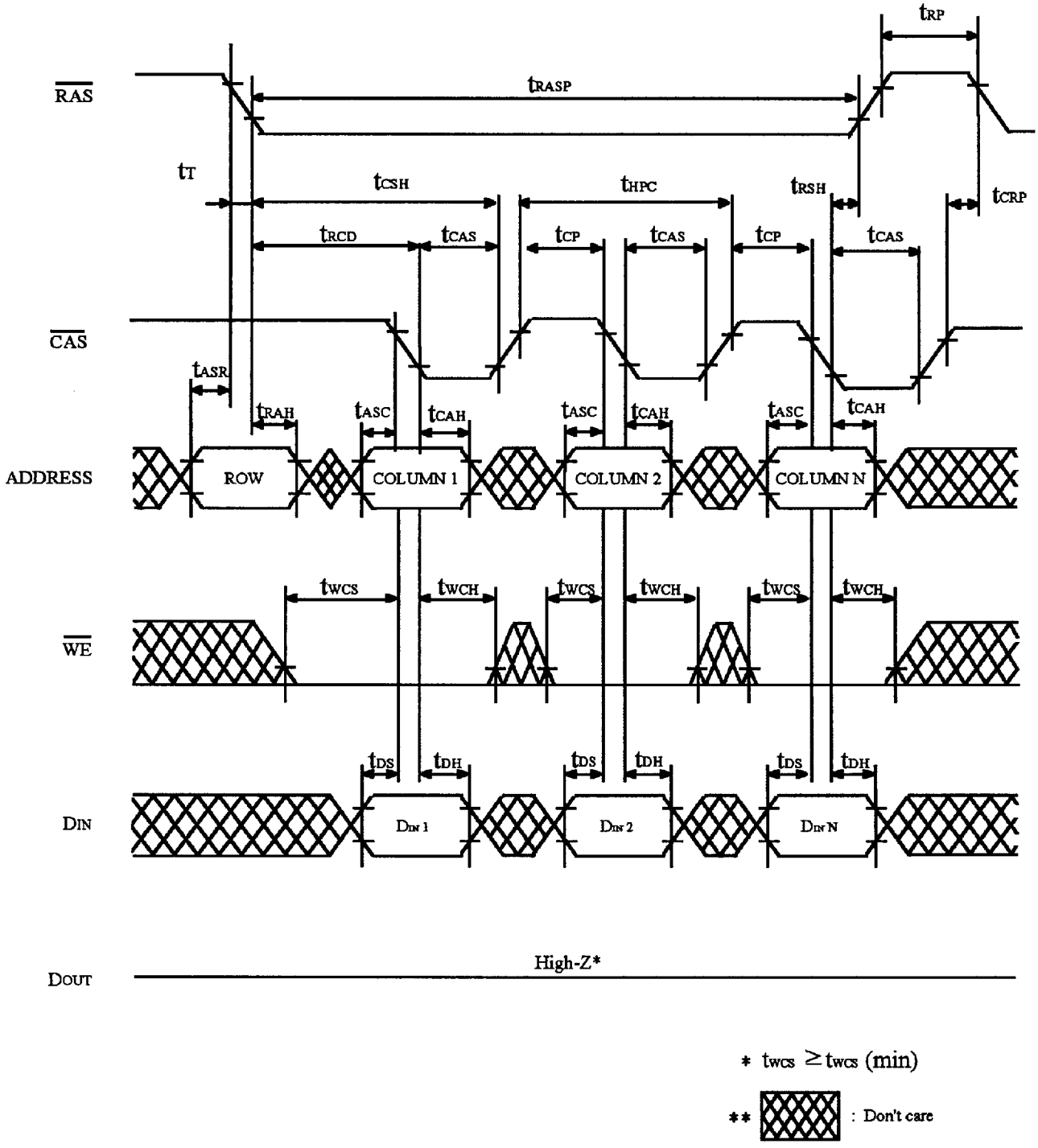
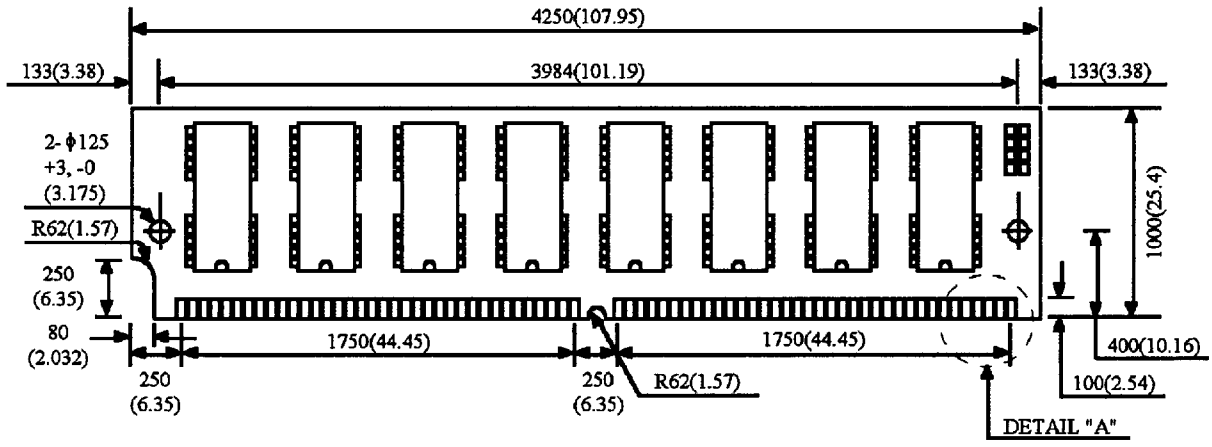


FIGURE 7. EXTENDED DATA OUT MODE EARLY WRITE CYCLE

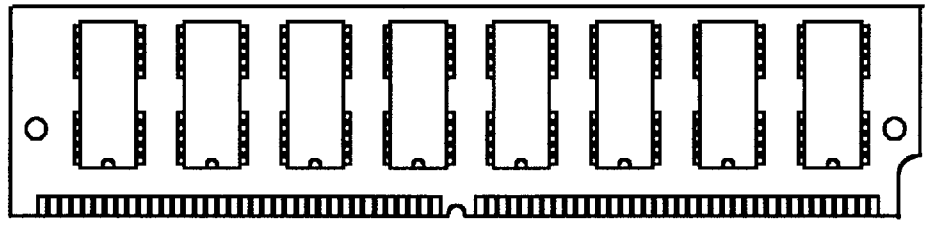
Package Dimension

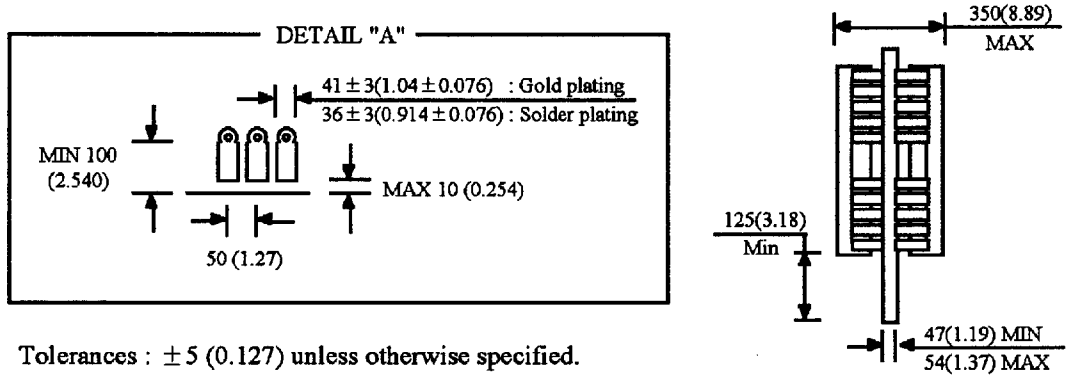
Unit: mil (mm)
* (1mil = 1/1000 inches)

Front



Rear





Tolerances : ±5 (0.127) unless otherwise specified.