a6402

## Universal Asynchronous Receiver/Transmitter

Features

- a6402 MegaCore function implementing a universal asynchronous receiver/transmitter (UART)
- Optimized for FLEX® and MAX® architectures
- Uses approximately 162 FLEX logic elements (LEs)
- Programmable word length, stop bits, and parity
- Full duplex operation
- Includes status flags for parity, framing, and overrun errors
- Functionally based on the Harris HD-6402 device, except as noted in the "Variations & Clarifications" section on page 63

General Description

The a6402 MegaCore function implements a universal asynchronous receiver/transmitter (UART), which provides an interface between a microprocessor and a serial communications channel. See Figure 1.

Figure 1. a6402 Symbol
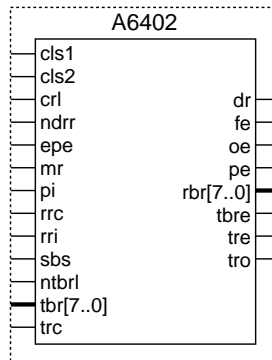
Ports

shows the input and output ports for the `a6402`.

Name	Type	Polarity	Description
cls1 cls2	Input	–	Character length select bits. These bits determine the length of the data word. 00 = 5-bit word format 01 = 6-bit word format 10 = 7-bit word format 11 = 8-bit word format
crl	Input	High	Control register load. Controls how the data word is loaded into the control register.
ndrr	Input	Low	Data received reset. Clears the `dr` output.
epe	Input	High/low	Even parity enable. When high, even parity; when low, odd parity.
mr	Input	High	Master reset. Clears the `pe`, `fe`, `dr`, and `oe` outputs, and asserts the `tre` and `tbre` outputs.
pi	Input	High	Parity inhibit. When `pi` is asserted, parity is neither generated nor checked.
rrc	Input	–	Receiver register clock. Operates at 16 times the receive data rate.
rri	Input	–	Receiver register input. Serial input data.
sbs	Input	High/low	Stop bit select. When high, `sbs` generates 2 stop bits (1.5 stop bits for 5-bit format); when low, `sbs` generates 1 stop bit.
ntbrl	Input	Low	Transmitter buffer register load. Enables load of the transmitter buffer register.
tbr[7..0]	Input	–	Transmitter buffer register input bus.
trc	Input	–	Transmitter register clock. Operates at 16 times the transmit data rate.
dr	Output	High	Data received. Indicates that a data word has been transferred to the receiver buffer register.
fe	Output	High	Framing error. Asserted when the expected stop bit(s) is not detected.
oe	Output	High	Overrun error. Asserted when data in the receiver buffer register is overwritten while the `dr` output is still asserted.
pe	Output	High/low	Parity error. Set when the calculated parity does not match the received parity. When `pi` is asserted, `pe` is set low.
rbr[7..0]	Output	–	Receiver buffer register bus.
tbre	Output	High	Transmitter buffer register empty. Indicates that the transmitter buffer register is empty.
tre	Output	High	Transmitter register empty. Indicates that the data word is completely transmitted out of the transmitter register.
tro	Output	–	Transmitter register output. Serial output data.

Table 1. a6402 Ports

Configurations

The a6402 receives and transmits data in a variety of configurations, including 5-, 6-, 7-, or 8-bit data words; odd, even, or no parity; and 1, 1.5, or 2 stop bits. Table 2 shows the available configuration options.

Table 2. a6402 Available Configurations

| Character Format				Control Word				
Data Bits	Parity Bit	Start Bit	Stop Bits	cls2	cls1	pi	epe Note (1)	sbs
5	Odd	1	1	0	0	0	0	0
	Odd	1	1.5	0	0	0	0	1
	Even	1	1	0	0	0	1	0
	Even	1	1.5	0	0	0	1	1
	None	1	1	0	0	1	X	0
	None	1	1.5	0	0	1	X	1
6	Odd	1	1	0	1	0	0	0
	Odd	1	2	0	1	0	0	1
	Even	1	1	0	1	0	1	0
	Even	1	2	0	1	0	1	1
	None	1	1	0	1	1	X	0
	None	1	2	0	1	1	X	1
7	Odd	1	1	1	0	0	0	0
	Odd	1	2	1	0	0	0	1
	Even	1	1	1	0	0	1	0
	Even	1	2	1	0	0	1	1
	None	1	1	1	0	1	X	0
	None	1	2	1	0	1	X	1
8	Odd	1	1	1	1	0	0	0
	Odd	1	2	1	1	0	0	1
	Even	1	1	1	1	0	1	0
	Even	1	2	1	1	0	1	1
	None	1	1	1	1	1	X	0
	None	1	2	1	1	1	X	1

Note:
(1)   The X indicates "don't care."

Functional Description

Figure 2 shows a block diagram of the a6402.

Figure 2. a6402 Block Diagram
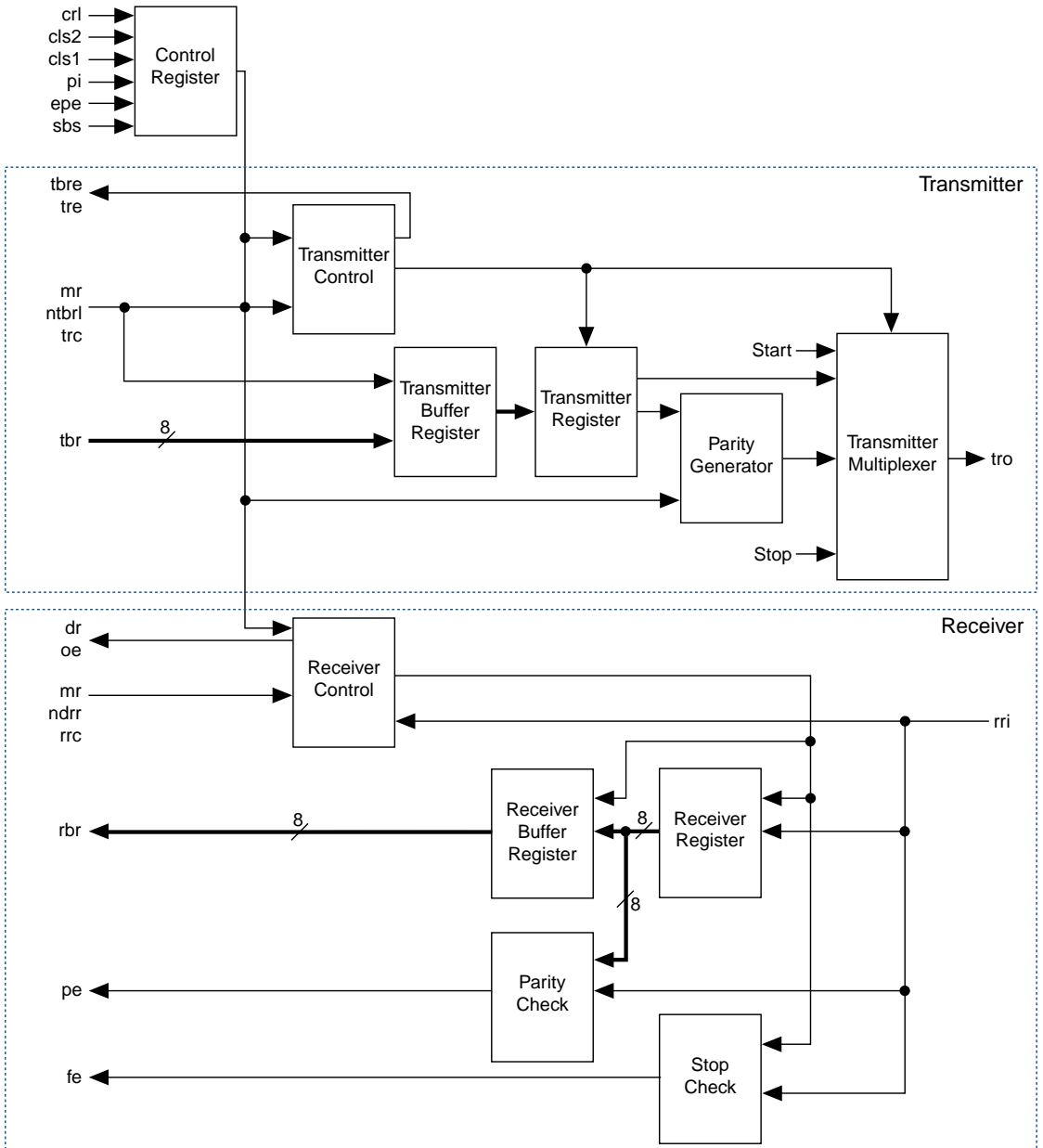
Master Reset

When the `mr` input is asserted, the `pe`, `fe`, `oe`, and `dr` outputs are asynchronously cleared and `tbre` and `tre` are asserted. The assertion of `mr` also sets all state machines to a default idle state. This condition does not affect the receiver buffer register. The `mr` input must be pulsed high at least once after power-up. When `mr` is deasserted, normal operation resumes at the next rising edge of `trc` or `rrc`.

☞ Once the `pe`, `fe`, and `oe` outputs are set, the only exit condition available is through asserting `mr`.

Control Register

The control register contains the configuration of the data word, including the number of bits, calculated parity, and the number of stop bits. The `crl` input, an active high register enable, controls how the data word is loaded into the control register. When `crl` is asserted, the `cls2`, `cls1`, `pi`, `epe`, and `sbs` inputs are loaded on the next rising edge of the `trc` input.

Transmitter

The transmitter consists of the following elements:

■ *Transmitter control*—The transmitter control contains three interconnected state machines. The first state machine regulates the baud rate by performing a divide-by-16 operation on the `trc` input. The second state machine detects the low-to-high transition on `ntbrl`, starts the serial transmission through `tro`, transfers data from the transmitter buffer register to the transmitter register, and generates the status signals `tbre` and `tre`. The third state machine controls the multiplexing of data bits to the `tro` output.

■ *Transmitter buffer register*—The transmitter buffer register is loaded via `ntbrl`, an active-low register enable, that causes `tbr[7..0]` to be loaded from the microprocessor on the next `trc` clock edge.

■ *Transmitter register*—The transmitter register loads the data from the transmitter buffer register and holds that data until transmission is complete.

■ *Parity generator*—The parity generator calculates the appropriate parity value depending on the epe input (even or odd parity) and the cls inputs (data word length).

■ *Transmitter multiplexer*—The transmitter multiplexer selects a single-bit data value and drives the tro output. Inputs to the transmitter multiplexer include the start bit, all eight bits from the transmitter register, the parity bit, and a stop or idle bit.
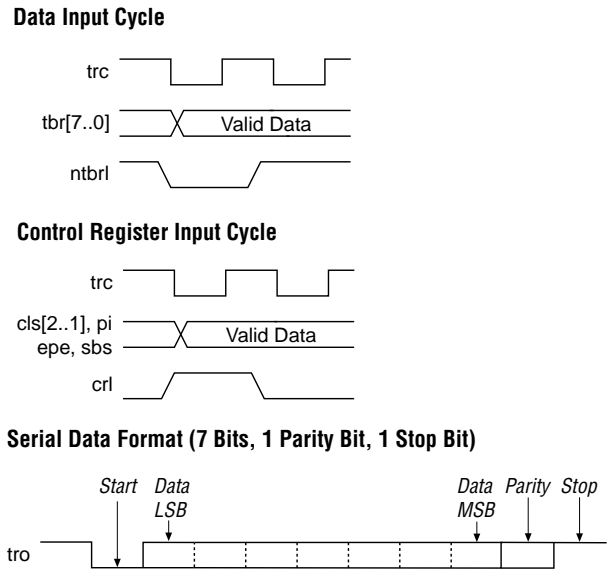
Receiver

The receiver consists of the following elements:

■ *Receiver control*—The receiver control contains three interconnected state machines. The first state machine performs a divide-by-16 operation on the rrc clock to determine when to sample the rri serial input. The second state machine detects the high-to-low transition on rri, determines if a valid start bit has been received, transfers data from the receiver register to the receiver buffer register, and generates the status signals dr and oe. The third state machine loads the individual bits of the receiver register and the fe and pe outputs.

■ *Receiver register*—The receiver register loads the number of data bits determined by the cls inputs. If the data word is less than eight bits, the data is right-justified with the MSBs filled with logic lows. When the stop bit is detected, the receiver register transfers its contents to the receiver buffer register.

■ *Parity check*—The parity check calculates the parity of the data word and the parity bit. If an error occurs, the pe output is asserted. Once asserted, the pe output can only be cleared by asserting the mr input.

■ *Stop check*—The stop check samples the middle of the first expected stop bit. If an error occurs, the fe output is asserted. Once asserted, the fe output can only be cleared by asserting the mr input.

Timing Waveforms

Figure 3 shows the timing waveforms for the a6402.

Figure 3. a6402 Functional Timing Waveforms

Data Input Cycle

trc

tbr[7..0]   Valid Data

ntbrl

Control Register Input Cycle

trc

cls[2..1], pi
epe, sbs   Valid Data

crl

Serial Data Format (7 Bits, 1 Parity Bit, 1 Stop Bit)

Start Data   Data Parity Stop
       LSB   MSB

tro

Variations & Clarifications

The following characteristics distinguish the Altera® a6402 from the Harris HD-6402:

- The a6402 does not contain the sfd and rrd inputs, and the outputs are not tri-stated.
- In the a6402, the control and transmitter buffer registers are implemented as registers and use trc as a clock source; these registers are implemented as latches in the HD-6402 device.
- In the a6402, after mr is deasserted, normal operation can resume on the next rrc or trc rising clock edge. In the HD-6402 device, normal operation does not resume for 18 clock cycles.
- Due to the synchronization process in the a6402, tbre is deasserted two clock cycles after the low-to-high transition of ntbrl. In the HD-6402 device, tbre is deasserted immediately after the low-to-high transition of ntbrl.
- In the a6402, the tro output is registered to remove glitches. This register uses trc as the clock source.
- Once the pe, fe, and oe outputs are asserted, the HD-6402 device has no exit condition other than through asserting mr.