

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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SHEET	22	23	24	25																					
REV STATUS OF SHEETS	REV SHEET																								
					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

<b>PMIC N/A</b>  <b>STANDARDIZED MILITARY DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  <b>AMSC N/A</b>	PREPARED BY <i>Kenneth Ricci</i>	<b>DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444</b>		
	CHECKED BY <i>Ray Morrison</i>	MICROCIRCUITS, DIGITAL, CMOS 16K X 4 SRAM, MONOLITHIC SILICON		
	APPROVED BY <i>[Signature]</i>	SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-86859</b>
	DRAWING APPROVAL DATE 20 JUNE 1988	SHEET 1 OF 25		
REVISION LEVEL				

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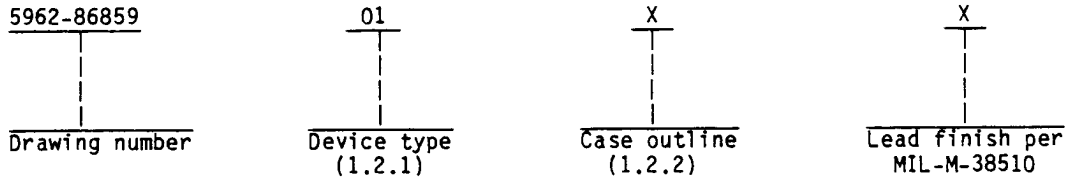
U.S. GOVERNMENT PRINTING OFFICE: 1987 - 748-129/60911  
5962-E140

**DISTRIBUTION STATEMENT A.** Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01			85 ns
02			85 ns
03			70 ns
04			70 ns
05			55 ns
06			55 ns
07			45 ns
08			45 ns
09			35 ns
10			35 ns
11	See 6.4	16K X 4 Static Ram	70 ns
12			70 ns
13			55 ns
14			55 ns
15			45 ns
16			45 ns
17			35 ns
18			35 ns
19			55 ns
20			55 ns
21			45 ns
22			45 ns
23			35 ns
24			35 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" X .420" X .090"), flat package
L	D-9 (24-lead, 1.280" X .310" X .200"), dual-in-line package
T	Figure 1 (22-lead, 1.260" X .310" X .140"), dual-in-line package
U	C-11A (28-terminal, .560" X .358" X .075"), leadless chip carrier package
W	D-7 (22-lead, 1.111" X .410" X .225"), dual-in-line package
X	C-11 (28-terminal, .560" X .358" X .120") leadless chip carrier package
Y	Figure 1 (22-lead, 1.110" X .310" X .175"), dual-in-line package
Z	Figure 1 (22-terminal, .490" X .290" X .080"), leadless chip carrier package

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1.3 Absolute maximum ratings.

Supply voltage range ( $V_{CC}$ )	- - - - -	-0.5 V dc to +7.0 V dc	1/
DC output current	- - - - -	20 mA	
Ambient storage temperature	- - - - -	-65°C to +150°C	
Temperature under bias	- - - - -	-55°C to +125°C	
Thermal resistance, junction-to-case ( $\theta_{JC}$ ):			
Cases K, L, U, W, and X	- - - - -	See MIL-M-38510, appendix C	
Cases Y and T	- - - - -	28°C/W	2/
Case Z	- - - - -	22°C/W	Z/
Power dissipation	- - - - -	1.0 W	

1.4 Recommended operating conditions.

Supply voltage ( $V_{CC}$ )	- - - - -	+4.5 V dc to +5.5 V dc	1/
Ground voltage ( $V_{SS}$ )	- - - - -	0 V dc	
Input high voltage ( $V_{IH}$ )	- - - - -	+2.2 V dc to $V_{CC} + 0.5$ V dc	
Input low voltage ( $V_{IL}$ )	- - - - -	-0.5 V dc to 0 V dc	3/
Operating case temperature range ( $T_C$ )	- - - - -	-55°C to +125°C	

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

- 1/ All voltages referenced to  $V_{SS}$ .
- Z/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value stated herein.
- 3/  $V_{IL}$  negative undershoots to a minimum of -2.0 V dc are allowed with a maximum 20 ns pulse width.

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### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth tables. The truth tables shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (reference MIL-M-38510, paragraph 3.1.3.8) shall be subjected to and pass the internal moisture content test, (test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C < T <sub>C</sub> < +125°C V <sub>SS</sub> = 0 V, 4.5 V < V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input leakage current	I <sub>LI</sub>	V <sub>CC</sub> = max, V <sub>IN</sub> = GND to V <sub>CC</sub>	1,2,3	A11		10	uA
Output leakage current	I <sub>LO</sub>	V <sub>CC</sub> = max, V <sub>OUT</sub> = GND to V <sub>CC</sub> CE ≥ V <sub>IH</sub> WE ≤ V <sub>IL</sub>	1,2,3	A11		10	uA
Output low voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 8 mA V <sub>IL</sub> = 0.8 V; V <sub>IH</sub> = 2.2 V	1,2,3	A11		0.4	V
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -4 mA V <sub>IL</sub> = 0.8 V; V <sub>IH</sub> = 2.2 V	1,2,3	A11	2.4		V
Operating supply current	I <sub>CC1</sub>	CE = V <sub>IL</sub> , outputs open V <sub>CC</sub> = max, f = 1/t <sub>AVAX</sub>	1,2,3	01,03,05, 07,09		140	mA
				02,04,06, 08,10, 17-20		115	
				11-16, 21-24		90	
Standby power supply current (TTL)	I <sub>CC2</sub>	CE ≥ V <sub>IH</sub> , outputs open V <sub>CC</sub> = max	1,2,3	01-10		50	mA
				11-24		30	
Standby power supply current (CMOS)	I <sub>CC3</sub>	V <sub>CC</sub> + 0.2 V ≥ CE ≥ V <sub>CC</sub> - 0.2 V outputs open V <sub>CC</sub> + 0.2 V ≥ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or +0.2 V ≥ V <sub>IN</sub> ≥ -0.2 V	1,2,3	A11		25	mA
Data retention current	I <sub>CC4</sub> 1/	V <sub>CC</sub> = V <sub>DR</sub> = 2.0 V	1,2,3	02,04,06, 08,10,11, 13,15,17, 19,21,23,		1000	uA
Input capacitance	C <sub>I</sub> 1/	V <sub>I</sub> = 5.0 V or GND f = 1 MHz, T <sub>C</sub> = +25°C See 4.3.1c	4	A11		8	pF
Output capacitance	C <sub>O</sub> 1/	V <sub>O</sub> = 5.0 V or GND f = 1 MHz, T <sub>C</sub> = +25°C See 4.3.1c	4	A11		10	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>3/ 4/</sup> -55°C < T <sub>C</sub> < +125°C V <sub>SS</sub> = 0 V, 4.5 V < V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle time	t <sub>AVAX</sub> <u>1/ 2/</u>		9,10,11	01,02	85		ns
				03,04,11, 12	70		
				05,06,13, 14,19,20	55		
				07,08,15, 16,21,22	45		
				09,10,17, 18,23,24	35		
Address cycle time	t <sub>AVQV</sub> <u>2/</u>		9,10,11	01,02		85	ns
				03,04,11, 12		70	
				05,06,13, 14,19,20		55	
				07,08,15, 16,21,22		45	
				09,10,17, 18,23,24		35	
Chip-enable access time	t <sub>ELQV</sub> <u>1/ 2/</u>		9,10,11	01,02		85	ns
				03,04,11, 12		70	
				05,06,13, 14,19,20		55	
				07,08,15, 16,21,22		45	
				09,10,17, 18,23,24		35	
Output hold from address change	t <sub>AVQX</sub> <u>1/ 2/</u>		9,10,11	All	3		ns
Chip select to power up time	t <sub>PU</sub> <u>5/</u>		9,10,11	All	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions <sup>3/</sup> <sup>4/</sup> -55°C < T <sub>C</sub> < +125°C V <sub>SS</sub> = 0 V, 4.5 V < V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip deselect to power down time	t <sub>PD</sub> <sup>5/</sup>		9,10,11	01,02		85	ns
				03,04,11, 12		70	
				05,06,13, 14,19,20		55	
				07,08,15, 16,21,22		45	
				09,10,17, 18,23,24		35	
Output enable to output valid	t <sub>OLQV</sub> <sup>2/</sup>		9,10,11	01-06		55	ns
				07-18		35	
Chip select to output in low Z	t <sub>ELOX</sub> <sup>1/</sup> <sup>2/</sup> <sup>6/</sup>		9,10,11	A11	3		ns
Output enable to output in low Z	t <sub>OLOX</sub> <sup>1/</sup> <sup>2/</sup> <sup>6/</sup>		9,10,11	01-18	3		ns
Chip select to output in high Z	t <sub>EHQZ</sub> <sup>1/</sup> <sup>2/</sup> <sup>6/</sup>		9,10,11	01-24		30	ns
Output disable to output in high Z	t <sub>OHQZ</sub> <sup>1/</sup> <sup>2/</sup> <sup>6/</sup>		9,10,11	01-18		30	ns
Write enable to output in high Z	t <sub>WLOZ</sub> <sup>1/</sup> <sup>2/</sup> <sup>6/</sup>			01-06,11, 12		40	ns
				07-10, 13-24		20	
Data valid to end of write	t <sub>DVWH</sub> <sup>2/</sup>		9,10,11	01-24	35		ns
Data hold time	t <sub>WHDX</sub> <sup>2/</sup>		9,10,11	01-24	5		ns
Output active from end of write	t <sub>WHQV</sub> <sup>1/</sup> <sup>2/</sup> <sup>6/</sup>		9,10,11	01-24	3		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ 3/ 4/ -55°C < T <sub>C</sub> < +125°C V <sub>SS</sub> = 0 V, 4.5 V ≤ V <sub>CC</sub> < 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write-cycle time 1/	t <sub>AVAV</sub>		9,10,11	01,02	75		ns
				03,04,11, 12	60		
				05,06,13, 14,19,20	55		
				07,08,15, 16,21,22	45		
				09,10,17, 18,23,24	35		
Chip-select to end of write	t <sub>ELWH</sub> 4/		9,10,11	01,02	75		ns
				03,04,11, 12	60		
				05,06,13, 14,19,20	50		
				07,08,15, 16,21,22	40		
				09,10,17, 18,23,24	30		
Address valid to end of write	t <sub>AVWH</sub>			01-04, 11,12	75		ns
				05-10, 13-24	40		
Address-setup time	t <sub>AVWL</sub>		9,10,11	01-24	5		ns
Write pulse width	t <sub>WLWH</sub>			01-04, 11,12	75		ns
				05-10, 13-24	40		
Write recovery time	t <sub>EHOL</sub>		9,10,11	01-24	5		ns

See footnotes on next page.

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- 1/ This parameter tested initially and after any design or process change which could affect this parameter, and is therefore guaranteed to the limits specified in table I.
- 2/ For timing waveforms, see figure 4.
- 3/ AC parameters are tested using input rise and fall times of 5 ns and input pulse levels of GND to 3.0 V. Both input and output timing reference levels are 1.5 V, and the output load is shown on figure 5.
- 4/ On devices with two chip selects, both chip selects must be active low for the device to be selected.
- 5/ This parameter if not tested, shall be guaranteed to the limits specified in table I.
- 6/ Transition is measured  $\pm 500$  mV from steady state.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

##### 4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ( $C_I$  and  $C_O$  measurement) shall be measured only for the initial test and after any process or design changes which may affect capacitance.

d. Subgroup 7 and 8 tests sufficient to verify the truth tables.

##### 4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2)  $T_A = +125^\circ\text{C}$ , minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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Case Y

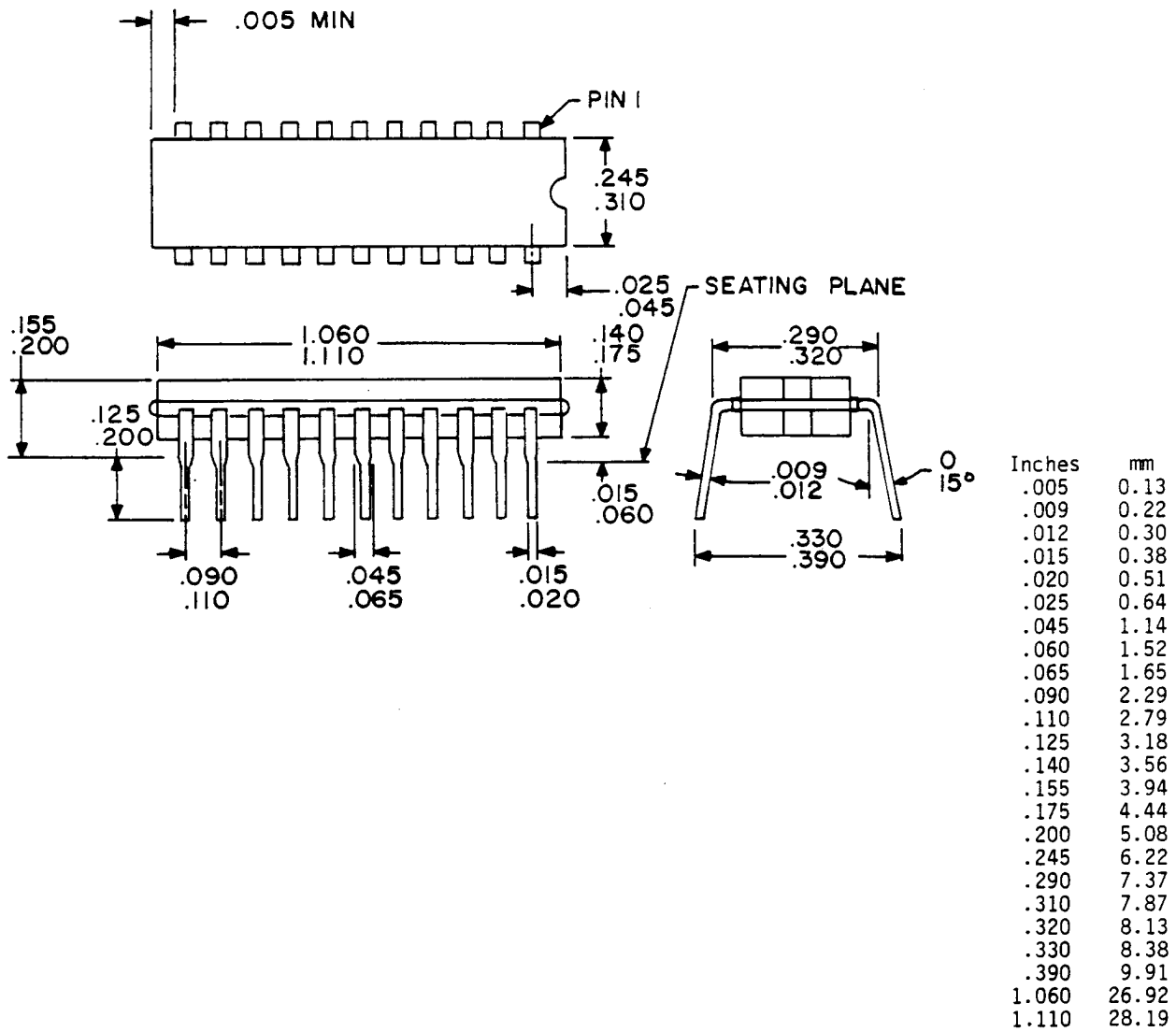


FIGURE 1. Case Outlines.

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DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
**A**

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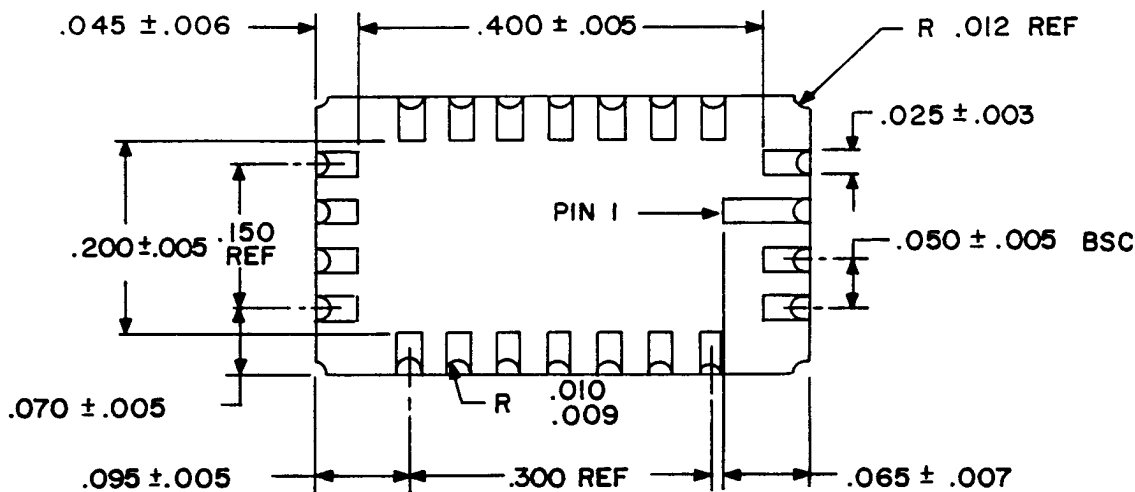
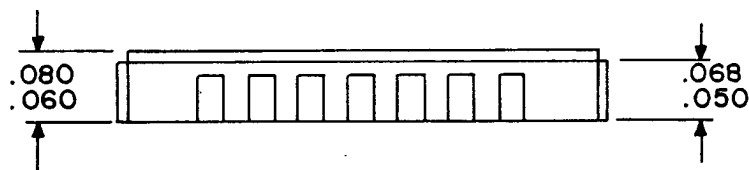
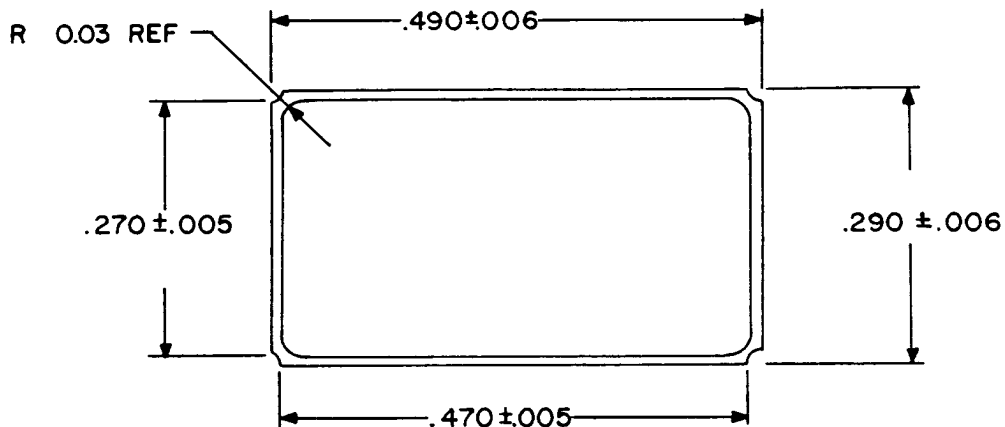
SHEET

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Case Z



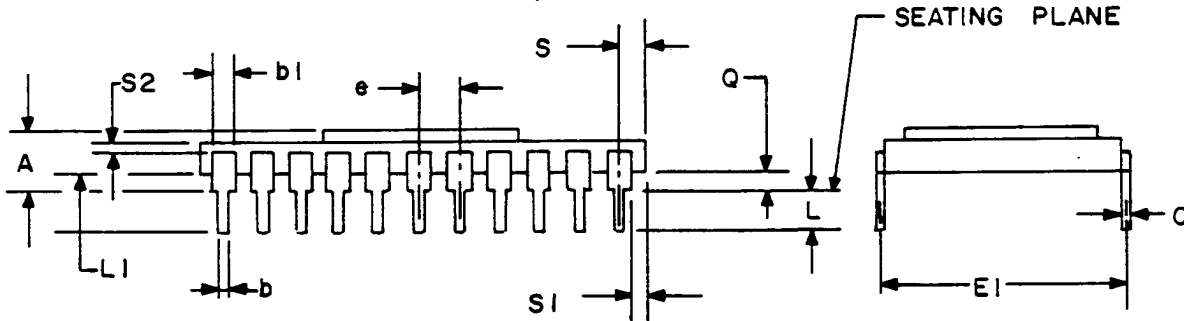
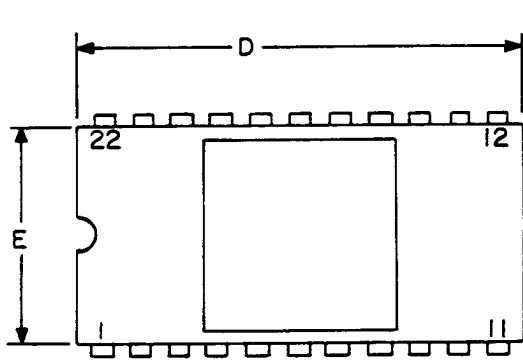
Inches	mm
.003	0.08
.005	0.13
.006	0.15
.007	0.18
.009	0.23
.010	0.25
.012	0.30
.025	0.64
.030	0.76
.045	1.14
.050	1.27
.060	1.52
.068	1.73
.070	1.78
.080	2.03
.095	2.41
.200	5.08
.270	6.86
.290	7.37
.300	7.62
.400	10.16
.490	12.45

FIGURE 1. Case outlines - Continued.

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Symbol	Limits	
	Inches	
	Min	Max
A	.100	.200
b	.014	.023
b1	.030	.060
C	.008	.015
D	1.050	1.260
E	.260	.310
E1	.280	.320
e	.100	BSC
L	.125	.200
L1	.150	
Q	.015	.060
S	.030	.065
S1	.005	
S2	.005	

Inches	mm
.005	0.13
.008	0.20
.014	0.36
.015	0.38
.023	0.58
.030	0.76
.060	1.52
.065	1.65
.100	2.54
.125	3.18
.150	3.81
.200	5.08
.260	6.60
.290	7.37
.310	7.87
.320	8.13
1.050	26.67
1.260	32.00

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

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DEFENSE ELECTRONICS SUPPLY CENTER  
DAYTON, OHIO 45444

SIZE  
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Terminal symbol						
Device	01-10		11-18		19-24	
Case	L	X	<u>1/</u> L, K	<u>2/</u> X, U	<u>3/</u> W, Y, Z	K
Terminal number						
1	A <sub>0</sub>	NC	A <sub>0</sub>	NC	A <sub>5</sub>	A <sub>0</sub>
2	A <sub>1</sub>	NC	A <sub>1</sub>	NC	A <sub>6</sub>	A <sub>1</sub>
3	A <sub>2</sub>	A <sub>0</sub>	A <sub>2</sub>	A <sub>0</sub>	A <sub>7</sub>	A <sub>2</sub>
4	A <sub>3</sub>	A <sub>1</sub>	A <sub>3</sub>	A <sub>1</sub>	A <sub>8</sub>	A <sub>3</sub>
5	A <sub>4</sub>	A <sub>2</sub>	A <sub>4</sub>	A <sub>2</sub>	A <sub>9</sub>	A <sub>4</sub>
6	A <sub>5</sub>	A <sub>3</sub>	A <sub>5</sub>	A <sub>3</sub>	A <sub>10</sub>	A <sub>5</sub>
7	A <sub>6</sub>	A <sub>4</sub>	A <sub>6</sub>	A <sub>4</sub>	A <sub>11</sub>	A <sub>6</sub>
8	A <sub>7</sub>	A <sub>5</sub>	A <sub>7</sub>	A <sub>5</sub>	A <sub>12</sub>	A <sub>7</sub>
9	A <sub>8</sub>	A <sub>6</sub>	A <sub>8</sub>	A <sub>6</sub>	A <sub>13</sub>	A <sub>8</sub>
10	$\overline{CE}_1$	A <sub>7</sub>	$\overline{CE}$	A <sub>7</sub>	$\overline{CE}$	$\overline{CE}$
11	$\overline{OE}$	A <sub>8</sub>	$\overline{OE}$	A <sub>8</sub>	GND	NC
12	GND	$\overline{CE}_1$	GND	$\overline{CE}$	$\overline{WE}$	GND
13	$\overline{WE}$	$\overline{OE}$	$\overline{WE}$	$\overline{OE}$	I/O <sub>0</sub>	$\overline{WE}$
14	I/O <sub>1</sub>	GND	I/O <sub>1</sub>	GND	I/O <sub>1</sub>	I/O <sub>1</sub>
15	I/O <sub>2</sub>	$\overline{CE}_2$	I/O <sub>2</sub>	NC	I/O <sub>2</sub>	I/O <sub>2</sub>
16	I/O <sub>3</sub>	$\overline{WE}$	I/O <sub>3</sub>	$\overline{WE}$	I/O <sub>3</sub>	I/O <sub>3</sub>
17	I/O <sub>4</sub>	I/O <sub>1</sub>	I/O <sub>4</sub>	I/O <sub>1</sub>	A <sub>0</sub>	I/O <sub>4</sub>
18	$\overline{CE}_2$	I/O <sub>2</sub>	NC	I/O <sub>2</sub>	A <sub>1</sub>	NC
19	A <sub>9</sub>	I/O <sub>3</sub>	A <sub>9</sub>	I/O <sub>3</sub>	A <sub>2</sub>	A <sub>9</sub>
20	A <sub>10</sub>	I/O <sub>4</sub>	A <sub>10</sub>	I/O <sub>4</sub>	A <sub>3</sub>	A <sub>10</sub>
21	A <sub>11</sub>	A <sub>9</sub>	A <sub>11</sub>	A <sub>9</sub>	A <sub>4</sub>	A <sub>11</sub>
22	A <sub>12</sub>	A <sub>10</sub>	A <sub>12</sub>	A <sub>10</sub>	V <sub>CC</sub>	A <sub>12</sub>
23	A <sub>13</sub>	A <sub>11</sub>	A <sub>13</sub>	A <sub>11</sub>	--	A <sub>13</sub>
24	V <sub>CC</sub>	A <sub>12</sub>	V <sub>CC</sub>	A <sub>12</sub>	--	V <sub>CC</sub>
25	--	A <sub>13</sub>	--	A <sub>13</sub>	--	--
26	--	NC	--	NC	--	--
27	--	NC	--	NC	--	--
28	--	V <sub>CC</sub>	--	V <sub>CC</sub>	--	--

NC = No connection

1/ K does not apply to devices 11-14.

2/ U does not apply to devices 11-14.

3/ Y does not apply to devices 19 and 20.

FIGURE 2. Terminal connections.

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Device types 01 through 10

Mode	CE1	CE2	WE	OE	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D <sub>OUT</sub>	Active
Write	L	L	L	X	D <sub>IN</sub>	Active
Read	L	L	H	H	High Z	Active

Device types 11 through 24

Mode	CE	WE	OE 1/	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	D <sub>OUT</sub>	Active
Write	L	L	X	D <sub>IN</sub>	Active
Read 1/	L	H	H	High Z	Active

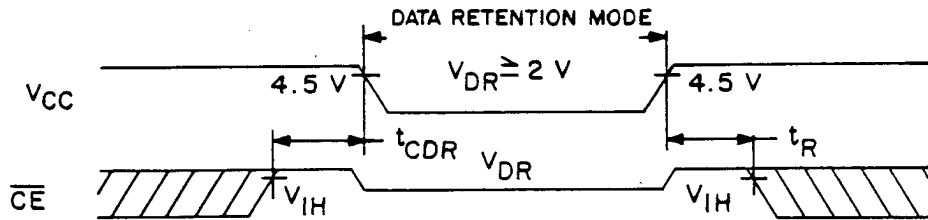
1/ Does not apply to devices 19 through 24.

FIGURE 3. Truth tables.

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LOW  $V_{CC}$  DATA RETENTION WAVEFORM

(Device types 02, 04, 06, 08 10, 11, 13, 15, 17, 19, 21, and 23)



NOTE:  $t_{CDR} = 0$  ns (minimum); may not be tested, but is guaranteed.  
 $t_r = t_{AVAX}$

TIMING WAVEFORM OF READ CYCLE NO. 1

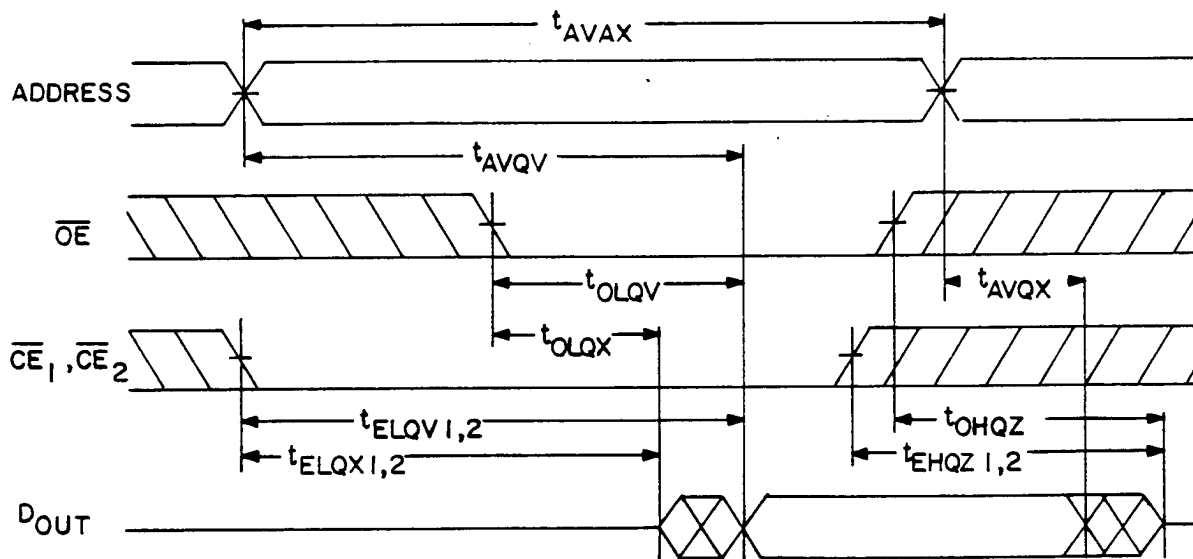


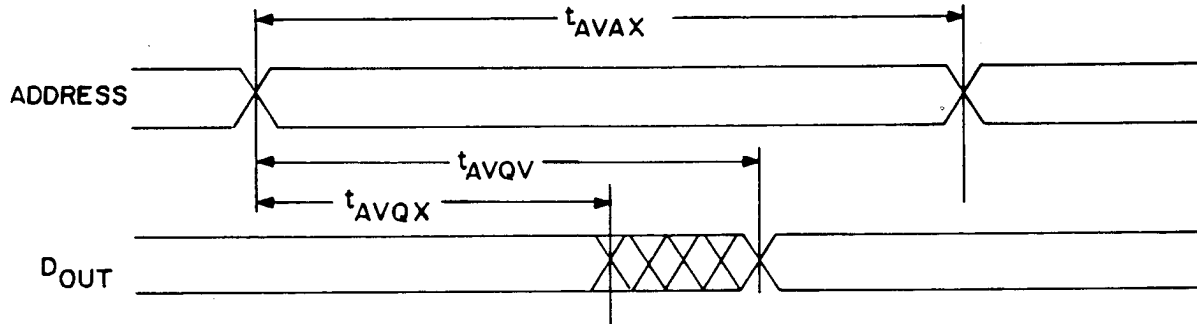
FIGURE 4. Switching time waveforms.

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TIMING WAVEFORM OF READ CYCLE NO. 2



TIMING WAVEFORM OF READ CYCLE NO. 3

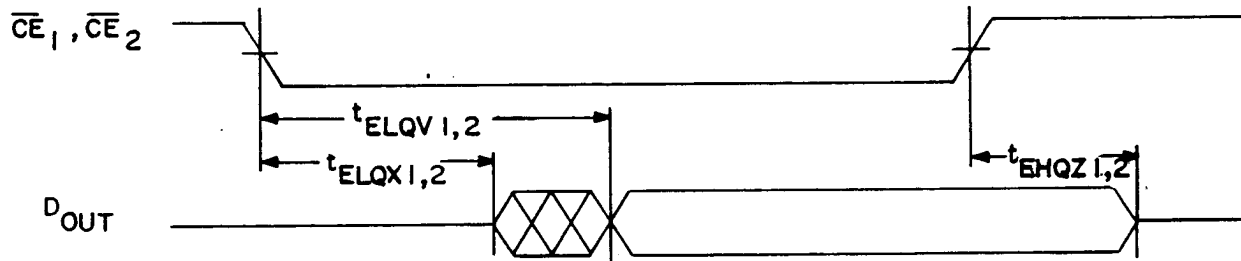


FIGURE 4. Switching time waveforms - Continued.

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TIMING WAVEFORM OF WRITE CYCLE NO. 1

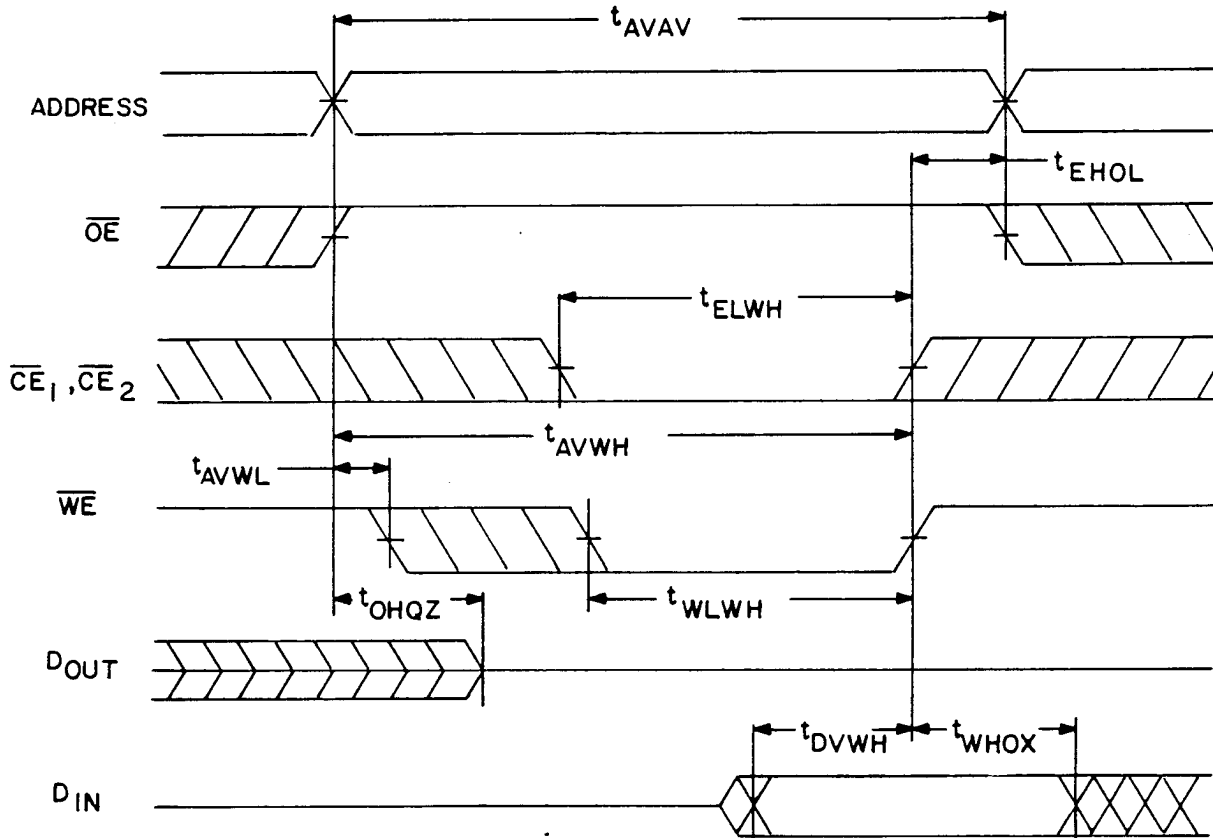


FIGURE 4. Switching time waveforms - Continued.

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TIMING WAVEFORM OF WRITE CYCLE NO. 2

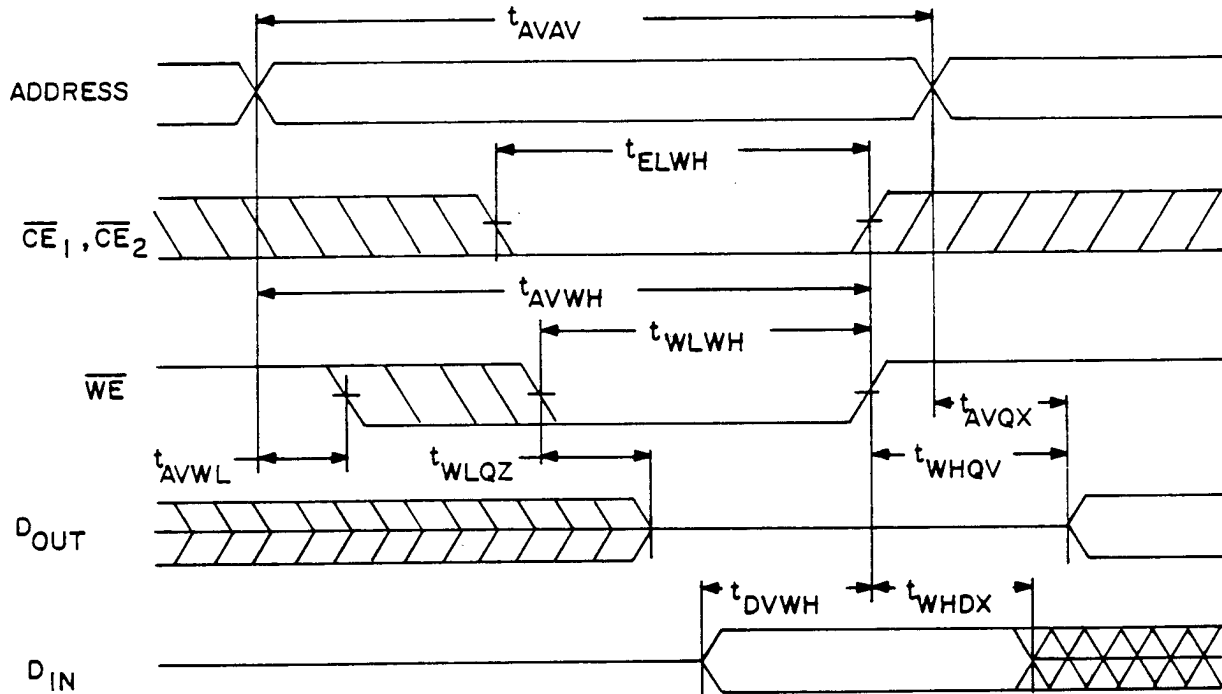
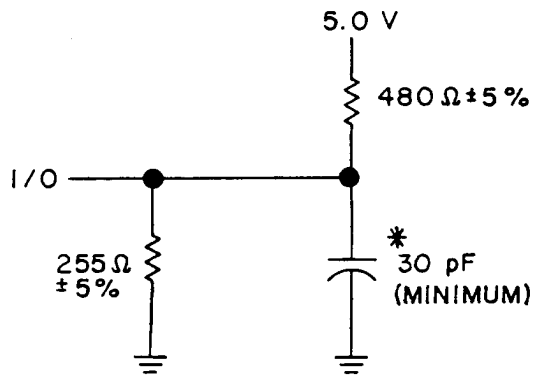


FIGURE 4. Switching time waveforms - Continued.

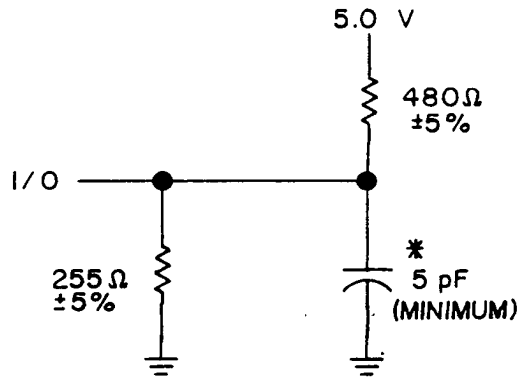
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Circuit A or equivalent



Circuit B or equivalent

for ( $t_{ELQX}$ ,  $t_{OLQX}$ ,  $t_{EHQZ}$ ,  $t_{OHQZ}$ ,  $t_{WLQZ}$ ,  $t_{WHQV}$ )

\*Including scope and jig

FIGURE 5. Output loads circuits.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, 8***,9,10,11
Groups C and D end-point electrical (method 5005)	2,3,7,8

- \* PDA applies to subgroup 1 and 7
- \*\* See 4.3.1c.
- \*\*\* See 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1</u> /	Replacement military specification part number
5962-8685901LX	61772	IDT7198S85CB	
5962-8685901XX	61772	IDT7198S85LB	
5962-8685902LX	61772	IDT7198L85CB	
5962-8685902XX	61772	IDT7198L85LB	
5962-8685903LX	61772	IDT7198S70CB	
5962-8685903XX	61772	IDT7198S70LB	
5962-8685904LX	61772	IDT7198L70CB	
5962-8685904XX	61772	IDT7198L70LB	
5962-8685905LX	61772	IDT7198S55CB	
5962-8685905XX	61772	IDT7198S55LB	
5962-8685906LX	61772	IDT7198L55CB	
5962-8685906XX	61772	IDT7198L55LB	
5962-8685907LX	61772	IDT7198S45CB	
5962-8685907XX	61772	IDT7198S45LB	
5962-8685908LX	61772	IDT7198L45CB	
5962-8685908XX	61772	IDT7198L45LB	
5962-8685909LX	61772	IDT7198S35CB	
5962-8685909XX	61772	IDT7198S35LB	
5962-8685910LX	61772	IDT7198L35CB	
5962-8685910XX	61772	IDT7198L35LB	
5962-8685911LX	60911 07263 61772	IMS1624S-70LM F1625DMQB70 IDT6198L70CB	
5962-8685911XX	60911 07263 61772	IMS1624W-70LM F1625LMQB70 IDT6198L70LB	

See footnotes at end of table.

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Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
5962-8685912LX	60911 07263 61772	IMS1624S-70M F1624DMQB70 IDT6198S70CB	
5962-8685912XX	60911 07263 61772	IMS1624W-70M F1624LMQB70 IDT6198S70LB	
5962-8685913LX	60911 07263 61772	IMS1624S-55LM F1625DMQB55 IDT6198L55CB	
5962-8685913XX	60911 07263 61772	IMS1624W-55LM F1625LMQB55 IDT6198L55LB	
5962-8685914LX	60911 61772 07263	IMS1624S-55M IDT6198S55CB F1624DMQB55	
5962-8685914XX	60911 61772 07263	IMS1624W-55M IDT6198S55LB F1624LMQB55	
5962-8685915LX	60911 07263 65786 61772	IMS1624S-45LM F1625DMQB45 CY7C166L-45DMB IDT6198L45CB	
5962-8685915XX	60911 07263 65786 61772	IMS1624W-45LM F1625LMQB45 CY7C166L-45LMB IDT6198L45LB	
5962-8685915UX	65786	CY7C166L-45LMB	
5962-8685915KX	65786	CY7C166L-45KMB	
5962-8685916LX	60911 07263 65786 61772	IMS1624S-45M F1624DMQB45 CY7C166-45DMB IDT6198S45CB	
5962-8685916XX	60911 07263 65786 61772	IMS1624W-45M F1624LMQB45 CY7C166-45LMB IDT6198S45LB	
5962-8685916UX	65786	CY7C166-45LMB	

See footnotes at end of table.

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Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
5962-8685916KX	65786	CY7C166-45KMB	
5962-8685917LX	07263 65786 61772	F1625DMQB35 CY7C166L-35DMB IDT6198L35CB	
5962-8685917XX	07263 65786 61772	F1625LMQB35 CY7C166L-35LMB IDT6198L35LB	
5962-8685917UX	65786	CY7C166L-35LMB	
5962-8685917KX	65786	CY7C166L-35KMB	
5962-8685918LX	07263 65786 61772	F1624DMQB35 CY7C166-35DMB IDT6198S35CB	
5962-8685918XX	07263 65786 61772	F1624LMQB35 CY7C166-35LMB IDT6198S35LB	
5962-8685918UX	65786	CY7C166-35LMB	
5962-8685918KX	65786	CY7C166-35KMB	
5962-8685919WX	07263	F1621DMQB55	
5962-8685919ZX	07263	F1621LMQB55	
5962-8685919TX	61772	IDT7188L55CB	
5962-8685919KX	61772	IDT7188L55FB	
5962-8685920WX	07263	F1620DMQB55	
5962-8685920ZX	07263	F1620LMQB55	
5962-8685920TX	61772	IDT7188S55CB	
5962-8685920KX	61772	IDT7188S55FB	
5962-8685921WX	07263	F1621DMQB45	
5962-8685921ZX	07263 65786	F1621LMQB45 CY7C164L-45LMB	
5962-8685921YX	65786	CY7C164L-45DMB	
5962-8685921KX	65786 61772	CY7C164L-45KMB IDT7188L45FB	

See footnotes at end of table.

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5962-8685921TX	61772	IDT7188L45CB	
5962-8685922WX	07263	F1620DMQB45	
5962-8685922ZX	07263 65786	F1620LMQB45 CY7C164-45LMB	
5962-8685922YX	65786	CY7C164-45DMB	
5962-8685922KX	65786 61772	CY7C164-45KMB IDT7188S45FB	
5962-8685922TX	61772	IDT7188S45CB	
5962-8685923WX	07263	F1621DMQB35	
5962-8685923ZX	07263 65786	F1621LMQB35 CY7C164L-35LMB	
5962-8685923YX	65786	CY7C164L-35DMB	
5962-8685923KX	65786 61772	CY7C164L-35KMB IDT7188L35FB	
5962-8685923TX	61772	IDT7188L35CB	
5962-8685924WX	07263	F1620DMQB35	
5962-8685924ZX	07263 65786	F1620LMQB35 CY7C164-35LMB	
5962-8685924YX	65786	CY7C164-35DMB	
5962-8685924KX	65786 61772	CY7C164-35KMB IDT7188S35FB	
5962-8685924TX	61772	IDT7188S35CB	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

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Vendor CAGE  
number

Vendor name  
and address

07263

Fairchild Semiconductor  
1111 39th Ave. S.E.  
Puyallup, WA 98373

60911

INMOS Corporation  
1110 Bayfield Drive  
Colorado Springs, CO 80906

61772

Integrated Device Technology, Inc.  
3236 Scott Blvd.  
Santa Clara, CA 95054

65786

Cypress Semiconductor  
3901 N. First Street  
San Jose, CA 95134

**STANDARDIZED  
MILITARY DRAWING**

**DEFENSE ELECTRONICS SUPPLY CENTER  
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**A**

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