Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

*Silicore** SLC1655 8-bit RISC Microcontroller/*VHDL*† Core

Product Overview

The *Silicore* SLC1655 is an 8-bit RISC microcontroller. It is delivered as a *VHDL* soft core module, and is intended for use in both FPGA and ASIC type devices. It is useful for microprocessor based embedded control applications such as: sensors, medical devices, consumer electronics, automotive systems, telecommunications, military, and industrial controls.

The core is especially useful wherever there is limited printed circuit board space. All microprocessor and application functions can be integrated onto a single FPGA or ASIC device, thereby creating a very compact design. For example, very small sensor circuits can be created with this core.

When implemented on an FPGA device, the *Silicore* SLC1655 offers a completely user-defined microcontroller. This eliminates expensive NRE charges and lengthy lead times which are common for semicustom integrated circuits. The end user can completely control the entire system integration process.

The core is also useful for high-volume applications. That's because it is unusually compact, and can be produced inexpensively in ASIC parts.

The *Silicore* SLC1655 can be used in a number of FPGA and ASIC target devices. This gives the user a wide range of options in mechanical packaging, temperature ranges, military specifications, and radiation hardening.

Numerous software tools are available for the *Silicore* SLC1655. The core is software compatible with the industry standard *PIC*‡ series of microcontrollers made by Microchip Technology Inc. (*Silicore* Corporation is not affiliated with Microchip Technology Inc.). There are many software tools available from third-party vendors. These include assemblers, C compilers, simulators, and fuzzy logic tools.

The core is delivered as a kit and includes complete documentation, *VHDL* source code, test benches, technical reference manual, generous license agreement, factory technical support, and an evaluation board. On-site training is also available at an extra charge.

The evaluation board demonstrates the capabilities of the microcontroller. It also includes an emulation ROM capability. This allows the user to assemble and download application software through a PC compatible parallel port cable. The (optional) *VHDL* parallel port interface entity is also included with the developer's kit.

Silicore SLC1655 Features

- 8-bit RISC microcontroller.
- Dual instruction and data buses with Harvard architecture.
- Fast operation: all microcontroller instructions (except branches) require one clock cycle. Branch instructions require two clock cycles.
- Very compact design minimizes gate count.
- 24 input and 48 output I/O lines.
- General purpose, 8-bit timer/counter module.
- Powerdown/sleep mode for low power applications.
- Instruction ROM§: 512 x 12 bit. Can be configured as embedded ROM, or as an emulation ROM for software development purposes.
- General purpose registers (RAM): 24 bytes.

* *Silicore* is a service mark and trademark of Silicore Corp.
† *VHDL* is a trademark of Cadence Design Systems, Inc.
‡ *PIC* is a registered trademark of Microchip Technology Inc.
§ Contact *Silicore* for versions with more RAM and ROM.

Silicore SLC1655 Features (continued)

- 32 op-code instructions with easy-to-use application software environment.
- A large base of software, tools, and reference books are available.
- Microcontroller design written in the flexible *VHDL* hardware description language. The *Silicore* SLC1655 is delivered as a soft core, meaning that all *VHDL* source code and test benches are supplied. This allows the user to tweak the design for a particular application. Complete documentation is also provided.
- Very portable design can be operated on a wide variety of FPGA and ASIC target devices.
- Straightforward synchronous design simplifies system integration.
- Very simple timing constraint definition.

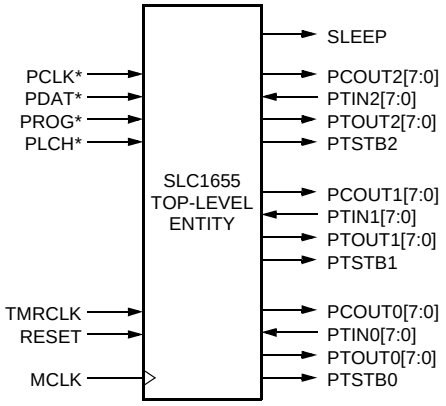
The maximum operating speed is a function of the target device technology[1].

External Architecture

The core has a classic microcontroller topology. Connections are quite simple and include clock, reset, timer/counter input, sleep pin, and I/O ports. An optional emulation ROM capability can also be used. This allows instructions to be downloaded through a PC compatible parallel port.

All I/O is handled through 24 input lines and 48 output lines. These can be used independently, or can be configured as three bidirectional ports (buses). Each port has an output strobe for connection to external FIFO buffers.

1. Operating speeds on typical FPGA parts are about 5 MIPS—10 MIPS.



0386 (F)

* EMR: Optional emulation ROM.

Figure 1. *VHDL* Top Level Entity Description

Table 1. Signal Descriptions

Signal Name	I/O Type	Signal Description
MCLK	I	Microcontroller lock
PCLK*	I	Program clock (EMR)
PCOUT0-2[7:0]	O	Port control output
PDAT*	I	Program data (EMR)
PLCH*	I	Program latch (EMR)
PROG*	I	Program enable (EMR)
PTINO-2[7:0]	I	I/O port input
PTOUT0-2[7:0]	O	I/O port output
PTSTB0-2	O	Port output strobe
RESET	I	Reset (external)
SLEEP	O	Powerdown/sleep mode
TMRCLK	I	External timer/counter clock

* EMR: Optional emulation ROM.

Silicore SLC1655 Features (continued)

Internal Architecture

The *Silicore* SLC1655 uses a classic Harvard architecture. This means that it has dual instruction and data buses, and an unencoded instruction stream. This creates both a fast processor, and a very simple design topology. Furthermore, the design is completely synchronous. All operations occur at the rising edge of MCLK. This makes the design portable across many FPGA and ASIC target devices.

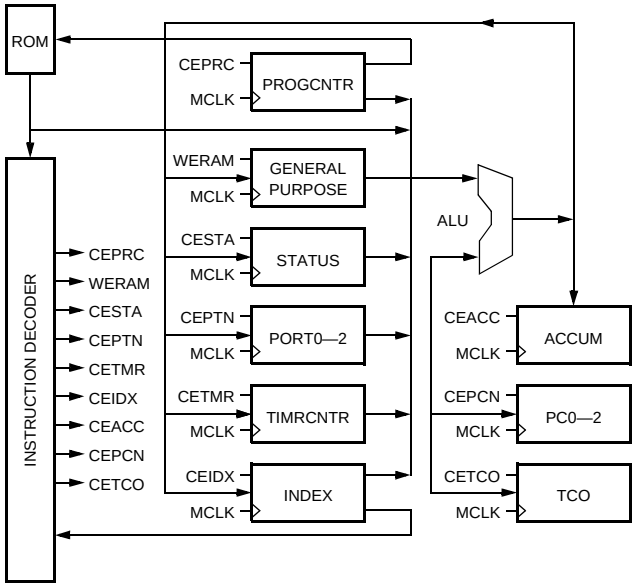


Figure 2. Internal Architecture

Table 2. Internal Register Set

Register	Address	R/W Address
ACCUM	Implicit	R/W
PC0	Implicit	W
PC1	Implicit	W
PC2	Implicit	W
TCO	Implicit	W
STACK1	Implicit	R/W
STACK2	Implicit	R/W
INDIRECT	0 x 00	R/W
TIMRCNTR	0 x 00	R/W
PROGCNTR	0 x 00	R/W
STATUS	0 x 00	R/W
INDEX	0 x 00	R/W
PORT0	0 x 00	R/W
PORT1	0 x 00	R/W
PORT2	0 x 00	R/W
GEN PURPOSE	0 x 08–0 x 1F	R/W

Instruction Set

The core is controlled by a simple instruction set with a total of 32 op-codes. These include add, subtract, increment, decrement, logical, loop, and branch instructions. A branch-to-subroutine and a small (two level) stack is also included.

VHDL Synthesis & Tools

The *Silicore* SLC1655 is delivered as *VHDL* source code. The core must be synthesized by the user before operation on a particular target device (such as an FPGA or ASIC). Most of the internal entities are provided with the source code. However, there are a few exceptions. RAM, ROM, and I/O drivers must be synthesized with entities provided by the FPGA or ASIC vendor. That's because portable, sythesizable RAM and ROM elements are not supported by the *VHDL* standards. Examples of complete design solutions are provided in the technical reference manual.

The *Silicore* SLC1655 is provided as a soft core. This means that all *VHDL* source code and test benches are provided with the design.

Silicore SLC1655 Features (continued)

It is assumed by *Silicore* Corporation that all simulation and synthesis tools conform to the following standards: *IEEE** STD 1076-1993, *IEEE* STD 1073.3-1997, and *IEEE* STD 1164-1993.

Almost any synthesis tool that supports common *VHDL* structures can be used. The original core was created with Peak*VHDL* and PeakFPGA from Accolade Design Automation.

Evaluation Board

An evaluation board for the *Silicore* SLC1655 is available. This allows the user to demonstrate and evaluate the microcontroller. Functions included with the evaluation board include:

- Lucent *ORCA*® OR2CA15A-4 FPGA
- Programmed demonstration ROM
- Programmed emulation ROM
- PC download cable (for emulation ROM)
- PC download software (for emulation ROM)
- 5 MHz/5 MIPS crystal clock oscillator
- 9 Vdc power supply
- 16 x 1 LCD module
- 4 keyswitches
- 500 Hz free running oscillator
- Complete instructions and technical reference manual

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 3. Instruction Set Summary

Mnemonic	Operand	Description
ADD	R, D	ADD register and ACCUM
AND	R, D	AND register with ACCUM
ANDI	V	AND immediate with ACCUM
BCLR	R, B	Clear request bit
BRA	V	Branch
BSET	R, B	Set register bit
BSR	V	Branch to subroutine
BTSC	R, B	Test bit and skip if clear
BTSS	R, B	Test bit and skip if set
CLR	R, D	Clear register or ACCUM
DEC	R, D	Decrement register
DECSZ	R, D	Decrement register, skip if zero
INC	R, D	Increment register
INCSZ	R, D	Increment register, skip if zero
MOV	R, D	Move register
MOVA	R	Move ACCUM to register
MOVI	V	Move immediate to ACCUM
MOVP	—	Move ACCUM to PCO-2
MOVT	—	Move ACCUM to TCO
NOP	—	No operation
NOT	R, D	NOT register
OR	R, D	OR register with ACCUM
ORI	V	OR immediate with ACCUM
PWRDN	—	Powerdown
RET	V	Return from subroutine
ROL	R, D	Rotate register left
ROR	R, D	Rotate register right
RWT	—	Reset watchdog timer
SUB	R, D	Subtract ACCUM from register
SWPN	R, D	Swap nibbles with ACCUM
XOR	R, D	XOR register with ACCUM
XORI	V	XOR immediate with ACCUM

Evaluation Kit

The *Silicore* SLC1655 evaluation kit allows the user to test drive the microcontroller core. It includes the following items:

- Evaluation board with Lucent
- OR2CA15A-4 FPGA
- Two FPGA PROM samples including stand-alone ROM and emulation ROM configurations
- 12 foot PC compatible parallel port download cable
- Technical reference manual and complete documentation
- Assembler and simulator not included

Developer's Kit

The *Silicore* SLC1655 developer's kit allows the user to synthesize and reproduce the microcontroller core. It includes:

- Complete *VHDL* source code, including all test benches and test vectors
- Standard license agreement
- Evaluation board
- 16 hours factory technical support
- 1 year limited warranty (including software updates)

For additional information, contact your Microelectronics Group Account Manager or the following:
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