

MITSUBISHI MICROCOMPUTERS

M37702M2LXXXGP, M37702S1LGP M37702M2LXXXHP, M37702S1LHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37702M2LXXXGP is a single-chip 16-bit microcomputer designed with high-performance CMOS silicon gate technology. This is housed in a small 80-pin plastic molded QFP. This single-chip microcomputer has a large 16 M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for communication, office, business and industrial equipment controller that require high-speed processing of large data.

The strong points of the M37702M2LXXXGP, M37702S1LGP, M37702M2LXXXHP and M37702S1LHP are the low supply voltage and small package.

The differences between M37702M2LXXXGP, M37702S1LGP, M37702M2LXXXHP and M37702S1LHP are the ROM size and the package as shown below. Therefore, the following descriptions will be for the M37702M2LXXXGP unless otherwise noted.

Type name	ROM size	Package
M37702M2LXXXGP	16 K bytes	80-pin plastic molded QFP (80P6S-A)
M37702S1LGP	External	80-pin plastic molded QFP (80P6S-A)
M37702M2LXXXHP	16 K bytes	80-pin plastic molded fine-pitch QFP (80P6D-A)
M37702S1LHP	External	80-pin plastic molded fine-pitch QFP (80P6D-A)

FEATURES

- Number of basic instructions103
- Memory size ROM 16 K bytes
 RAM 512 bytes
- Instruction execution time
 The fastest instruction at 8 MHz frequency 500 ns
- Single low supply voltage 2.7 – 5.5 V
- Low power dissipation
 (At 3 V supply voltage, 8 MHz frequency) 12 mW (Typ.)
 (At 5 V supply voltage, 8 MHz frequency) 30 mW (Typ.)
- Wide operating temperature range –40 – 80°C
- Interrupts 19 types 7 levels
- Multiple function 16-bit timer 5 + 3
- UART (may also be synchronous) 2
- 8-bit A-D converter 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
 (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
- Small package
 M37702M2LXXXGP, M37702S1LGP
 80-pin QFP (0.65 mm lead pitch)
 M37702M2LXXXHP, M37702S1LHP
 80-pin fine-pitch QFP (0.5 mm lead pitch)

APPLICATION

Control devices for communication equipment such as cellular radio telephones, cordless telephones, and radio communications
Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers
Control devices for industrial equipments such as ME, NC, and measuring instruments

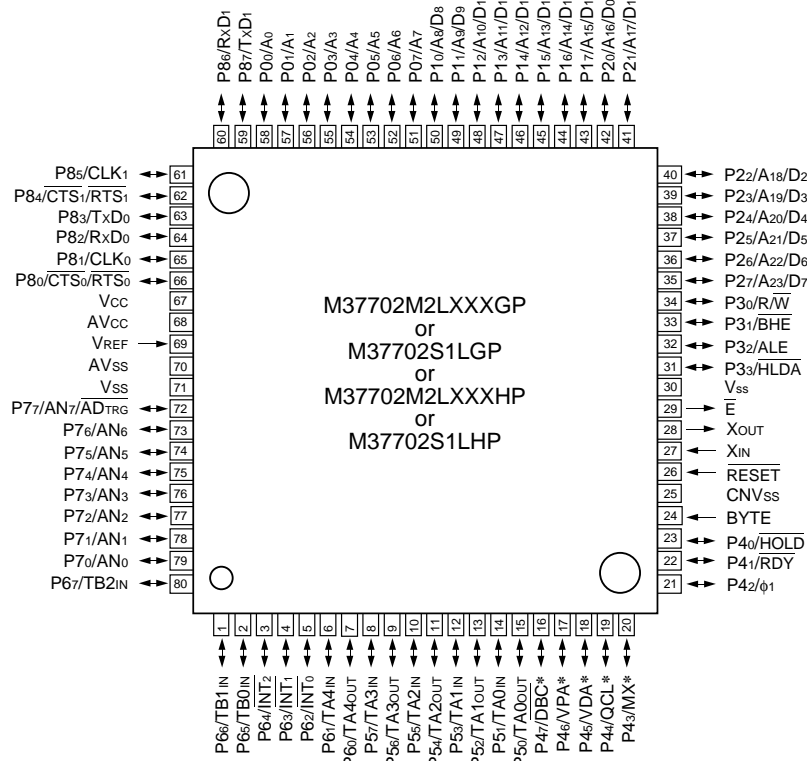
NOTE

Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

M37702M2LXXXGP, M37702S1LGP M37702M2LXXXHP, M37702S1LHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

PIN CONFIGURATION (TOP VIEW)



Outline

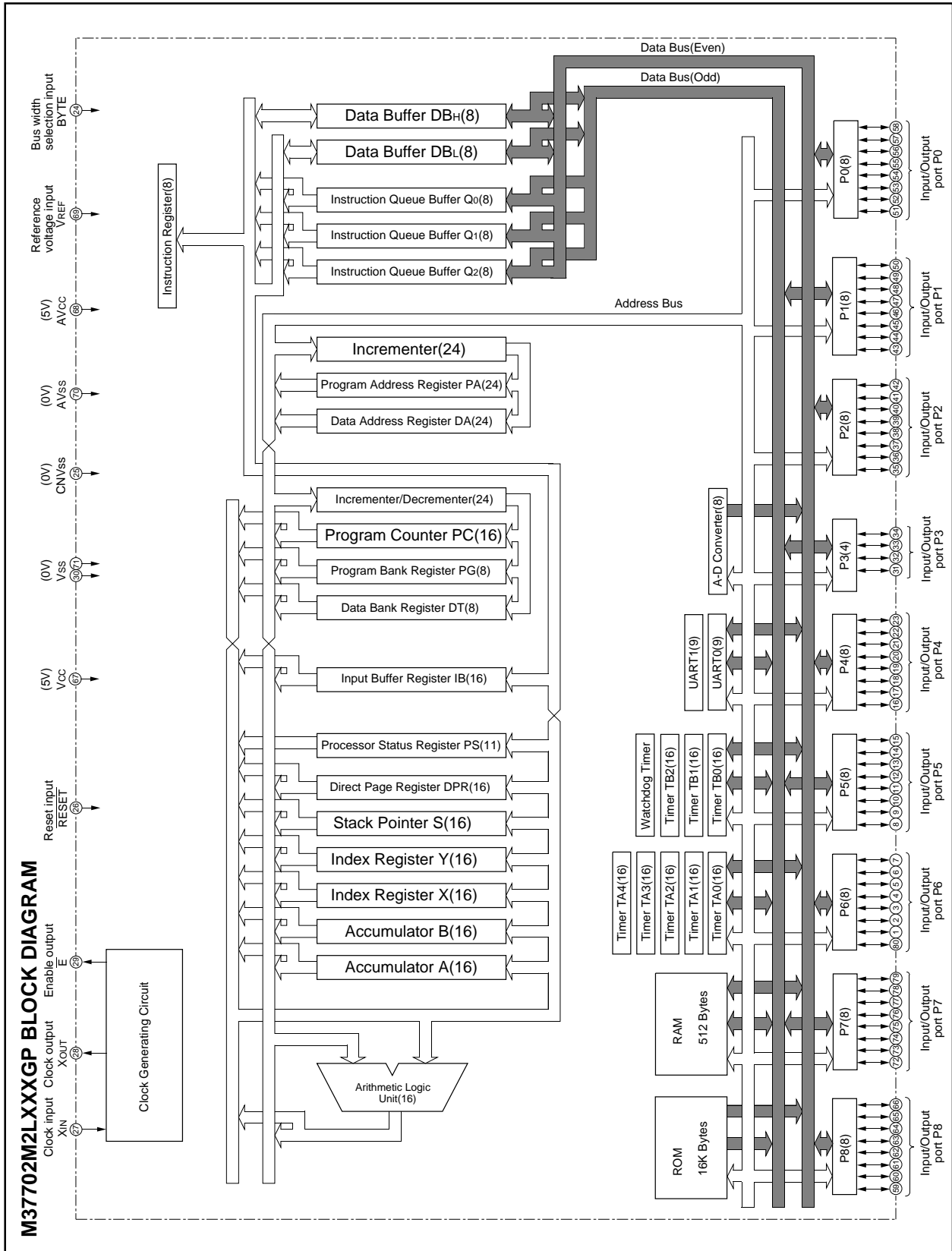
M37702M2LXXXGP, M37702S1LGP.....80P6S-A

M37702M2LXXXHP, M37702S1LHP.....80P6D-A

* : Used in the evaluation chip mode only

**M37702M2LXXXGP, M37702S1LGP
M37702M2LXXXHP, M37702S1LHP**

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



**M37702M2LXXXGP, M37702S1LGP
M37702M2LXXXHP, M37702S1LHP**

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37702M2LXXXGP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		500 ns (the fastest instruction at external clock 8 MHz frequency)
Memory size	ROM	16 K bytes
	RAM	512 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit X 8
	P3	4-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 2
A-D converter		8-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0 – 7.)
Clock generating circuit		Built-in (externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		2.7 – 5.5 V
Power dissipation		12 mW (at 3 V supply voltage, external clock 8 MHz frequency)
		30 mW (at 5 V supply voltage, external clock 8 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 M bytes
Operating temperature range		–40 – 85°C
Device structure		CMOS high-performance silicon gate process
Package	M37702M2LXXXGP, M37702S1LGP	80-pin plastic molded QFP (80P6S-A: 0.65 mm lead pitch)
	M37702M2LXXXHP, M37702S1LHP	80-pin plastic molded fine-pitch QFP (80P6D-A: 0.5 mm lead pitch)

M37702M2LXXXGP, M37702S1LGP M37702M2LXXXHP, M37702S1LHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power supply		Supply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for single-chip mode, and to Vcc for external ROM types.
RESET	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
XIN	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
\bar{E}	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AVCC, AVSS	Analog supply input		Power supply for the A-D converter. Connect AVcc to Vcc and AVss to Vss externally.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address (A7 – A0) is output in memory expansion mode or microprocessor mode.
P10 – P17	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D15 – D8) is input or output when \bar{E} output is "L" and an address (A15 – A8) is output when \bar{E} output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address (A15 – A8) is output.
P20 – P27	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data (D7 – D0) is input or output when \bar{E} output is "L" and an address (A23 – A16) is output when \bar{E} output is "H".
P30 – P33	I/O port P3	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/W, BHE, ALE and HLDA signals are output.
P40 – P47	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, P40 and P41 become HOLD and RDY input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port P42 can be programmed for ϕ_1 output pin divided the clock to XIN pin by 2. In microprocessor mode, P42 always has the function as ϕ_1 output pin.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3.
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input INT0, INT1 and INT2 pins, and input pins for timer B0, timer B1 and timer B2.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN0 – AN7 input pins. P77 also has an A-D conversion trigger input function.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as RXD, TXD, CLK, CTS/RTS pins for UART 0 and UART 1.

M37702M2LXXXGP, M37702S1LGP M37702M2LXXXHP, M37702S1LHP

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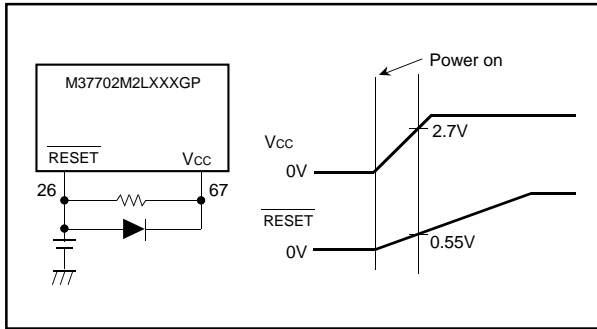


Fig. 2 Example of a reset circuit (perform careful evaluation at the system design level before using)

ADDRESSING MODES

The M37702M2LXXXGP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37702M2LXXXGP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

M37702M2LXXXGP;

- (1) M37702M2LXXXGP mask ROM order confirmation form
- (2) 80P6S mark specification form
- (3) ROM data (EPROM 3 sets)

M37702M2LXXXHP;

- (1) M37702M2LXXXHP mask ROM order confirmation form
- (2) 80P6D mark specification form
- (3) ROM data (EPROM 3 sets)

MEMORY

The memory map is shown in Figure 3.

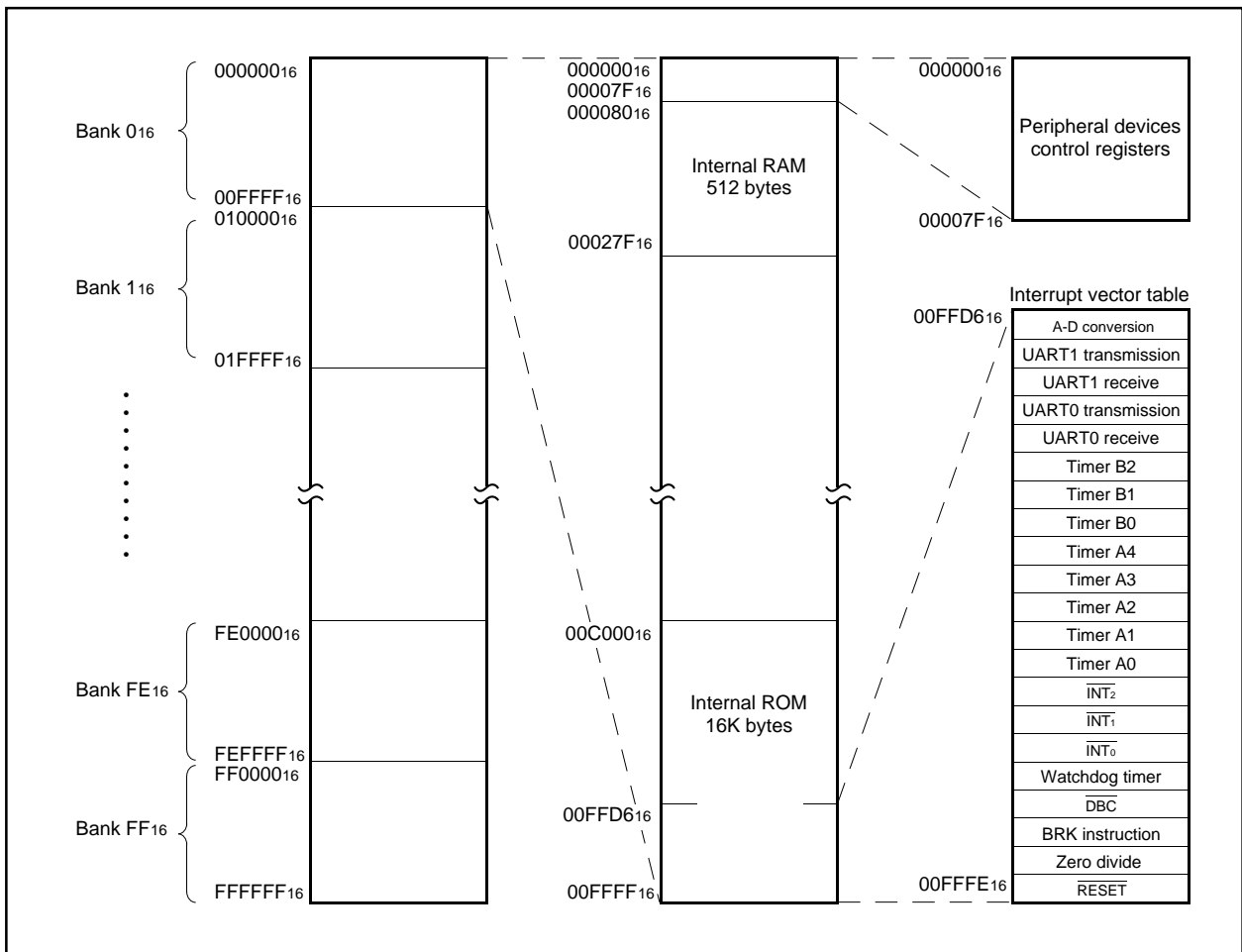


Fig. 3 Memory map

M37702M2LXXXGP, M37702S1LGP M37702M2LXXXHP, M37702S1LHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3 to 7	V
AV _{CC}	Analog supply voltage		-0.3 to 7	V
V _I	Input voltage	RESET, CNV _{SS} , BYTE	-0.3 to 12	V
V _I	Input voltage	P00-P07, P10-P17, P20-P27, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, V _{REF} , X _{IN}	-0.3 to V _{CC} +0.3	V
V _O	Output voltage	P00-P07, P10-P17, P20-P27, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, X _{OUT} , E	-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25 °C	300 (Note 1)	mW
T _{opr}	Operating temperature		-40 to 85	°C
T _{stg}	Storage temperature		-65 to 150	°C

Note 1. In the case of M37702M2LXXXHP and M37702S1LHP, the rating of power dissipation is 200 mW.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7 to 5.5 V, T_a = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage	2.7		5.5	V
AV _{CC}	Analog supply voltage		V _{CC}		V
V _{SS}	Supply voltage		0		V
AV _{SS}	Analog supply voltage		0		V
V _{IH}	High-level input voltage	P00-P07, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC}	V _{CC}	V
V _{IH}	High-level input voltage	P10-P17, P20-P27 (in single-chip mode)	0.8V _{CC}	V _{CC}	V
V _{IH}	High-level input voltage	P10-P17, P20-P27 (in memory expansion mode and micro-processor mode)	0.5V _{CC}	V _{CC}	V
V _{IL}	Low-level input voltage	P00-P07, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, X _{IN} , RESET, CNV _{SS} , BYTE	0	0.2V _{CC}	V
V _{IL}	Low-level input voltage	P10-P17, P20-P27 (in single-chip mode)	0	0.2V _{CC}	V
V _{IL}	Low-level input voltage	P10-P17, P20-P27 (in memory expansion mode and micro-processor mode)	0	0.16V _{CC}	V
I _{OH(peak)}	High-level peak output current	P00-P07, P10-P17, P20-P27, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87		-10	mA
I _{OH(avg)}	High-level average output current	P00-P07, P10-P17, P20-P27, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87		-5	mA
I _{OL(peak)}	Low-level peak output current	P00-P07, P10-P17, P20-P27, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87		10	mA
I _{OL(avg)}	Low-level average output current	P00-P07, P10-P17, P20-P27, P30-P33, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87		5	mA
f(X _{IN})	External clock frequency input			8	MHz

Note 2. Average output current is the average value of a 100 ms interval.

3. The sum of I_{OL(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, and P7 must be 80 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, and P7 must be 80 mA or less.

**M37702M2LXXXGP, M37702S1LGP
M37702M2LXXXHP, M37702S1LHP**

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$, $f(X_{IN}) = 8\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VOH	High-level output voltage P00–P07, P10–P17, P20–P27, P30, P31, P33, P40–P47, P50–P57, P60–P67, P70–P77, P80–P87	$V_{CC} = 5\text{ V}$, $I_{OH} = -10\text{ mA}$	3			V	
		$V_{CC} = 3\text{ V}$, $I_{OH} = -1\text{ mA}$	2.5				
VOH	High-level output voltage P00–P07, P10–P17, P20–P27, P30, P31, P33	$V_{CC} = 5\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	4.7			V	
VOH	High-level output voltage P32	$V_{CC} = 5\text{ V}$, $I_{OH} = -10\text{ mA}$	3.1			V	
		$V_{CC} = 5\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	4.8				
		$V_{CC} = 3\text{ V}$, $I_{OH} = -1\text{ mA}$	2.6				
VOH	High-level output voltage \bar{E}	$V_{CC} = 5\text{ V}$, $I_{OH} = -10\text{ mA}$	3.4			V	
		$V_{CC} = 5\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	4.8				
		$V_{CC} = 3\text{ V}$, $I_{OH} = -1\text{ mA}$	2.6				
VOL	Low-level output voltage P00–P07, P10–P17, P20–P27, P30, P31, P33, P40–P47, P50–P57, P60–P67, P70–P77, P80–P87	$V_{CC} = 5\text{ V}$, $I_{OL} = 10\text{ mA}$			2	V	
		$V_{CC} = 3\text{ V}$, $I_{OL} = 1\text{ mA}$			0.5		
VOL	Low-level output voltage P00–P07, P10–P17, P20–P27, P30, P31, P33	$V_{CC} = 5\text{ V}$, $I_{OL} = 2\text{ mA}$			0.45	V	
VOL	Low-level output voltage P32	$V_{CC} = 5\text{ V}$, $I_{OL} = 10\text{ mA}$			1.9	V	
		$V_{CC} = 5\text{ V}$, $I_{OL} = 2\text{ mA}$			0.43		
		$V_{CC} = 3\text{ V}$, $I_{OL} = 1\text{ mA}$			0.4		
VOL	Low-level output voltage \bar{E}	$V_{CC} = 5\text{ V}$, $I_{OL} = 10\text{ mA}$			1.6	V	
		$V_{CC} = 5\text{ V}$, $I_{OL} = 2\text{ mA}$			0.4		
		$V_{CC} = 3\text{ V}$, $I_{OL} = 1\text{ mA}$			0.4		
VT+ – VT–	Hysteresis $\overline{\text{HOLD}}$, $\overline{\text{RDY}}$, TA0IN–TA4IN , TB0IN–TB2IN , INT0–INT2 , ADTRG , CTS0 , CTS1 , CLK0 , CLK1	$V_{CC} = 5\text{ V}$	0.4		1	V	
		$V_{CC} = 3\text{ V}$	0.1		0.7		
VT+ – VT–	Hysteresis $\overline{\text{RESET}}$	$V_{CC} = 5\text{ V}$	0.2		0.5	V	
		$V_{CC} = 3\text{ V}$	0.1		0.4		
VT+ – VT–	Hysteresis X_{IN}	$V_{CC} = 5\text{ V}$	0.1		0.3	V	
		$V_{CC} = 3\text{ V}$	0.06		0.2		
IIH	High-level input current P00–P07, P10–P17, P20–P27, P30–P33, P40–P47, P50–P57, P60–P67, P70–P77, P80–P87, X_{IN} , $\overline{\text{RESET}}$, CNVss , BYTE	$V_{CC} = 5\text{ V}$, $V_I = 5\text{ V}$			5	μA	
		$V_{CC} = 3\text{ V}$, $V_I = 3\text{ V}$			4		
IIL	Low-level input current P00–P07, P10–P17, P20–P27, P30–P33, P40–P47, P50–P57, P60–P67, P70–P77, P80–P87, X_{IN} , $\overline{\text{RESET}}$, CNVss , BYTE	$V_{CC} = 5\text{ V}$, $V_I = 0\text{ V}$			–5	μA	
		$V_{CC} = 3\text{ V}$, $V_I = 0\text{ V}$			–4		
VRAM	RAM hold voltage	When clock is stopped.	2			V	
ICC	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.	$f(X_{IN}) = 8\text{ MHz}$, square waveform	$V_{CC} = 5\text{ V}$	6	12	mA
			$V_{CC} = 3\text{ V}$	4	8		
		$T_a = 25\text{ }^\circ\text{C}$ when clock is stopped.				1	μA
			$T_a = 85\text{ }^\circ\text{C}$ when clock is stopped.				

A-D CONVERTER CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$, $f(X_{IN}) = 8\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF} = V_{CC}$			± 3	LSB
RLADDER	Ladder resistance	$V_{REF} = V_{CC}$	2		10	$\text{k}\Omega$
tCONV	Conversion time		28.5			μs
VREF	Reference voltage		2.7		V_{CC}	V
VIA	Analog input voltage		0		V_{REF}	V

**M37702M2LXXXGP, M37702S1LGP
M37702M2LXXXHP, M37702S1LHP**

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TIMING REQUIREMENTS ($V_{CC} = 2.7$ to 5.5 V, $V_{SS} = 0$ V, $T_a = 25$ °C, $f(XIN) = 8$ MHz, unless otherwise noted)

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C	External clock input cycle time	125		ns
t _{W(H)}	External clock input high-level pulse width	50		ns
t _{W(L)}	External clock input low-level pulse width	50		ns
t _r	External clock rise time		20	ns
t _f	External clock fall time		20	ns

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{su(P0D-E)}	Port P0 input setup time	300		ns
t _{su(P1D-E)}	Port P1 input setup time	300		ns
t _{su(P2D-E)}	Port P2 input setup time	300		ns
t _{su(P3D-E)}	Port P3 input setup time	300		ns
t _{su(P4D-E)}	Port P4 input setup time	300		ns
t _{su(P5D-E)}	Port P5 input setup time	300		ns
t _{su(P6D-E)}	Port P6 input setup time	300		ns
t _{su(P7D-E)}	Port P7 input setup time	300		ns
t _{su(P8D-E)}	Port P8 input setup time	300		ns
t _{h(E-P0D)}	Port P0 input hold time	0		ns
t _{h(E-P1D)}	Port P1 input hold time	0		ns
t _{h(E-P2D)}	Port P2 input hold time	0		ns
t _{h(E-P3D)}	Port P3 input hold time	0		ns
t _{h(E-P4D)}	Port P4 input hold time	0		ns
t _{h(E-P5D)}	Port P5 input hold time	0		ns
t _{h(E-P6D)}	Port P6 input hold time	0		ns
t _{h(E-P7D)}	Port P7 input hold time	0		ns
t _{h(E-P8D)}	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{su(P1D-E)}	Port P1 input setup time	80		ns
t _{su(P2D-E)}	Port P2 input setup time	80		ns
t _{su(RDY-φ1)}	RDY input setup time	90		ns
t _{su(HOLD-φ1)}	HOLD input setup time	90		ns
t _{h(E-P1D)}	Port P1 input hold time	0		ns
t _{h(E-P2D)}	Port P2 input hold time	0		ns
t _{h(φ1-RDY)}	RDY input hold time	0		ns
t _{h(φ1-HOLD)}	HOLD input hold time	0		ns

M37702M2LXXXGP, M37702S1LGP M37702M2LXXXHP, M37702S1LHP

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Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (TA)	TAiIN input cycle time	250		ns
t _W (TAH)	TAiIN input high-level pulse width	125		ns
t _W (TAL)	TAiIN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (TA)	TAiIN input cycle time	1000		ns
t _W (TAH)	TAiIN input high-level pulse width	500		ns
t _W (TAL)	TAiIN input low-level pulse width	500		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (TA)	TAiIN input cycle time	500		ns
t _W (TAH)	TAiIN input high-level pulse width	250		ns
t _W (TAL)	TAiIN input low-level pulse width	250		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _W (TAH)	TAiIN input high-level pulse width	250		ns
t _W (TAL)	TAiIN input low-level pulse width	250		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (UP)	TAiOUT input cycle time	5000		ns
t _W (UPH)	TAiOUT input high-level pulse width	2500		ns
t _W (UPL)	TAiOUT input low-level pulse width	2500		ns
t _{SU} (UP-TiN)	TAiOUT input setup time	1000		ns
t _H (TiN-UP)	TAiOUT input hold time	1000		ns

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Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (TB)	TBiN input cycle time (one edge count)	250		ns
t _w (TBH)	TBiN input high-level pulse width (one edge count)	125		ns
t _w (TBL)	TBiN input low-level pulse width (one edge count)	125		ns
t _C (TB)	TBiN input cycle time (both edges count)	500		ns
t _w (TBH)	TBiN input high-level pulse width (both edges count)	250		ns
t _w (TBL)	TBiN input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (TB)	TBiN input cycle time	1000		ns
t _w (TBH)	TBiN input high-level pulse width	500		ns
t _w (TBL)	TBiN input low-level pulse width	500		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (TB)	TBiN input cycle time	1000		ns
t _w (TBH)	TBiN input high-level pulse width	500		ns
t _w (TBL)	TBiN input low-level pulse width	500		ns

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (AD)	$\overline{\text{ADTRG}}$ input cycle time (minimum allowable trigger)	2000		ns
t _w (ADL)	$\overline{\text{ADTRG}}$ input low-level pulse width	250		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _C (CK)	CLK _i input cycle time	500		ns
t _w (CKH)	CLK _i input high-level pulse width	250		ns
t _w (CKL)	CLK _i input low-level pulse width	250		ns
t _d (C-Q)	TxD _i output delay time		170	ns
t _h (C-Q)	TxD _i hold time	0		ns
t _{su} (D-C)	RxD _i input setup time	80		ns
t _h (C-D)	RxD _i input hold time	100		ns

External interrupt INT_i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _w (INH)	INT _i input high-level pulse width	250		ns
t _w (INL)	INT _i input low-level pulse width	250		ns

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SWITCHING CHARACTERISTICS ($V_{CC} = 2.7$ to 5.5 V, $V_{SS} = 0$ V, $T_a = 25$ °C, $f(XIN) = 8$ MHz, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(E-P0Q)	Port P0 data output delay time	Fig. 4		300	ns
td(E-P1Q)	Port P1 data output delay time			300	ns
td(E-P2Q)	Port P2 data output delay time			300	ns
td(E-P3Q)	Port P3 data output delay time			300	ns
td(E-P4Q)	Port P4 data output delay time			300	ns
td(E-P5Q)	Port P5 data output delay time			300	ns
td(E-P6Q)	Port P6 data output delay time			300	ns
td(E-P7Q)	Port P7 data output delay time			300	ns
td(E-P8Q)	Port P8 data output delay time			300	ns

Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits		Unit	
			Min.	Max.		
td(P0A-E)	Port P0 address output delay time	Fig. 4	50		ns	
td(E-P1Q)	Port P1 data output delay time (BYTE = "L")			130	ns	
tPXZ(E-P1Z)	Port P1 floating start delay time (BYTE = "L")			10	ns	
td(P1A-E)	Port P1 address output delay time			50	ns	
td(P1A-ALE)	Port P1 address output delay time			40	ns	
td(E-P2Q)	Port P2 data output delay time			130	ns	
tPXZ(E-P2Z)	Port P2 floating start delay time			10	ns	
td(P2A-E)	Port P2 address output delay time			50	ns	
td(P2A-ALE)	Port P2 address output delay time			40	ns	
td(ϕ 1-HLDA)	HLDA output delay time				120	ns
td(ALE-E)	ALE output delay time			4	ns	
tW(ALE)	ALE pulse width			60	ns	
td(BHE-E)	BHE output delay time			50	ns	
td(R/W-E)	R/W output delay time			50	ns	
td(E- ϕ 1)	ϕ 1 output delay time			0	40	ns
th(E-P0A)	Port P0 address hold time			50	ns	
th(ALE-P1A)	Port P1 address hold time (BYTE = "L")			9	ns	
th(E-P1Q)	Port P1 data hold time (BYTE = "L")			50	ns	
tPZX(E-P1Z)	Port P1 floating release delay time (BYTE = "L")			95	ns	
th(E-P1A)	Port P1 address hold time (BYTE = "H")			50	ns	
th(ALE-P2A)	Port P2 address hold time			9	ns	
th(E-P2Q)	Port P2 data hold time			50	ns	
tPZX(E-P2Z)	Port P2 floating release delay time			95	ns	
th(E-BHE)	BHE hold time			18	ns	
th(E-R/W)	R/W hold time			18	ns	
tW(EL)	E pulse width			460	ns	

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Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(P0A-E)	Port P0 address output delay time	Fig. 4	50		ns
td(E-P1Q)	Port P1 data output delay time (BYTE = "L")			130	ns
tPXZ(E-P1Z)	Port P1 floating start delay time (BYTE = "L")			10	ns
td(P1A-E)	Port P1 address output delay time		50		ns
td(P1A-ALE)	Port P1 address output delay time		40		ns
td(E-P2Q)	Port P2 data output delay time			130	ns
tPXZ(E-P2Z)	Port P2 floating start delay time			10	ns
td(P2A-E)	Port P2 address output delay time		50		ns
td(P2A-ALE)	Port P2 address output delay time		40		ns
td(ϕ 1-HLDA)	HLDA output delay time			120	ns
td(ALE-E)	ALE output delay time		4		ns
tW(ALE)	ALE pulse width		60		ns
td(BHE-E)	BHE output delay time		50		ns
td(R/W-E)	R/W output delay time		50		ns
td(E- ϕ 1)	ϕ 1 output delay time		0	40	ns
th(E-P0A)	Port P0 address hold time		50		ns
th(ALE-P1A)	Port P1 address hold time (BYTE = "L")		9		ns
th(E-P1Q)	Port P1 data hold time (BYTE = "L")		50		ns
tPZX(E-P1Z)	Port P1 floating release delay time (BYTE = "L")		95		ns
th(E-P1A)	Port P1 address hold time (BYTE = "H")		50		ns
th(ALE-P2A)	Port P2 address hold time		9		ns
th(E-P2Q)	Port P2 data hold time		50		ns
tPZX(E-P2Z)	Port P2 floating release delay time		95		ns
th(E-BHE)	BHE hold time		18		ns
th(E-R/W)	R/W hold time		18		ns
tW(EL)	\bar{E} pulse width		210		ns

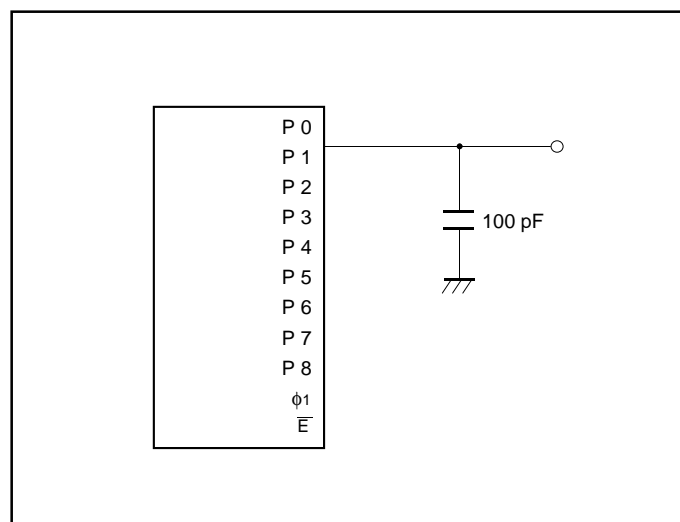


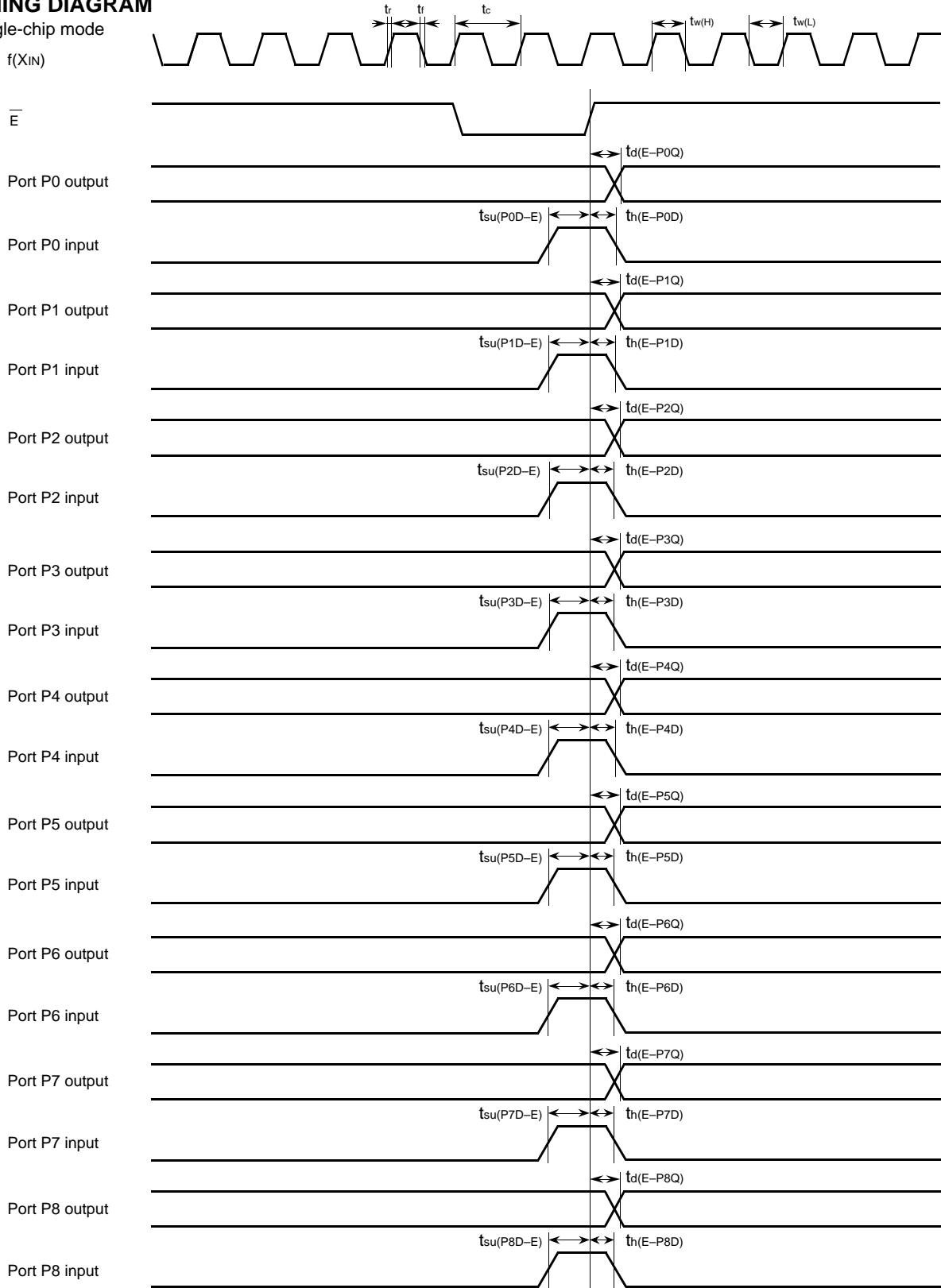
Fig. 4 Testing circuit for ports P0-P8, ϕ 1

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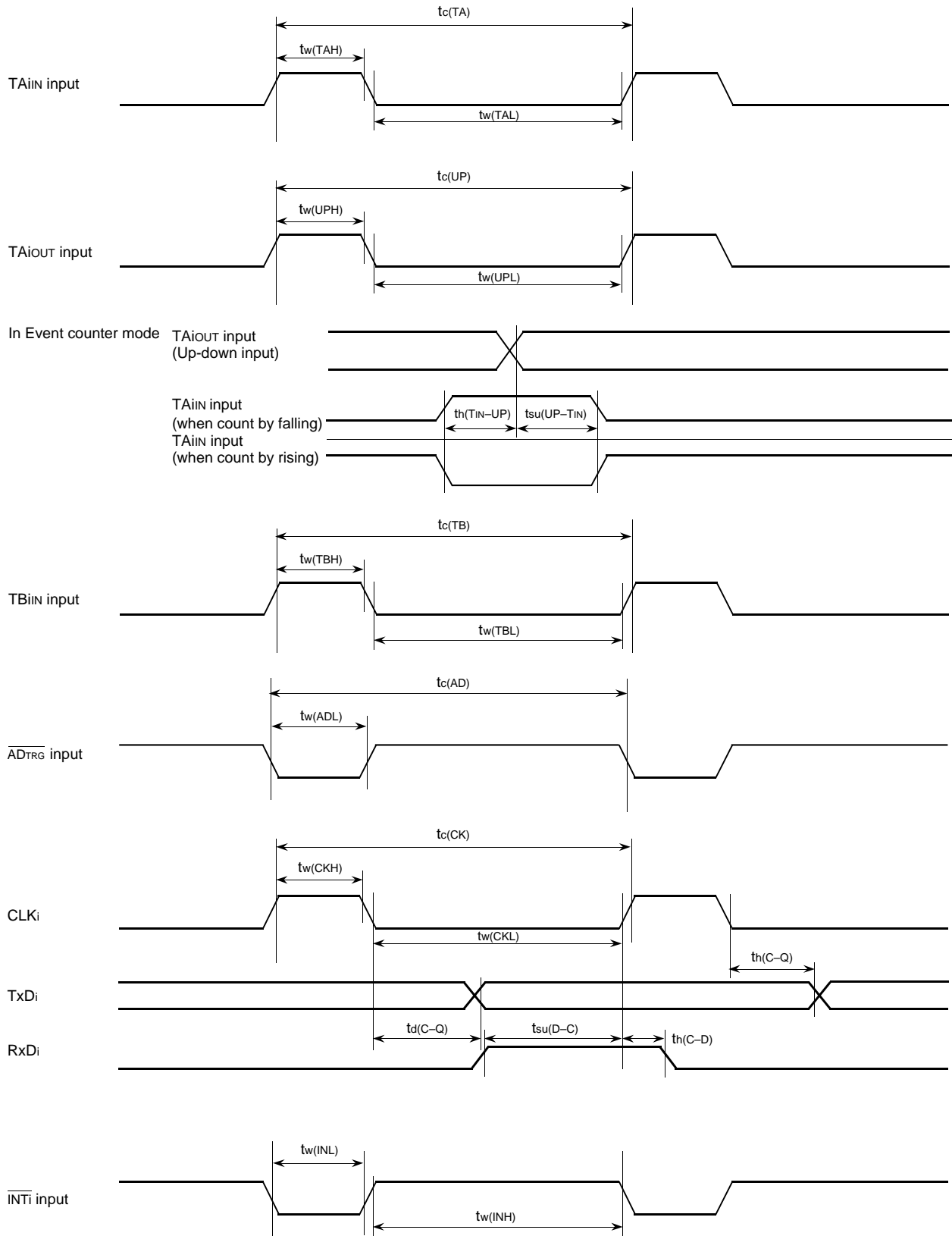
TIMING DIAGRAM

Single-chip mode



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M37702M2LXXXHP, M37702S1LHP

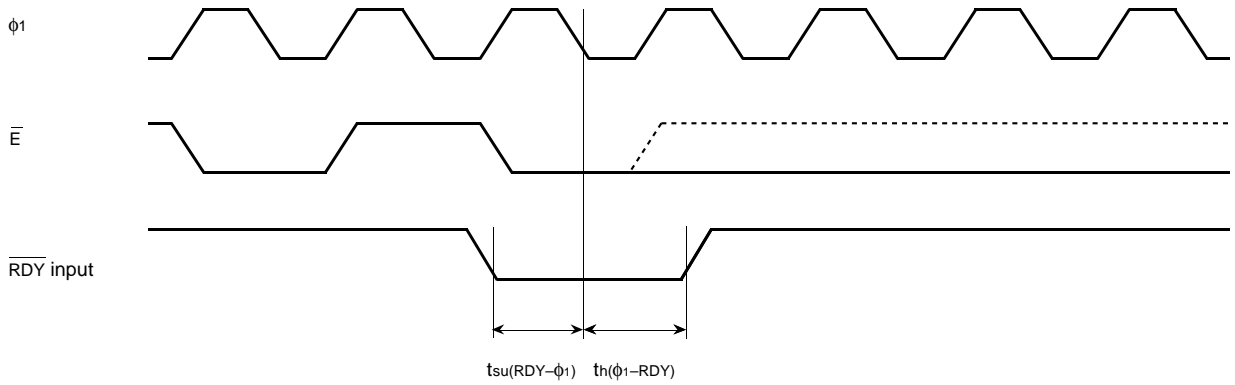
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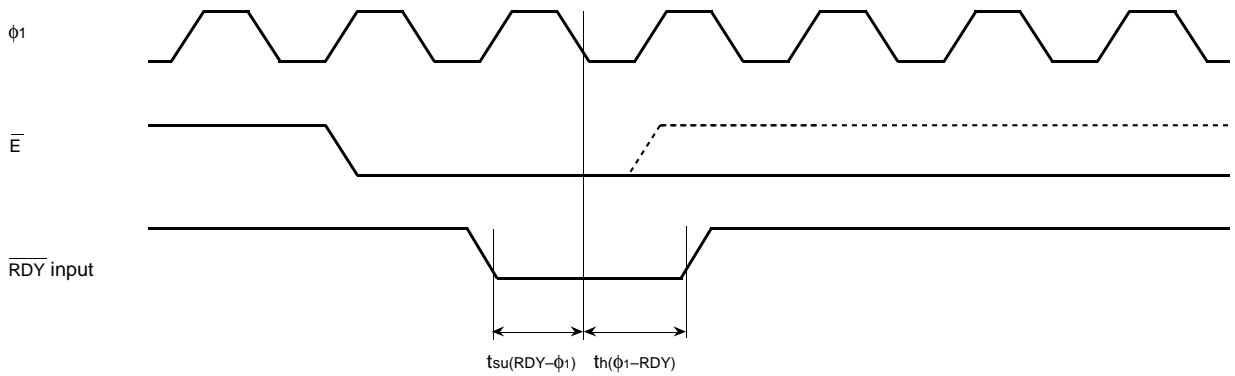
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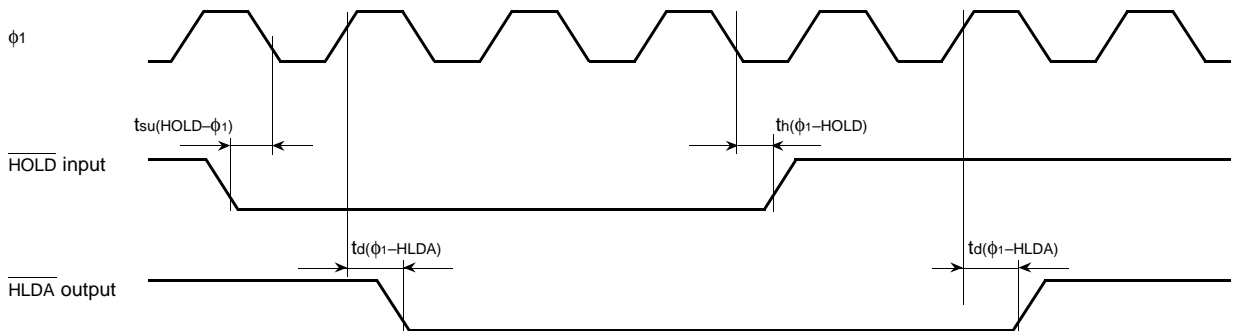
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



(When wait bit = "1" or "0" in common)



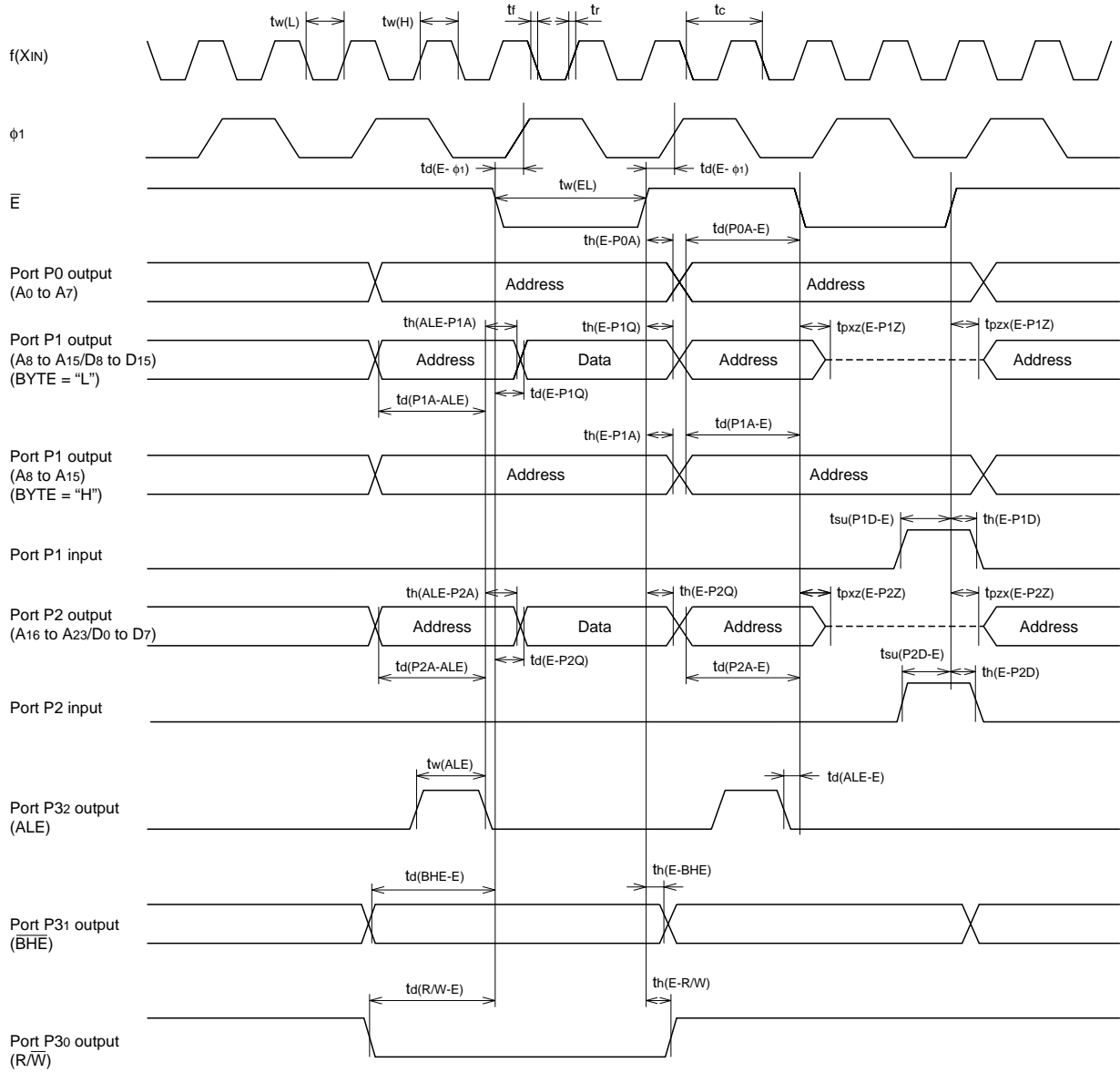
- Test conditions
- $V_{CC} = 2.7$ to 5.5 V
 - Input timing voltage : $V_{IL} = 0.2 V_{CC}$, $V_{IH} = 0.8 V_{CC}$
 - Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V

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SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

Memory expansion mode and microprocessor mode (When wait bit = "1")



Test conditions

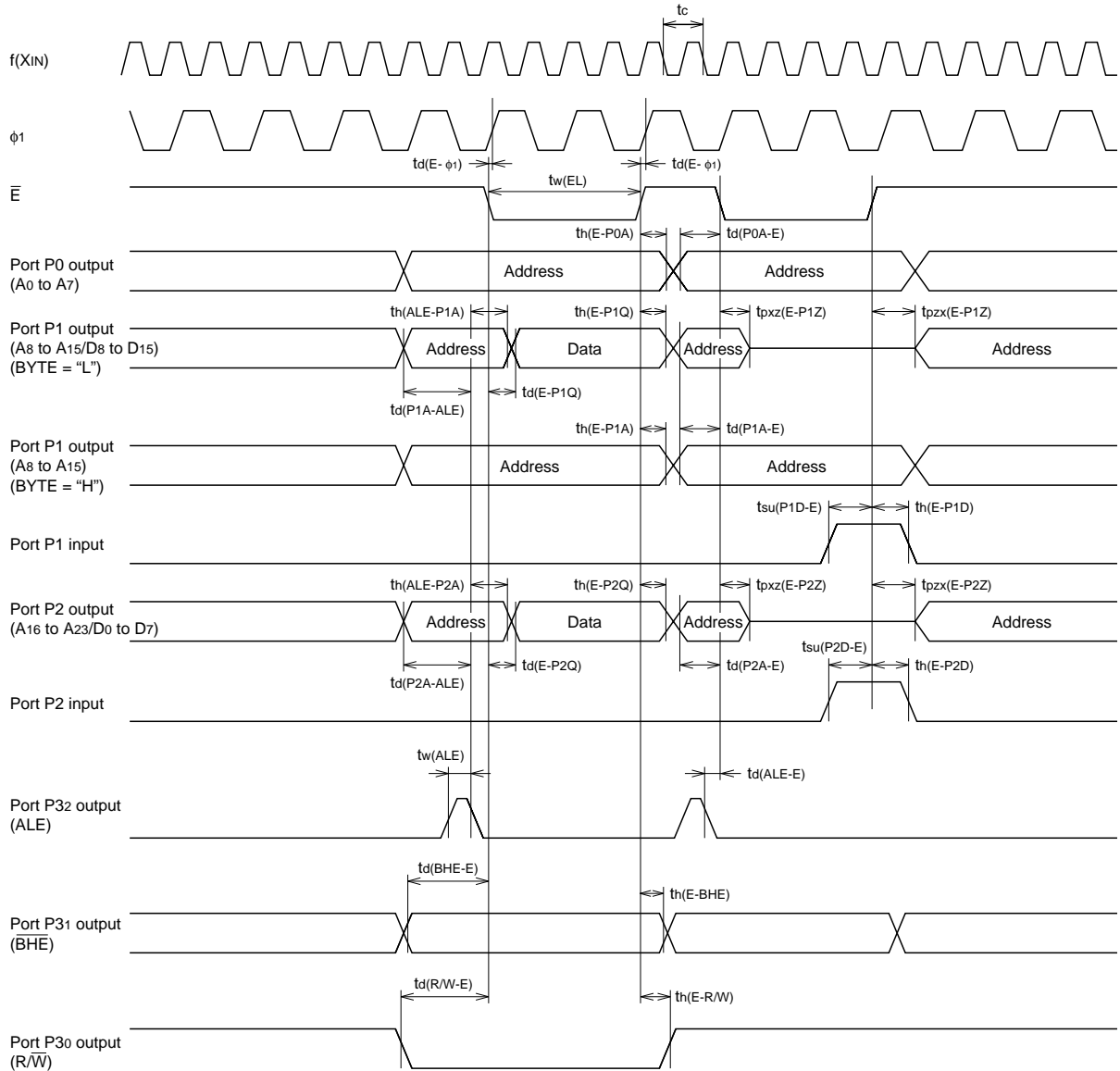
- $V_{CC} = 2.7$ to 5.5 V
- Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
- Ports P1, P2 input : $V_{IL} = 0.16 V_{CC}$, $V_{IH} = 0.5 V_{CC}$

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Memory expansion mode and microprocessor mode (When wait bit = "0", and external memory area is accessed)



Test conditions

- VCC = 2.7 to 5.5 V
- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Ports P1, P2 input : VIL = 0.16 Vcc, VIH = 0.5 Vcc

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