256MB- 32Mx64 SDRAM, UNBUFFERED

FEATURES

- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3 volt ± 0.3v Power Supply
- 144 Pin SO-DIMM JEDEC

DESCRIPTION

The WED3DG6433V is a 32Mx64 synchronous DRAM module which consists of four 32Mx16 SDRAM components in TSOP- 11 package, and one 2K EEPROM in an 8- pin TSSOP package for Serial Presence Detect which are mounted on a 144 Pin SO-DIMM multilayer FR4 Substrate.

* *This datasheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	2	VSS	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	VSS	56	VSS	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	VOLTAGE KEY				105	A8	106	BA0
13	DQ4	14	DQ36					107	VSS	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	VSS	22	VSS	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	$\overline{CS0}$	70	A12	119	VSS	120	VSS
27	VDD	28	VDD	71	*$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DNU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	VSS	76	VSS	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	VSS	36	VSS	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	VSS	140	VSS
47	DQ12	48	DQ44	91	VSS	92	VSS	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

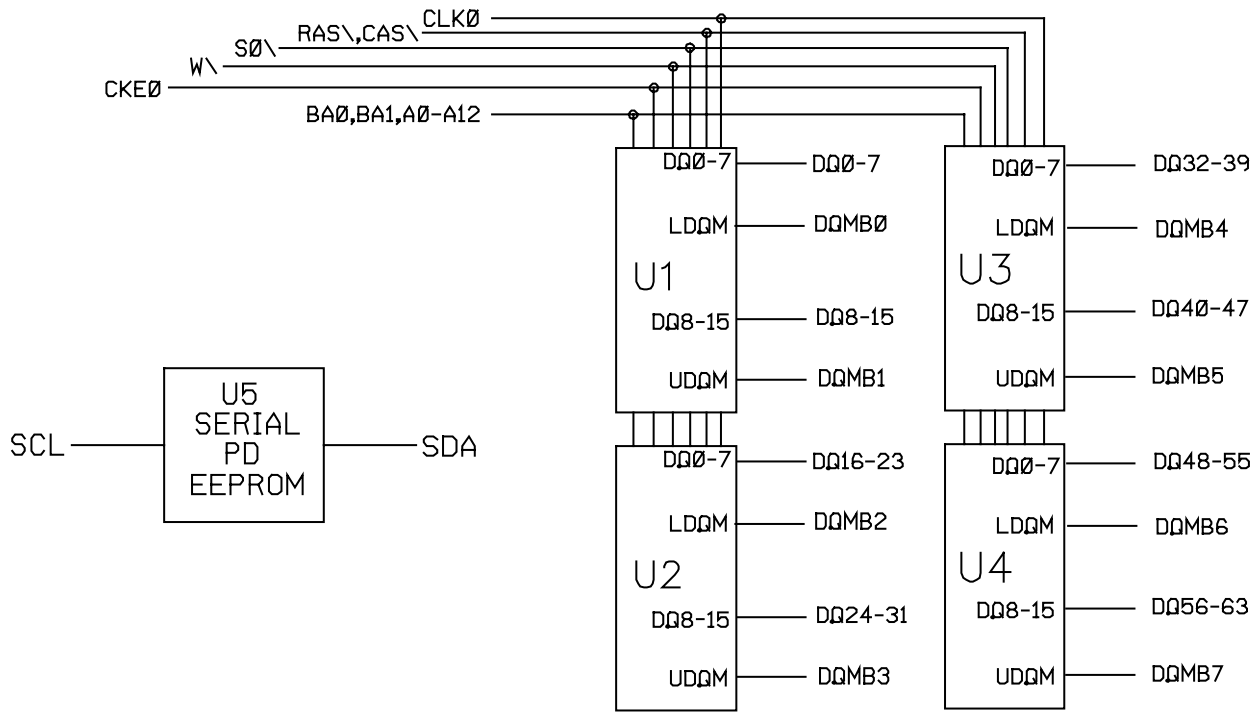
PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CLK0	Clock input
CKE0	Clock Enable input
$\overline{CS0}$	Chip select Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0-7	DQM
VDD	Power Supply (3.3V)
VSS	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

* These pins are not used in this module.

** These pins should be NC in the system which does not support SPD.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to VSS	V_{IN}, Vout	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Storage Temperature	TSTG	-55 ~ +150	°C
Power Dissipation	PD	4	W
Short Circuit Current	IOS	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage Referenced to: V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input High Voltage	VIH	2.0	3.0	VDDQ+0.3	V	1
Input Low Voltage	VIL	-0.3	—	0.8	V	2
Output High Voltage	VOH	2.4	—	—	V	IOH= -2mA
Output Low Voltage	VOL	—	—	0.4	V	IOL= -2mA
Input Leakage Current	ILI	-10	—	10	µA	3

Note: 1. VIH (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(T_A = 23°C, f = 1MHz, V_{DD} = 3.3V, VREF=1.4V ± 200mV)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12)	CIN1	-	45	pF
Input Capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN2	-	45	pF
Input Capacitance (CKE0)	CIN3	-	25	pF
Input Capacitance (CLK0)	CIN4	-	21	pF
Input Capacitance ($\overline{CS0}$)	CIN5	-	25	pF
Input Capacitance (DQM0-DQM7)	CIN6	-	12	pF
Input Capacitance (BA0-BA1)	CIN7	-	45	pF
Data input/output capacitance (DQ0-DQ63)	Cout	-	20	pF

OPERATING CURRENT CHARACTERISTICS

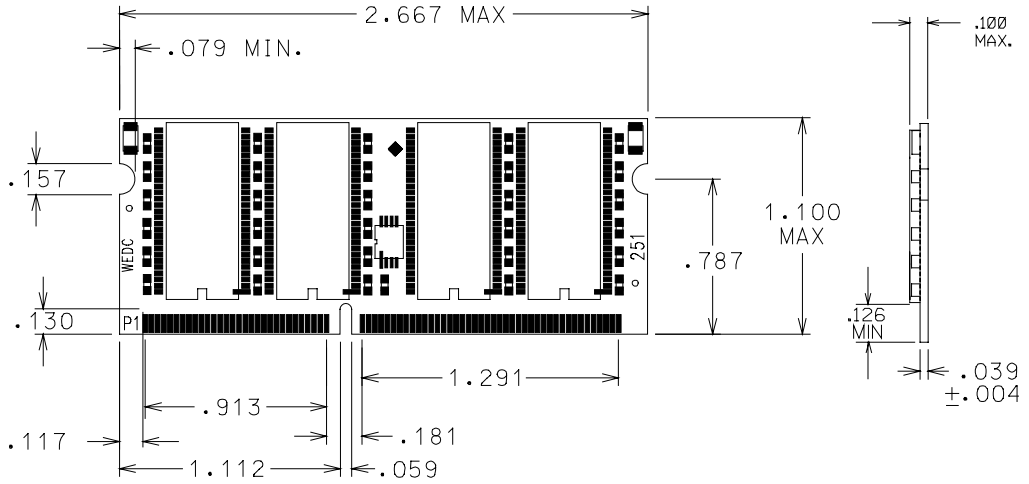
(V_{CC} = 3.3V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Version 133	Version 100	Units	Note
Operating Current (One bank active)	ICC1	Burst Length = 1 tRC ≥ tRC(min) IOL = 0mA	680	640	mA	1
Precharge Standby Current in Power Down Mode	ICC2P	CKE ≤ VIL(max), tCC = 10ns	20		mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tCC = ∞	20			
Precharge Standby Current in Non-Power Down Mode	Icc2N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are charged one time during 20	160		mA	
	Icc2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	80			
Active standby current in power-down mode	ICC3P	CKE ≥ VIL(max), tCC = 10ns	35		mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	35			
Active standby current in non power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥ VIH(min), tcc = 10ns Input signals are changed one time during 20ns	240		mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ input signals are stable	180		mA	
Operating current (Burst mode)	ICC4	Io = mA Page burst 4 Banks activated tCCD = 2CLK	920	720	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	1400	1280	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	25		mA	

Notes: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS (VIH/VIL = VDDQ/VssQ)

Ordering Information	Speed	Cas Latency
WED3DG6433V10D1	100MHz	CL=2
WED3DG6433V7D1	133MHz	CL=2
WED3DG6433V75D1	133MHz	CL=3

PACKAGE DIMENSIONS



ALL DIMENSIONS ARE IN INCHES

REV.	DATE	REQUESTED BY	DETAILS
A	11-16-01	PAUL MARIEN	CREATED
0	9-6-02	PAUL MARIEN	-CHANGE FROM ADVANCED TO FINAL