FEATURES

- HIGH OUTPUT CURRENT — 1A DC, 1.5A PEAK
- WIDE SUPPLY VOLTAGE RANGE — ±5 TO ±15V
- SEPARATE FRONT-END AND OUTPUT SUPPLIES
- LOW SATURATION VOLTAGE — 3.5V
- HIGH SLEW RATE — 10,000 V/µs @ 1A
  15,000 V/µs @ 0.5A
- LOW QUIESCENT CURRENT — 30mA
- SLEEP MODE CONTROL — 2.5mA
- HIGH FULL POWER BANDWIDTH — 70MHz

APPLICATIONS

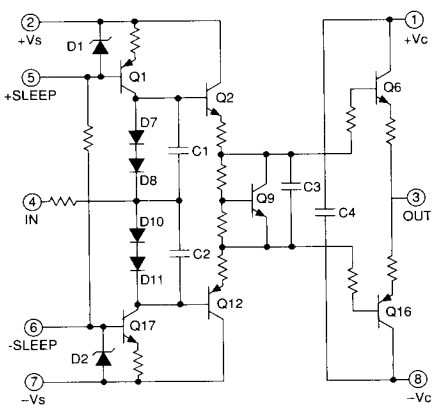
- LASER DIODE DRIVE
- GATE DRIVE FOR LARGE FETS
- SEMICONDUCTOR TESTING

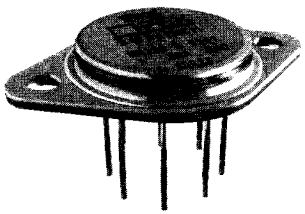
DESCRIPTION

The WB05 is a high slew rate, high current, wideband buffer capable of internal power dissipation of up to 15 watts. It provides high output currents of 1A continuous, and 1.5A peaks, under pulsed conditions. Typical circuit configuration using the WB05 will be a composite amplifier arrangement. Therefore, input capacitance has been minimized to reduce the drive requirements from the driver amplifier. A sleep mode feature has been incorporated to lower quiescent current during standby modes for battery powered applications.

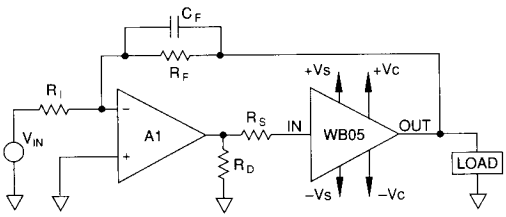
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

EQUIVALENT SCHEMATIC





TYPICAL APPLICATION

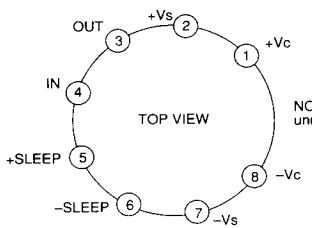


COMPOSITE AMPLIFIER CONFIGURATION

In this composite amplifier configuration, R_F and R_I should be kept as low as possible consistent with input impedance and gain requirements. Using low value resistors prevents high impedance nodes from acting as antennas, which could cause output signals to be picked up as positive feedback and result in oscillations. Low values also keep input and stray capacitance time constants low, for high speed and improved settling time. C_F is used to optimize settling time by compensating for input and stray capacitances. R_D (typically 500Ω) reduces the output impedance of A1 while R_S (typically 5-30Ω) provides damping for strays. The driver op amp must be capable of supplying adequate phase margin for itself and the WB05 at the closed loop gain used.

The driver amplifier also must be capable of providing enough current to drive R_D as well as charge the WB05's input and any other stray capacitances, at the intended slew rate. The phase shift introduced by the WB05 will increase the minimum required gain of the driver amplifier to guarantee stability. If the driver amplifier is a transimpedance amplifier, the inverting configuration shown will typically exhibit better slew rate and rise time than a noninverting configuration. This effect is due to the nature of the front end of most transimpedance amplifiers and the current available for turning on the output stage in the two different configurations. The case of the WB05 should be grounded if possible.

EXTERNAL CONNECTIONS



NOTE: If SLEEP pins are unused, leave open

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$, $+V_C$ to $-V_C$	30V
OUTPUT CURRENT, within SOA	1.5A
POWER DISSIPATION, internal at T_C = 25°C	15W
INPUT VOLTAGE RANGE	$\pm V_S$
TEMPERATURE, pins solder—10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to 150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

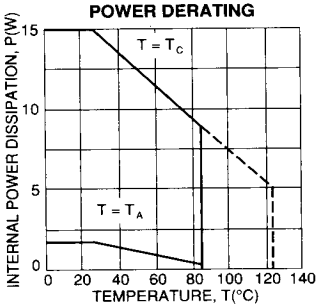
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			30	100	mV
OFFSET VOLTAGE, vs. temperature			100	500	µV/°C
BIAS CURRENT	V_{IN} = 0V		150	700	µA
INPUT CAPACITANCE			4		pF
INPUT VOLTAGE RANGE	I_{IN} < 1mA	$\pm V_S \mp 2$	$\pm V_S \mp 1.7$		V
INPUT OVERDRIVE CURRENT	$V_{IN} = +V_S$ or $V_{IN} = -V_S$		5	7	mA
PHASE SHIFT	f = 40MHz, R_L = 10Ω		8		°
	f = 150MHz, R_L = 10Ω		25		°
OUTPUT					
SATURATION VOLTAGE, (V_C-V_O)	I_O = 0.5A, $V_C = V_S - 3$	2.2	1.8		V
	I_O = 1A, $V_C = V_S - 3$	3.5	2.7		V
	I_O = 1A, $V_C = V_S$	6.5	6		V
OUTPUT CURRENT, continuous				1	A
OUTPUT CURRENT, pulsed	50% duty cycle, 10 ms pulse			1.5	A
SLEW RATE	R_L = 10Ω, V_{IN} = 15V/ns	8	10		V/ns
POWER BANDWIDTH	$V_C = V_S = \pm 15$, R_L = 20Ω	50	70		MHz
POWER BANDWIDTH	$V_C = V_S = \pm 5$, R_L = 20Ω		10		MHz
SETTLING TIME	8V step, R_L = 8Ω, to 0.1%		60		ns
	2V step, R_L = 10Ω, to 0.1%		22		ns
SMALL SIGNAL BANDWIDTH	$V_C = V_S = \pm 15$		250		MHz
OUTPUT IMPEDANCE	$V_C = V_S = \pm 15$, f = 1MHz		2		Ω
SMALL SIGNAL RISETIME	1V step, R_L = 10, $\pm V_S = \pm V_C$ = 15V		1.7		ns
SMALL SIGNAL PROP. DELAY	1V step, R_L = 10, $\pm V_S = \pm V_C$ = 15V		0.8		ns
DC GAIN	R_L = 10Ω, $\pm V_S = \pm V_C$ = 15V	0.82	0.87	0.93	V/V
POWER SUPPLY					
VOLTAGE (V_C, V_S)	Full temperature range	±5	±15	±15	V
QUIESCENT CURRENT			30	35	mA
	Sleep mode		2.5	3.5	mA
THERMAL					
RESISTANCE, AC junction to case[3]	Full temp. range, f > 60Hz		6	7.2	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		8.3	10	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	°C

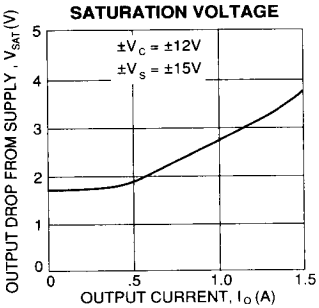
NOTES: 1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Case temperature is 25°C and the power supply voltage for all specifications is the TYP rating otherwise noted as a test condition. Case is grounded for all specifications.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

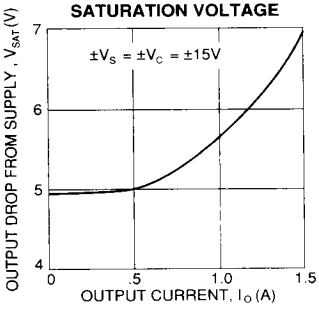
POWER DERATING



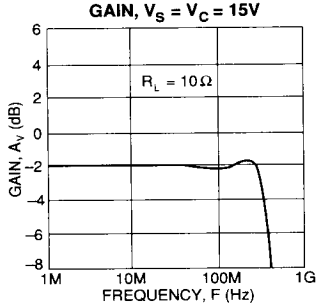
SATURATION VOLTAGE



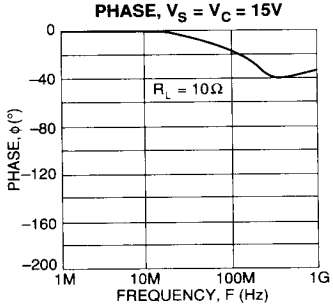
SATURATION VOLTAGE



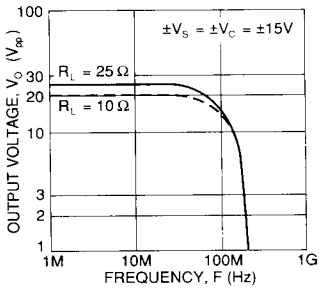
GAIN, $V_S = V_C = 15V$



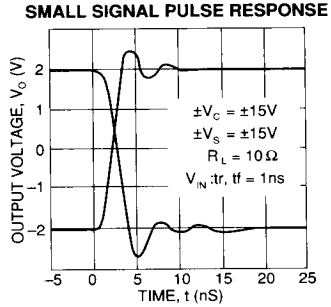
PHASE, $V_S = V_C = 15V$



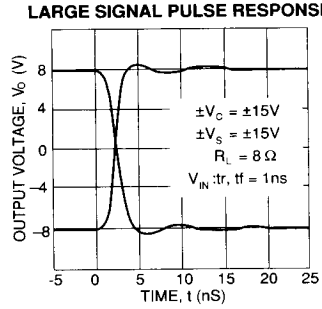
POWER RESPONSE



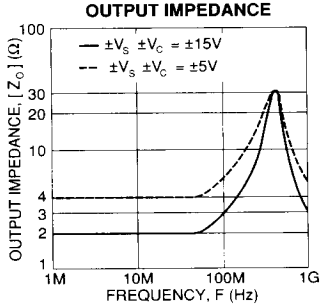
SMALL SIGNAL PULSE RESPONSE



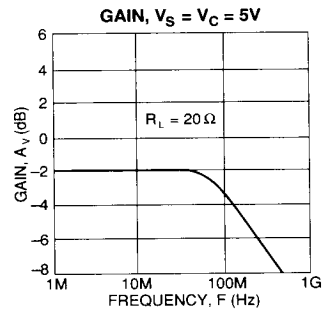
LARGE SIGNAL PULSE RESPONSE



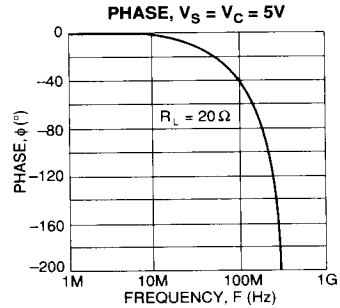
OUTPUT IMPEDANCE



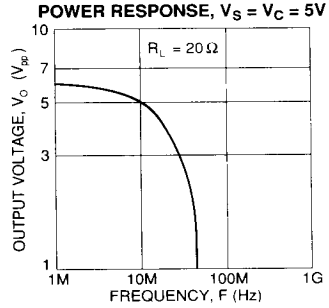
GAIN, $V_S = V_C = 5V$



PHASE, $V_S = V_C = 5V$



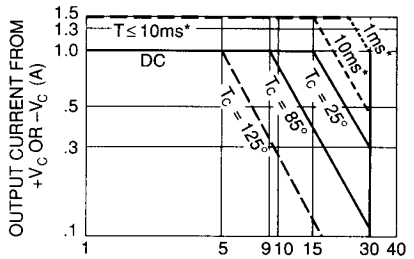
POWER RESPONSE, $V_S = V_C = 5V$



GENERAL

Please read the "General Operating Considerations" section. Additional information can be found in AN #15, "Applying the Ultra-fast WB05." For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)



*Pulsed operation: duty cycle less than or equal to 50%.

USE OF SUPPLY PINS FOR BOOST

The output stage supply voltage can be reduced or have series resistors installed to reduce power dissipation in the buffer if required. Output stage supply pins should be bypassed on the buffer side of the series resistors if they are used. Reduced output supplies (or increased input supplies) will also improve output voltage swing to the rail (V_{SAT}).

HIGH Z_L AND/OR C_L

The WB05 has been optimized for high current/low impedance loads. With large load impedances (Z_L > 100Ω) or high capacitive loading (C_L > 150pF), the buffer may show peaking in the small signal response. If required, a series R-C network of 22Ω and 68 pF can be connected from the output to ground to flatten the response.

CURRENT LIMIT

The scheme shown in Figure 1 is rather slow but is cost effective if the WB05 must be operated in a system where available supply voltages exceed ±15V or when it is desired to reduced power dissipation in the WB05 by running the output stage power supplies (±V_C) at a lower voltage. This circuit provides both regulated voltage and output current limit.

The circuit shown in Figure 2 takes advantage of the WB05 sleep pins. With Figure 2 there is a 10µs delay until the current is limited.

SLEEP MODE

The WB05 quiescent current will drop from ≈30mA to ≈2.5mA when both sleep pins are pulled within 100mV of their respective supply pins. A typical circuit for implementation is shown in Figure 3. Leave sleep pins unconnected if not used. **WARNING:** Grounding of sleep pins will cause severe damage to the op amp!

COMPOSITE AMPLIFIER CONSIDERATIONS

When the WB05 is used as shown in the "TYPICAL APPLICATION" figure, the phase shift of the WB05 is inside the feedback loop for A1 and must be considered for stability calculations. See AN #15.

SLEW RATE

The WB05 output can slew no faster than its input is driven. To achieve high input slew rates, keep driving impedances as low as practical. Note that any strays from layout will add to the input capacitance of the buffer and may form a pole with driving network resistance or driver output impedance.

LAYOUT AND BYPASS

The WB05 requires good VHF/UHF lead dress and layout due to its 250MHz small signal bandwidth. Output currents of up to 1.5A and high dV/dt at the output can cause unwanted inductive and capacitive coupling, respectively, in your layout. Recommended power supply bypassing is as follows:

Vc = Vs: On each supply rail, V+ and V-, place in parallel the following capacitors:
- C1, C4 = 330 to 1000 pF ceramic capacitor
- C2, C5 = 0.01 to 0.033 µF ceramic capacitor
- C3, C6 = 2.2 to 6.8 µF low ESR tantalum electrolytic

Vc ≠ Vs: On each Vc supply rail, +Vc and -Vc, place in parallel the following capacitors:
- C1, C6 = 330 to 1000 pF ceramic capacitor
- C2, C7 = 0.01 to 0.033 µF ceramic capacitor
- C3, C8 = 2.2 to 6.8 µF low ESR tantalum electrolytic

On each Vs supply rail, +Vs and -Vs, place in parallel the following capacitors:
- C4, C9 = 0.01 to 0.033 µF ceramic capacitor
- C5, C10 = 330 to 1,000pF ceramic capacitor

All capacitors must be as close to the buffer supply pins as possible, with short leads (1/8" to 1/4") and/or short, wide PCB traces to minimize stray inductances.

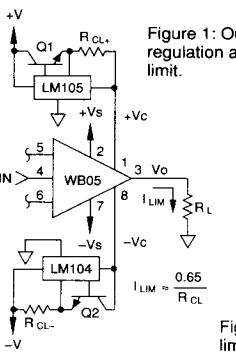


Figure 1: Output voltage regulation and current limit.

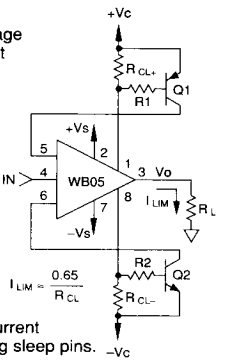


Figure 2: Current limiting using sleep pins.

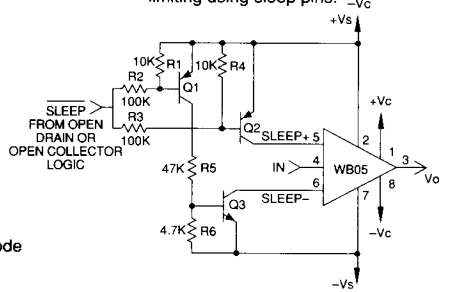


Figure 3: Sleep mode interface.

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