

NN514265 / NN514265A series **EDO (Hyper Page) Mode** **CMOS 256K × 16bit Dynamic RAM**



DESCRIPTION

The NN514265/A series is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 16 bits. The NN514265/A series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN514265/A series features an EDO (Hyper Page) mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit The NN514265/A series to be packaged in a standard 40-pin plastic SOJ, 44-pin plastic TSOP TYPEII. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

FEATURES

- 262,144 × 16 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

NN514265

Parameter	-45	-50	-60	-70
Max. RAS Access Time (t_{RAC})	45ns	50ns	60ns	70ns
Max. CAS Access Time (t_{CAC})	15ns	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	23ns	25ns	30ns	35ns
Min. Read/Write Cycle Time (t_{rc})	80ns	90ns	110ns	130ns

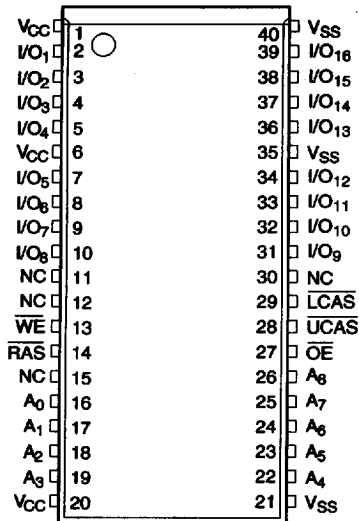
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Parameter	-35	-40	-45	-50	-60
Max. RAS Access Time (t_{RAC})	35ns	40ns	45ns	50ns	60ns
Max. CAS Access Time (t_{CAC})	10ns	10ns	13ns	13ns	15ns
Max. Column Address Access Time (t_{AA})	19ns	21ns	23ns	25ns	30ns
Min. Read/Write Cycle Time (t_{rc})	60ns	75ns	80ns	84ns	104ns

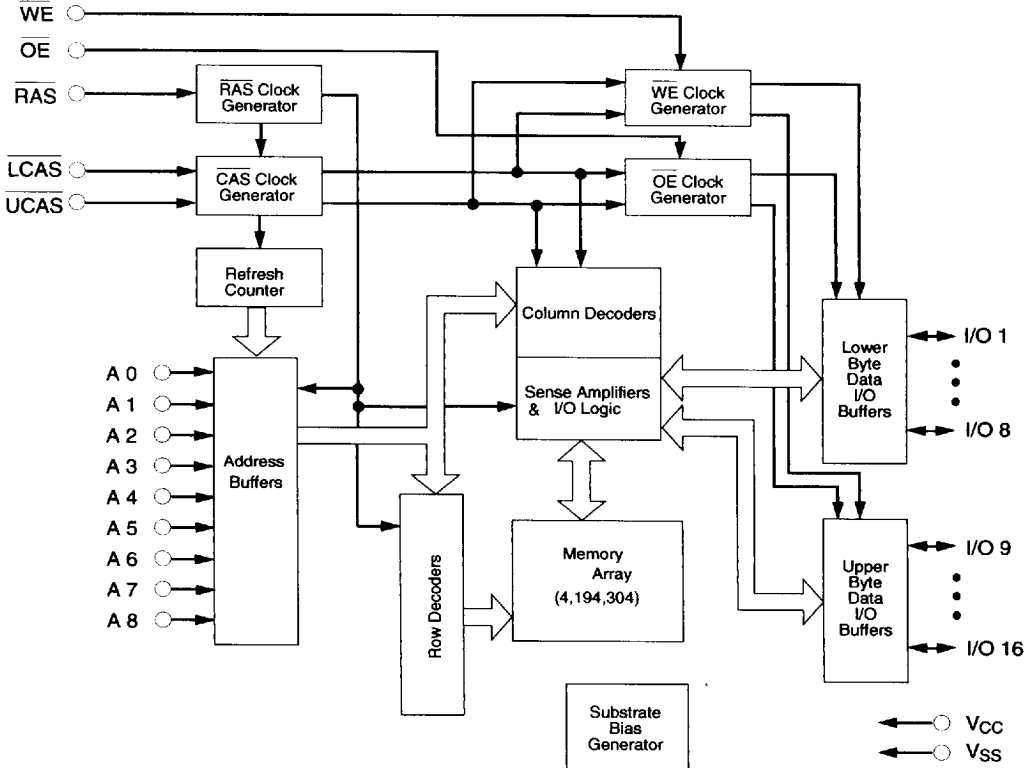
- EDO (Hyper Page) Mode Operation
 - Separate CAS (UCAS, LCAS) for Byte Selection
 - Byte Read/Write Mode Operation
 - Low Power Operation
 - Low Standby Current (CMOS level inputs)
 - Standard 1mA
 - L version 100μA
 - 512 Refresh Cycles
 - Standard distributed across 8ms
 - L version distributed across 128ms
 - Self Refresh Mode (L version)
 - All inputs/Outputs and Clocks fully TTL and CMOS compatible
 - Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
 - High Reliability Package
 - Plastic 40pin SOJ (P40SJ-2B)
 - Plastic 44pin TSOP TYPEII (P44/40TP-3B) (P44/40TP-3B-L)*
- *Note: Only for NN514265A

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PIN CONFIGURATION (TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V _{SS}	V _{in} , V _{out}	-1 to 7	V
Voltage on V _{CC} Relative to V _{SS}	V _{CC}	-1 to 7	V
Storage Temperature (Plastic)	T _{stg}	-55 to +125	°C
Power Dissipation	P _d	1.0	W
Ambient Operating Temperature	T _a	0 to +70	°C
Short Circuit Output Current	I _{out}	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V _{IL}	Input Low Voltage, All Inputs	-0.5	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)
(NN514265)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-45		180	mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
		-50		160	mA		
		-60		150	mA		
		-70		130	mA		
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
	Standby Current (L version)			100	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-45		180	mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
		-50		160	mA		
		-60		150	mA		
		-70		130	mA		
I _{CC4}	EDO (Hyper Page) Mode Current	-45		125	mA	t _{HPC} = t _{HPC} (min.) RAS = V _{IL} CAS, Address cycling	1, 2
		-50		120	mA		
		-60		110	mA		
		-70		100	mA		
I _{CC5}	Refresh Current (CAS before RAS refresh)	-45		180	mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
		-50		160	mA		
		-60		150	mA		
		-70		130	mA		
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			150	μA	512 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current (L version)			150	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A8)	—	5	pF
C _{IN2}	RAS, UCAS, LCAS, WE, OE	—	5	pF
C _{OUT}	I/O1 ~ I/O16	—	7	pF

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)
(NN514265A)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-35 -40 -45 -50 -60		180 160 140 120 100	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0	mA	RAS = $\overline{\text{CAS}} \geq (V_{CC} - 0.2V)$	
				2.0	mA	RAS = $\overline{\text{CAS}} \geq V_{IH}$	
I _{CC2}	Standby Current (L version)			150	μA	RAS = $\overline{\text{CAS}} \geq (V_{CC} - 0.2V)$ All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-35 -40 -45 -50 -60		180 160 140 120 100	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, $\overline{\text{CAS}} = V_{IH}$	1
I _{CC4}	EDO (Hyper Page) Mode Current	-35 -40 -45 -50 -60		110 100 90 80 70	mA mA mA mA mA	t _{HPC} = t _{HPC} (min.) RAS = V _{IL} CAS, Address cycling	1,2
I _{CC5}	Refresh Current (CAS before RAS refresh)	-35 -40 -45 -50 -60		180 160 140 120 100	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			200	μA	512 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current (L version)			200	μA	RAS = $\overline{\text{CAS}} \leq (V_{SS} + 0.2V)$ All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), $\overline{\text{CAS}} \geq V_{IH}(\text{min.})$ 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A8)	—	5	pF
C _{IN2}	RAS, UCAS, LCAS, WE, OE	—	5	pF
C _{OUT}	I/O1 ~ I/O16	—	7	pF

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AC ELECTRICAL CHARACTERISTICS

Test conditions : $V_{IH}/V_{IL} = 2.4V/0.8V$ $V_{OH}/V_{OL} = 2.0V/0.8V$ output loading $C_L = 100pF + 2TTL$

Operating conditions : ($0^\circ C \leq T_a \leq 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) (NOTES 3, 4, 5)

(NN514265)

NO.	NOTES		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from CAS	—	15	—	15	—	15	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from CAS Precharge	—	28	—	30	—	35	—	40	ns	13,14
3	t_{AVOV}	t_{AA}	Access Time from Column Address	—	23	—	25	—	30	—	35	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from RAS	—	45	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	CAS Hold Time	30	—	35	—	40	—	55	—	ns	
6	t_{RL1CX}	t_{CHS}	CAS Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	CAS Hold Time (CAS before RAS Refresh)	8	—	8	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	CAS Precharge Time (CAS before RAS Refresh)	8	—	8	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	CAS Precharge Time (EDO (Hyper Page) Mode)	5	—	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	CAS Pulse Width	8	100K	8	100K	10	100K	15	100K	ns	
11	t_{CL1RL2}	t_{CSR}	CAS Setup Time (CAS before RAS Refresh)	5	—	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	CAS to Output in Low-Z	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	CAS to RAS Precharge Time	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	CAS to WE Delay Time	35	—	35	—	35	—	50	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	8	—	8	—	10	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to RAS	30	—	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to CAS Lead Time	13	—	13	—	18	—	23	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to RAS Lead Time	22	—	24	—	30	—	35	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to WE Delay Time	48	—	50	—	50	—	65	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	8	—	8	—	10	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time (EDO (Hyper Page) Mode)	0	—	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	ns	12
24	t_{OL1QV}	t_{OEA}	OE Access Time	—	13	—	13	—	15	—	20	ns	
25	t_{WL1OL2}	t_{OEH}	OE Command Hold Time	13	—	13	—	15	—	20	—	ns	
26	t_{GH2GL2}	t_{OPZ}	OE Pulse Width for Output Disable When CAS High	5	—	7	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	OE Setup Time to CAS High	5	—	7	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	OE Setup Time to RAS High	5	—	7	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	OE to Data Delay Time	7	—	8	—	10	—	10	—	ns	
30	t_{GL2QX}	t_{OLZ}	OE to Output in low-Z	0	—	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	12	0	13	0	15	0	15	ns	10
32	t_{CH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to OE	0	10	0	10	0	15	0	15	ns	
33	t_{RHQZ}	t_{OFFR}	Output Buffer Turn-off Delay Time Referenced to RAS	0	12	0	13	0	15	0	15	ns	16

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NPNX

NO.	SYMBOL		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
34	tWL2QZ	tWEZ	Output Buffer Turn-off Delay Time Referenced to WE	0	12	0	13	0	15	0	15	ns	
35	tCL1RH1	tRSH	RAS Hold Time	13	—	13	—	15	—	20	—	ns	
36	tOL1RH1	tROH	RAS Hold Time Referenced to OE	8	—	8	—	10	—	10	—	ns	
37	tCH2RH1	tRHCP	RAS Hold Time Referenced CAS Precharge	28	—	30	—	35	—	40	—	ns	
38	tRH2RL2	tRP	RAS Precharge Time	25	—	25	—	30	—	40	—	ns	
39	tRH2RL2	tRPS	RAS Precharge Time (Self Refresh Mode)	80	—	90	—	110	—	130	—		
40	tRL1RH1	tRAS	RAS Pulse Width	45	100K	50	100K	60	100K	70	100K	ns	
41	tRL1RH1	tRASS	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	μs	
42	tRL1RH1	tRASP	RAS Pulse Width (EDO (Hyper Page) Mode)	45	100K	50	100K	60	100K	70	100K	ns	
43	tRL1CL1	tRCD	RAS to CAS Delay Time	13	30	13	35	13	45	13	50	ns	6
44	tRH2CL2	tRPC	RAS to CAS Precharge Time	10	—	10	—	10	—	10	—	ns	
45	tRL1AV	tRAD	RAS to Column Address Delay Time	11	20	11	23	11	30	11	35	ns	7
46	tRL2QX	tRLZ	RAS To Output in Low-Z	0	—	0	—	0	—	0	—	ns	
47	tRL1WL2	tRWD	RAS to WE Delay Time	60	—	65	—	75	—	100	—	ns	11
48	tCH2WL2	tRCH	Read Command Hold Time	0	—	0	—	0	—	0	—	ns	9
49	tRH2WL2	tRRH	Read Command Hold Time Referenced to RAS	5	—	5	—	5	—	5	—	ns	9
50	tWH2CL2	tRCS	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
51	tRL2RL2	tRC	Random Read or Write Cycle Time	80	—	90	—	110	—	130	—	ns	
52	tCL2CL2	tHPC	Read or Write Cycle Time (EDO (Hyper Page) Mode)	20	—	20	—	25	—	30	—	ns	13,14
53	tRL2RL2	tRMW	Read-Modify-Write Cycle Time	120	—	125	—	135	—	185	—	ns	
54	tCL2CL2	tPRMW	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	57	—	57	—	66	—	95	—	ns	13,14
55	tREF	tREF	Refresh Period	—	8	—	8	—	8	—	8	ms	15
56	tRL1AX	tRAH	Row Address Hold Time	8	—	8	—	8	—	8	—	ns	
57	tAVRL2	tASR	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
58	tT	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	ns	4,5
59	tWL1WH1	tWPZ	WE Pulse Width for Disable When CAS High	5	—	7	—	7	—	7	—	ns	
60	tCL1WH1	tWCH	Write Command Hold Time	8	—	8	—	10	—	15	—	ns	
61	tWL1WH1	tWP	Write Command Pulse Width	8	—	8	—	10	—	15	—	ns	
62	tWL1CL2	tWCS	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	11
63	tWL1CH1	tCWL	Write Command to CAS Lead Time	8	—	8	—	15	—	20	—	ns	
64	tWL1RH1	tRWL	Write Command to RAS Lead Time	8	—	8	—	10	—	20	—	ns	

A.C. ELECTRICAL CHARACTERISTICS

Test conditions : $V_{IH} / V_{IL} = 2.4V / 0.8V$ $V_{OH} / V_{OL} = 2.0V / 0.8V$ output loading $C_L = 50pF + 1TTL$

Operating conditions : ($0^\circ C \leq T_a \leq 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) (NOTES 3, 4, 5)

(NN514265A)

NO.	NOTES		PARAMETER	-35		-40		-45		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	10	—	10	—	15	—	15	—	15	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	21	—	23	—	28	—	30	—	35	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	19	—	21	—	23	—	25	—	30	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	35	—	40	—	45	—	50	—	60	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	27	—	30	—	30	—	35	—	40	—	ns	
6	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	8	—	8	—	8	—	8	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	7	—	8	—	8	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (EDO (Hyper Page) Mode)	5	—	5	—	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	6	100K	6	100K	8	100K	8	100K	10	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	—	20	—	35	—	35	—	35	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	6	—	6	—	8	—	8	—	10	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	25	—	28	—	30	—	35	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	9	—	11	—	13	—	13	—	18	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	18	—	20	—	22	—	24	—	30	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	29	—	31	—	48	—	50	—	50	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	6	—	6	—	8	—	8	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time (EDO (Hyper Page) Mode)	0	—	0	—	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	0	—	ns	12
24	t_{CL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	10	—	10	—	13	—	13	—	15	ns	
25	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	5	—	5	—	13	—	13	—	15	—	ns	
26	t_{GH2GL2}	t_{OPZ}	$\overline{OE}$ Pulse Width for Output Disable When $\overline{CAS}$ High	5	—	5	—	5	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	$\overline{OE}$ Setup Time to $\overline{CAS}$ High	5	—	5	—	5	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	$\overline{OE}$ Setup Time to $\overline{RAS}$ High	5	—	5	—	5	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	5	—	6	—	7	—	8	—	10	—	ns	
30	t_{GL2QX}	t_{OLZ}	$\overline{OE}$ to Output in low-Z	0	—	0	—	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	8	0	10	0	12	0	13	0	15	ns	10
32	t_{CH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	8	0	8	0	10	0	10	0	15	ns	

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NO.	SYMBOL		PARAMETER	-35		-40		-45		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
33	t _{RHQZ}	t _{OFF}	Output Buffer Turn-off Delay Time Referenced to RAS	0	8	0	10	0	12	0	13	0	15	ns	16
34	t _{WL2QZ}	t _{WEZ}	Output Buffer Turn-off Delay Time Referenced to WE	0	12	0	12	0	12	0	13	0	15	ns	
35	t _{CL1RH1}	t _{RSH}	RAS Hold Time	8	—	8	—	13	—	13	—	15	—	ns	
36	t _{OL1RH1}	t _{ROH}	RAS Hold Time Referenced to OE	7	—	8	—	8	—	8	—	10	—	ns	
37	t _{CH2RH1}	t _{RHCP}	RAS Hold Time Referenced CAS Precharge	24	—	26	—	28	—	30	—	35	—	ns	
38	t _{RH2RL2}	t _{RP}	RAS Precharge Time	20	—	25	—	25	—	25	—	30	—	ns	
39	t _{RH2RL2}	t _{RPS}	RAS Precharge Time (Self Refresh Mode)	60	—	70	—	80	—	90	—	110	—	ns	
40	t _{RL1RH1}	t _{RAS}	RAS Pulse Width	35	100K	40	100K	45	100K	50	100K	60	100K	ns	
41	t _{RL1RH1}	t _{RASS}	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	300	—	μs	
42	t _{RL1RH1}	t _{RASP}	RAS Pulse Width (EDO (Hyper Page) Mode)	35	100K	40	100K	45	100K	50	100K	60	100K	ns	
43	t _{RL1CL1}	t _{RCD}	RAS to CAS Delay Time	11	25	12	30	13	30	13	35	13	45	ns	6
44	t _{RH2CL2}	t _{RPC}	RAS to CAS Precharge Time	0	—	0	—	10	—	10	—	10	—	ns	
45	t _{RL1AV}	t _{RAD}	RAS to Column Address Delay Time	9	16	10	19	11	20	11	23	11	30	ns	7
46	t _{RL2QX}	t _{RLZ}	RAS To Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns	
47	t _{RL1WL2}	t _{RWD}	RAS to WE Delay Time	45	—	50	—	60	—	65	—	75	—	ns	11
48	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	0	—	ns	9
49	t _{RH2WL2}	t _{RRH}	Read Command Hold Time Referenced to RAS	5	—	5	—	5	—	5	—	5	—	ns	9
50	t _{WH2CL2}	t _{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
51	t _{RL2RL2}	t _{RC}	Random Read or Write Cycle Time	60	—	75	—	80	—	84	—	104	—	ns	
52	t _{CL2CL2}	t _{HPC}	Read or Write Cycle Time (EDO (Hyper Page) Mode)	13	—	15	—	20	—	20	—	25	—	ns	13,14
53	t _{RL2RL2}	t _{RMW}	Read-Modify-Write Cycle Time	80	—	100	—	120	—	125	—	135	—	ns	
54	t _{CL2CL2}	t _{PRMW}	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	52	—	55	—	57	—	57	—	66	—	ns	13,14
55	t _{REF}	t _{REF}	Refresh Period	—	8	—	8	—	8	—	8	—	8	ms	15
56	t _{RL1AX}	t _{RAH}	Row Address Hold Time	7	—	8	—	8	—	8	—	8	—	ns	
57	t _{AVRL2}	t _{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
58	t _T	t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	2	50	ns	4,5
59	t _{WL1WH1}	t _{WPZ}	WE Pulse Width for Disable When CAS High	5	—	5	—	5	—	7	—	7	—	ns	
60	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	6	—	6	—	8	—	8	—	10	—	ns	
61	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	6	—	6	—	8	—	8	—	10	—	ns	
62	t _{WL1CL2}	t _{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	11
63	t _{WL1CH1}	t _{CWL}	Write Command to CAS Lead Time	6	—	6	—	8	—	8	—	15	—	ns	
64	t _{WL1RH1}	t _{RWL}	Write Command to RAS Lead Time	8	—	8	—	8	—	8	—	10	—	ns	

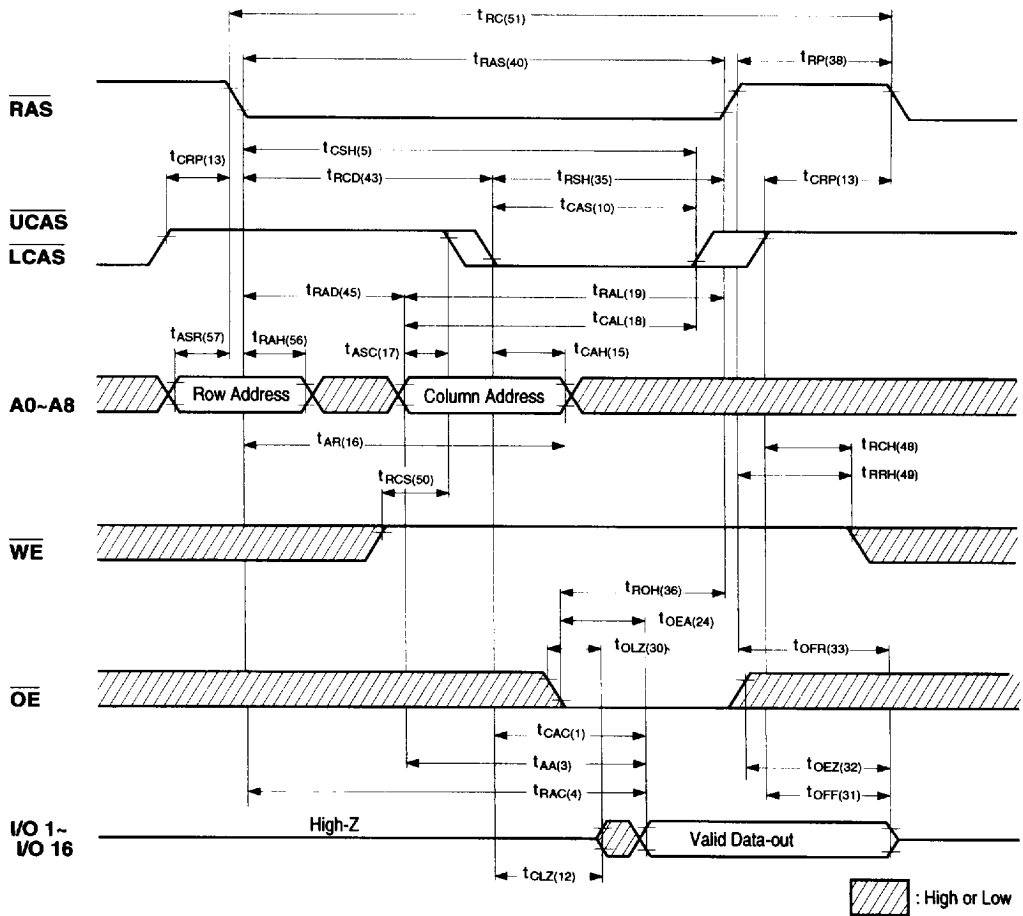
9005650 0001261 9T4

Notes:

3. Eight Initialization Cycles are required following a 200 μ s pause after Power Up. These Initialization Cycles may consist of any combination of the following : RAS only refresh Cycles, Read Cycles, Write Cycles, CAS before RAS refresh Cycles.
4. AC measurements assume $t_T=3$ ns.
5. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
6. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
7. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
8. Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
11. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{CPA} .
14. $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.
15. $t_{REF}=128$ msec for Long Refresh version (L version).
16. t_{OFR} applies only when $\overline{\text{CAS}}$ is high.

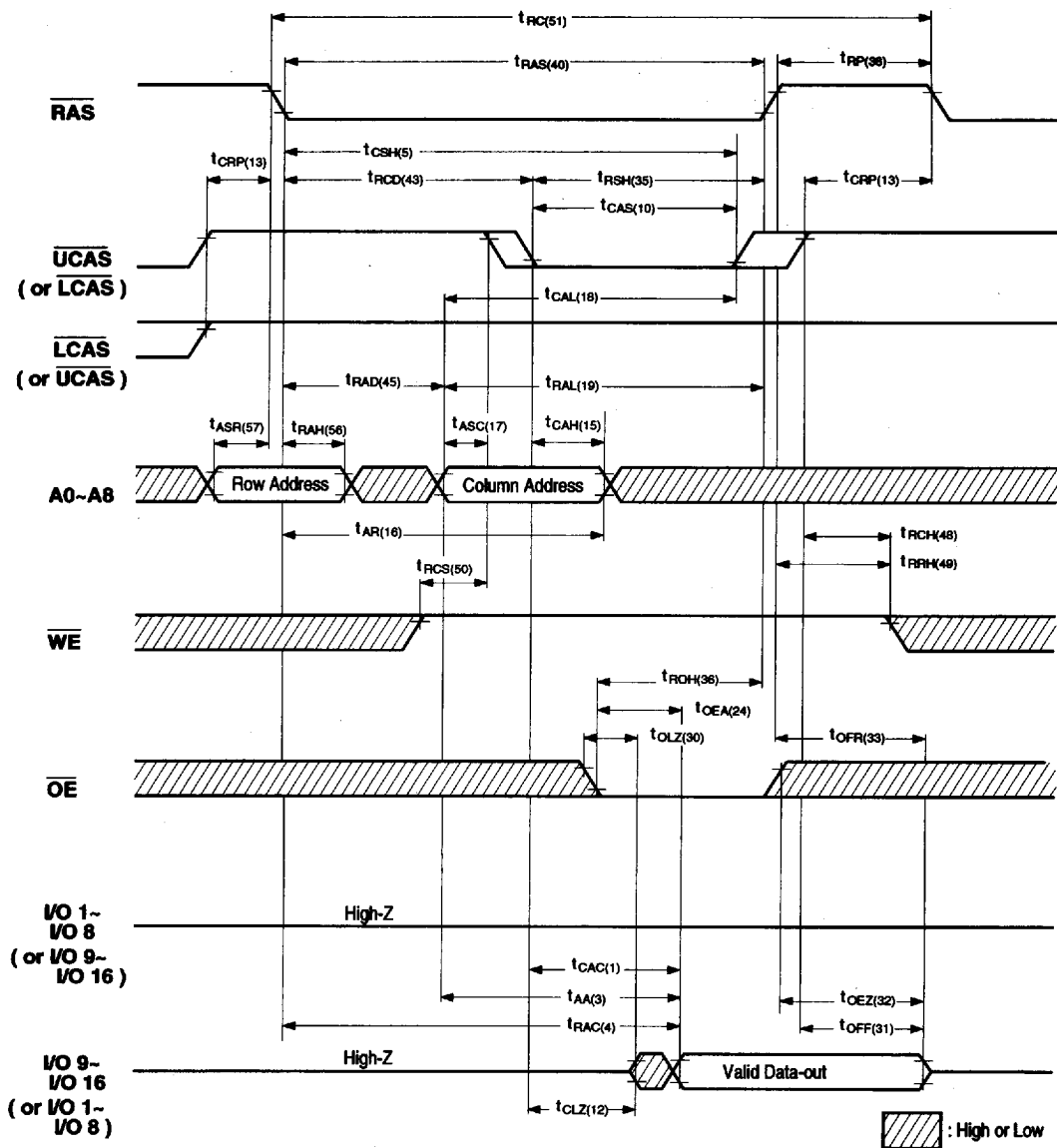
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WORD READ CYCLE



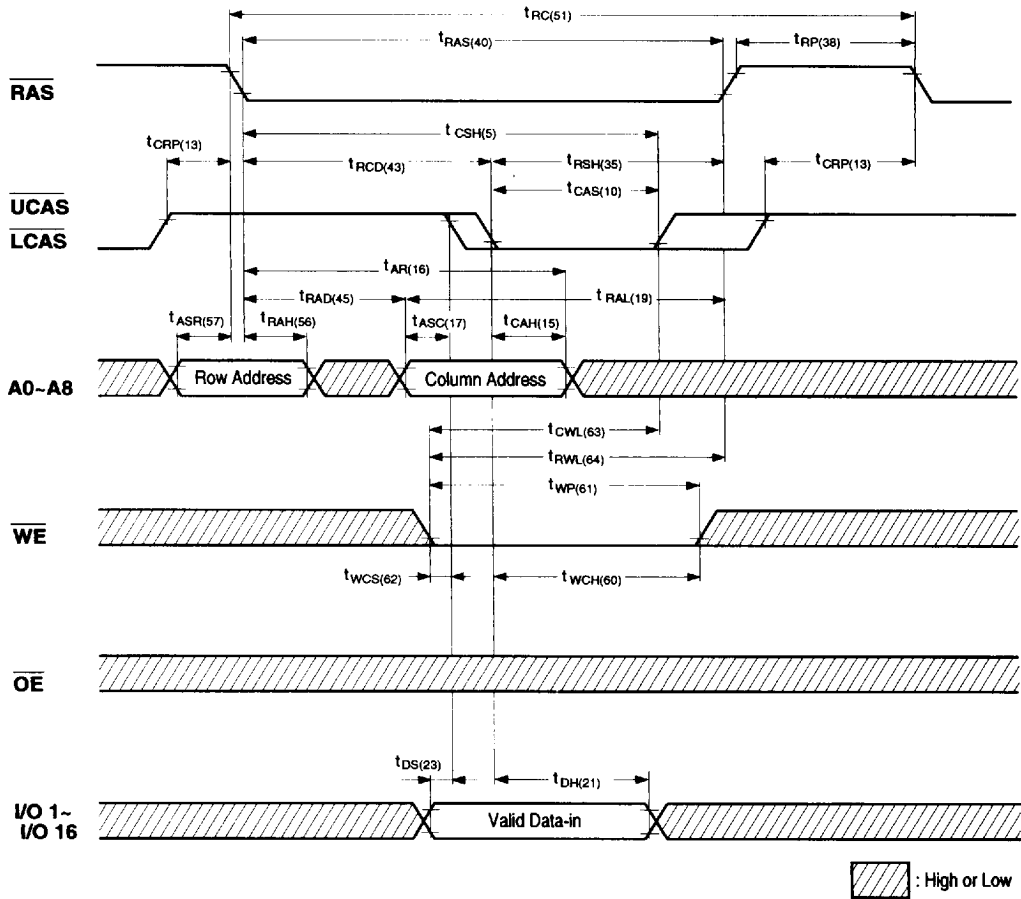
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BYTE READ CYCLE



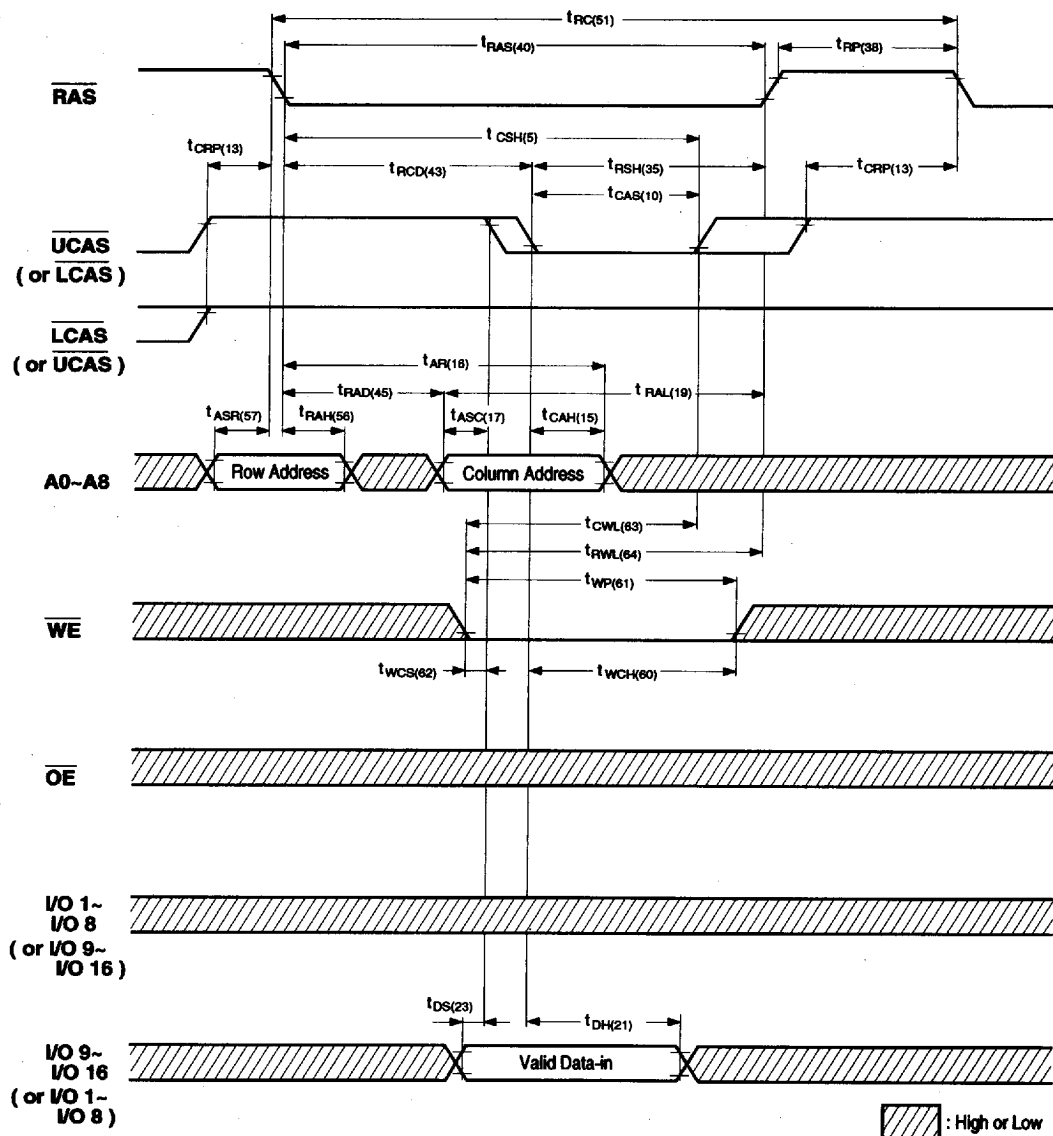
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WORD WRITE CYCLE (EARLY WRITE)



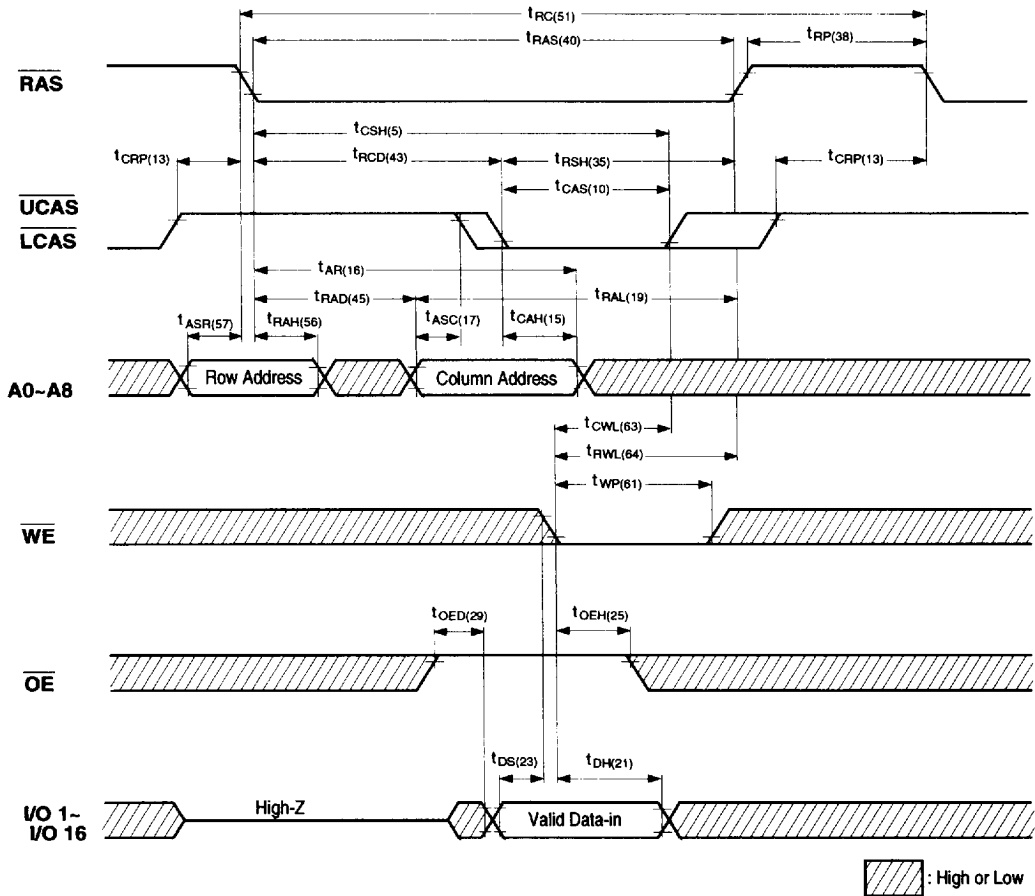
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BYTE WRITE CYCLE (EARLY WRITE)



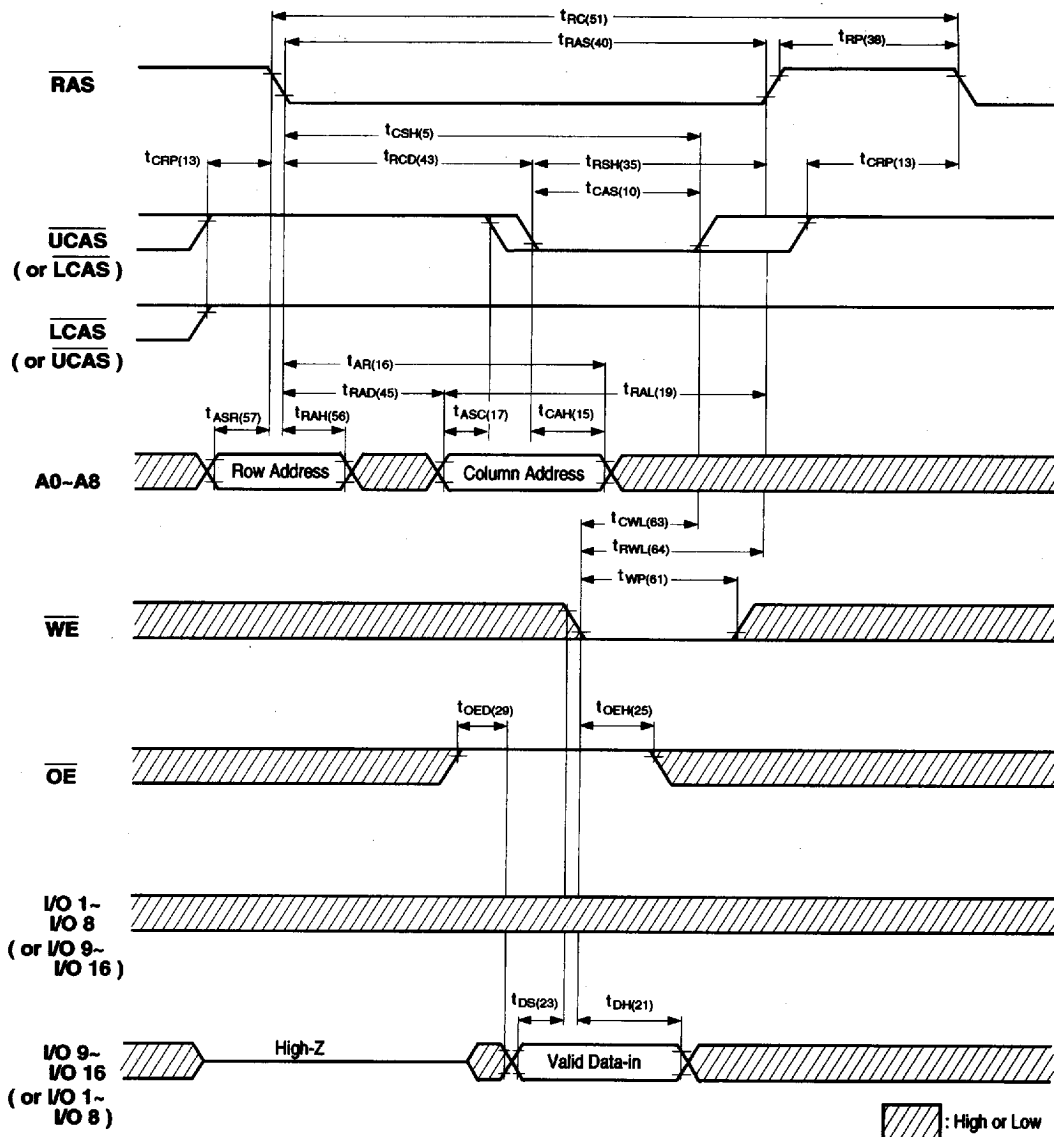
9005650 0001266 486

WORD WRITE CYCLE ($\overline{\text{OE}}$ -CONTROLLED WRITE)



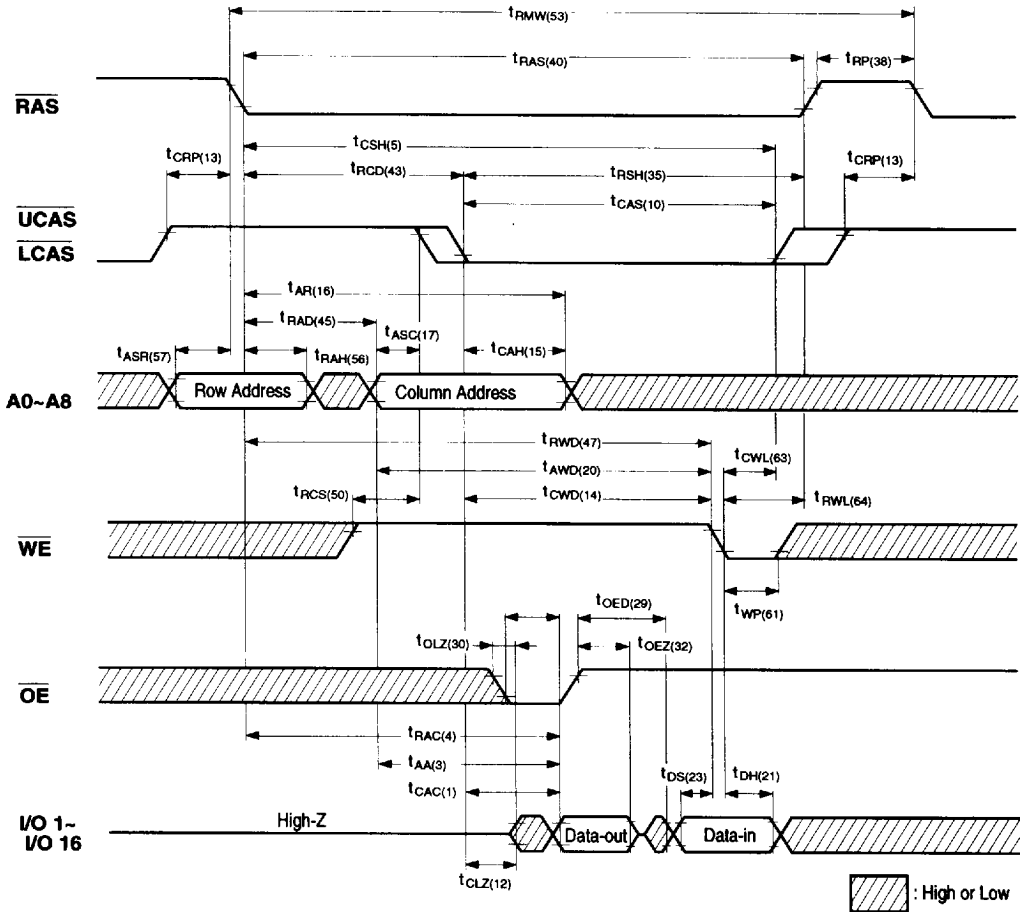
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BYTE WRITE CYCLE ($\overline{\text{OE}}$ -CONTROLLED WRITE)



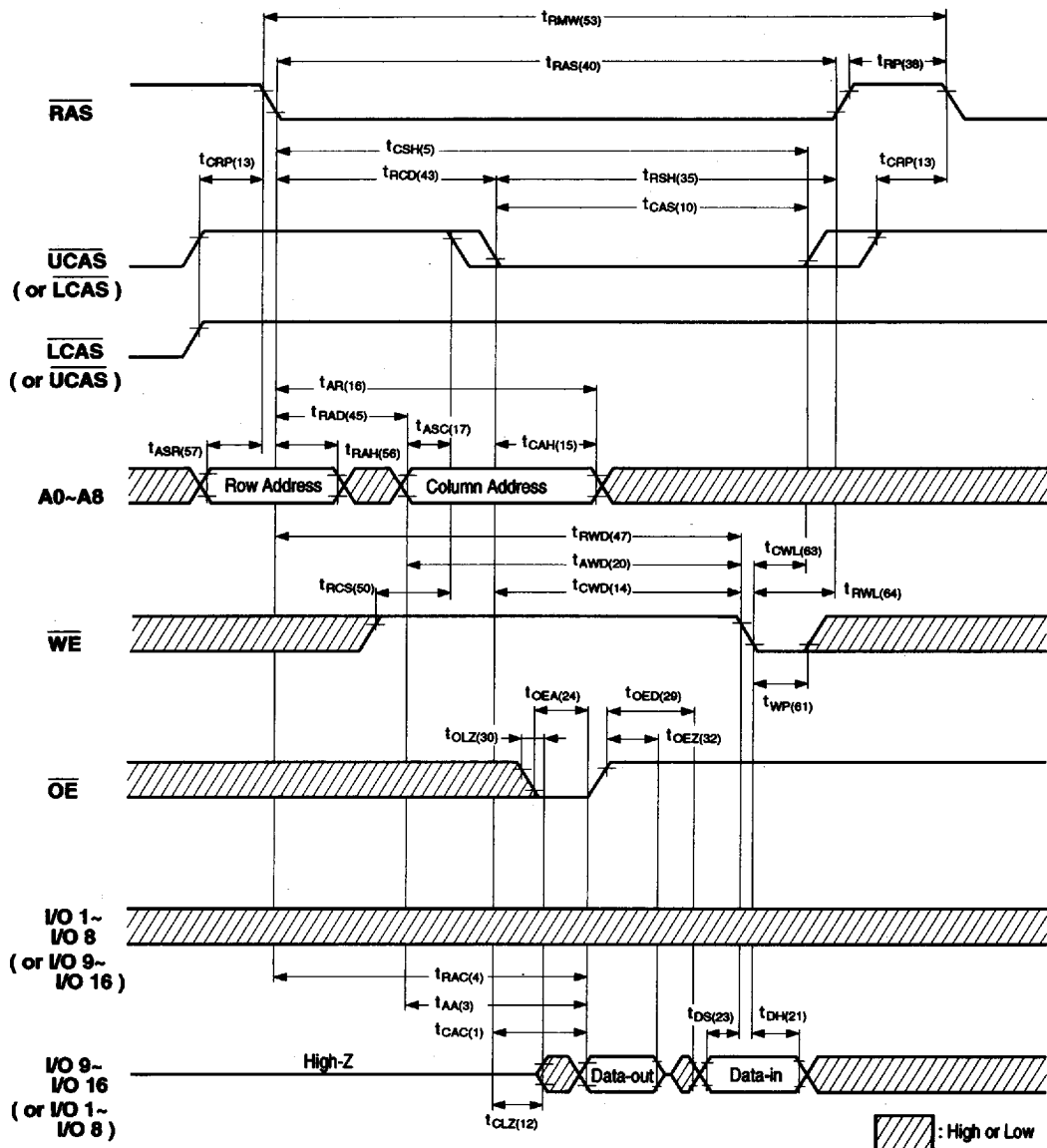
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WORD READ-MODIFY-WRITE CYCLE



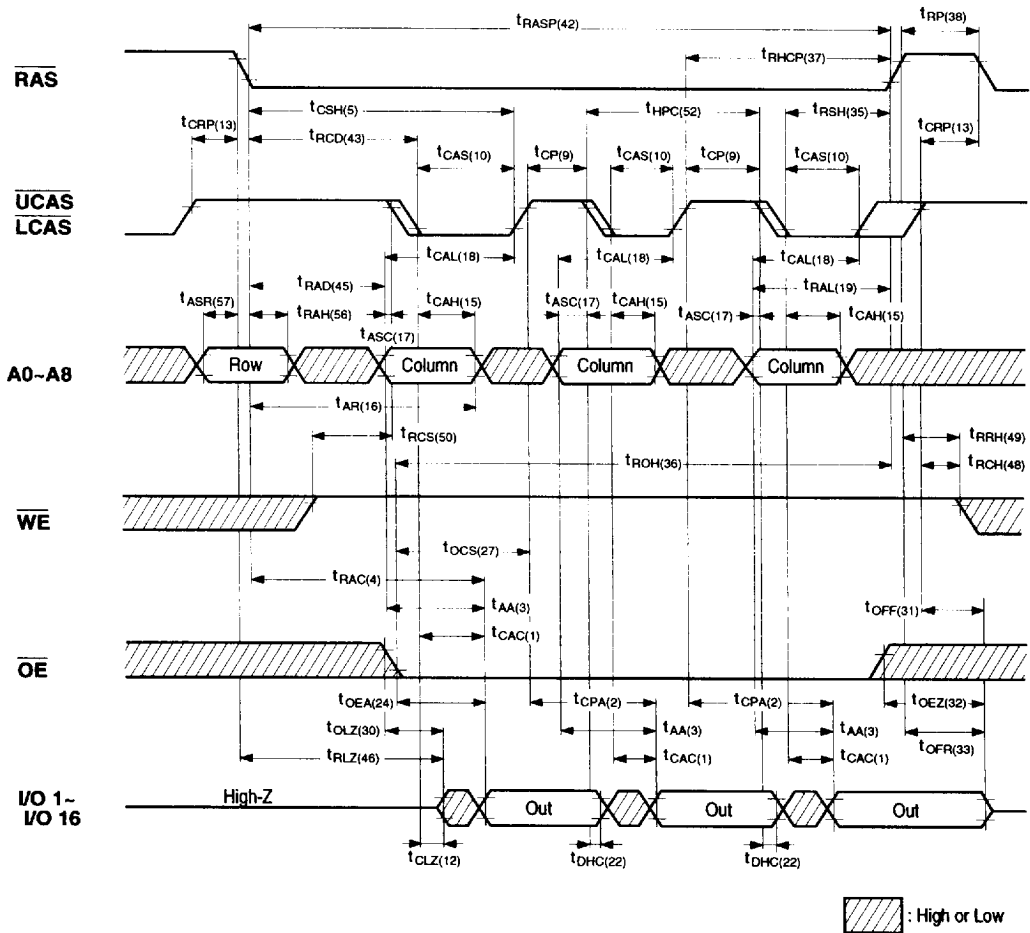
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BYTE READ-MODIFY-WRITE CYCLE



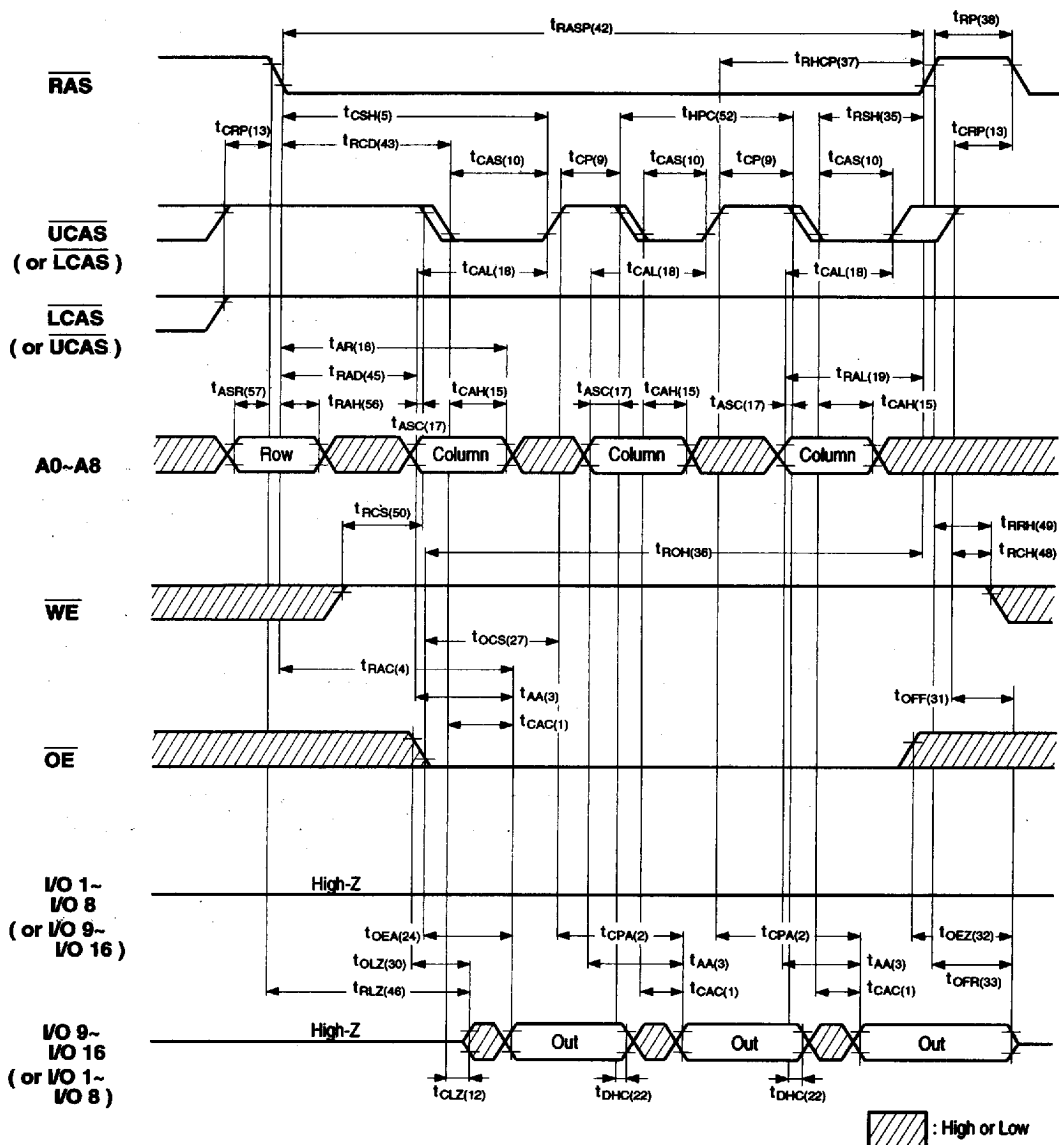
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EDO (HYPER PAGE) MODE WORD READ CYCLE



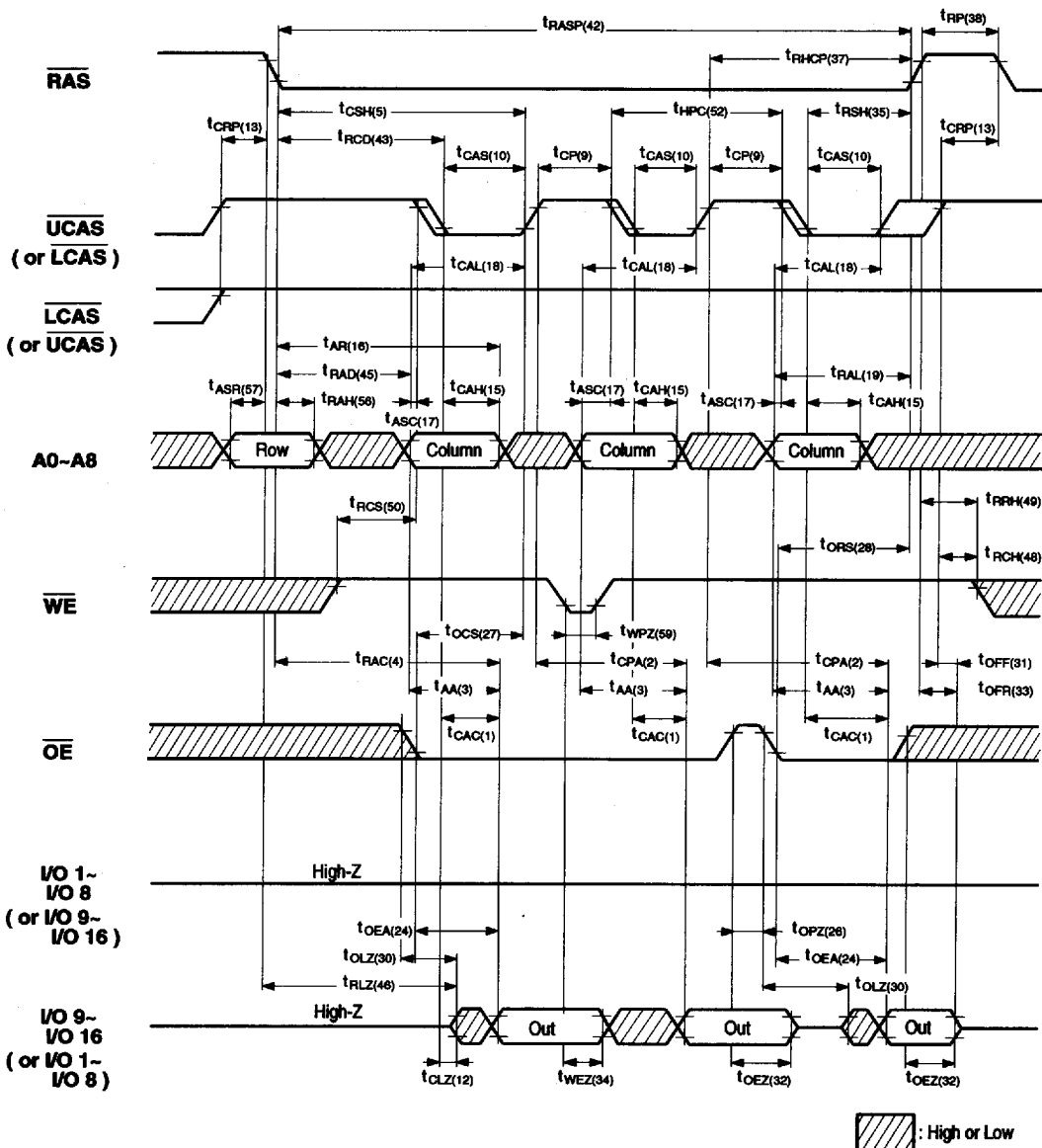
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EDO (HYPER PAGE) MODE BYTE READ CYCLE



9005650 0001272 78T

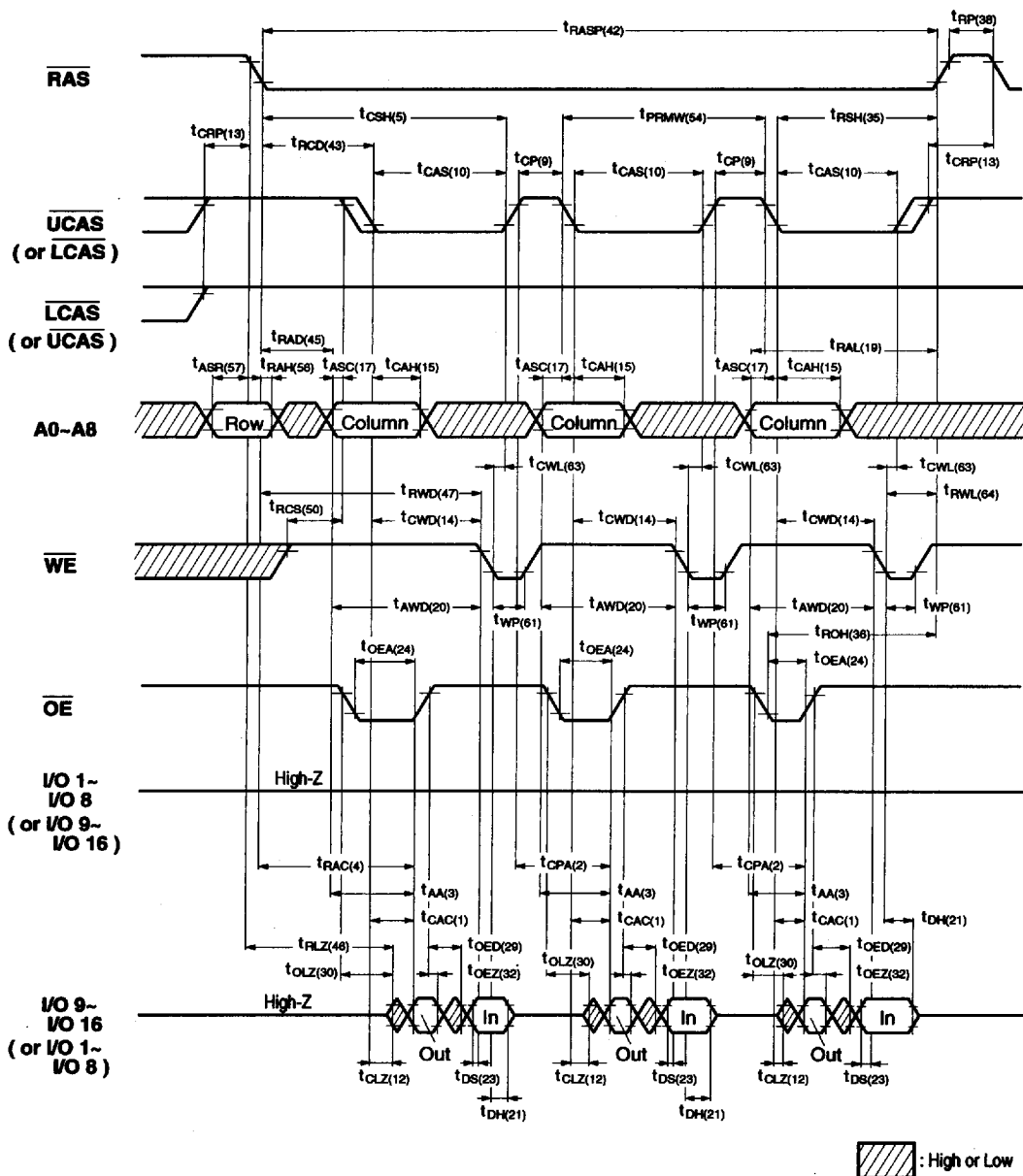
EDO (HYPER PAGE) MODE BYTE READ CYCLE (OE AND WE CONTROLLED OUTPUT)



9005650 0001274 552

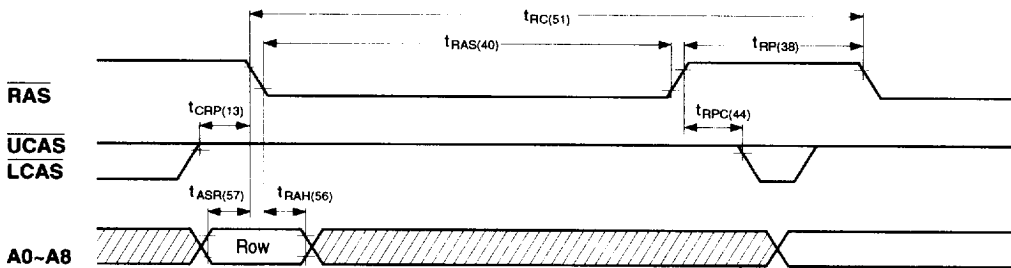


EDO (HYPER PAGE) MODE BYTE READ-MODIFY-WRITE CYCLE



9005650 0001278 1T8

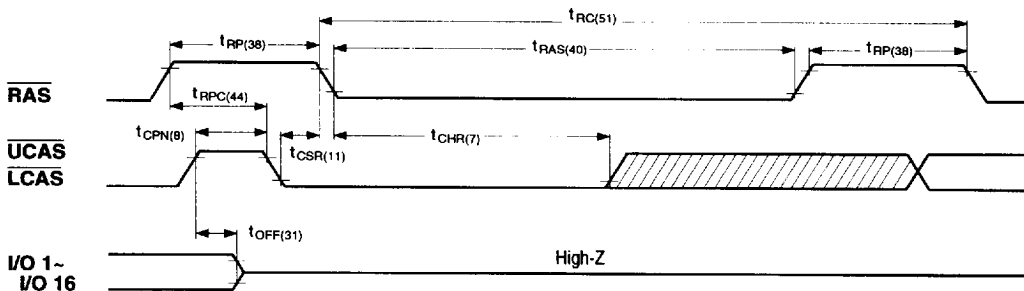
RAS ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

CAS BEFORE RAS REFRESH CYCLE

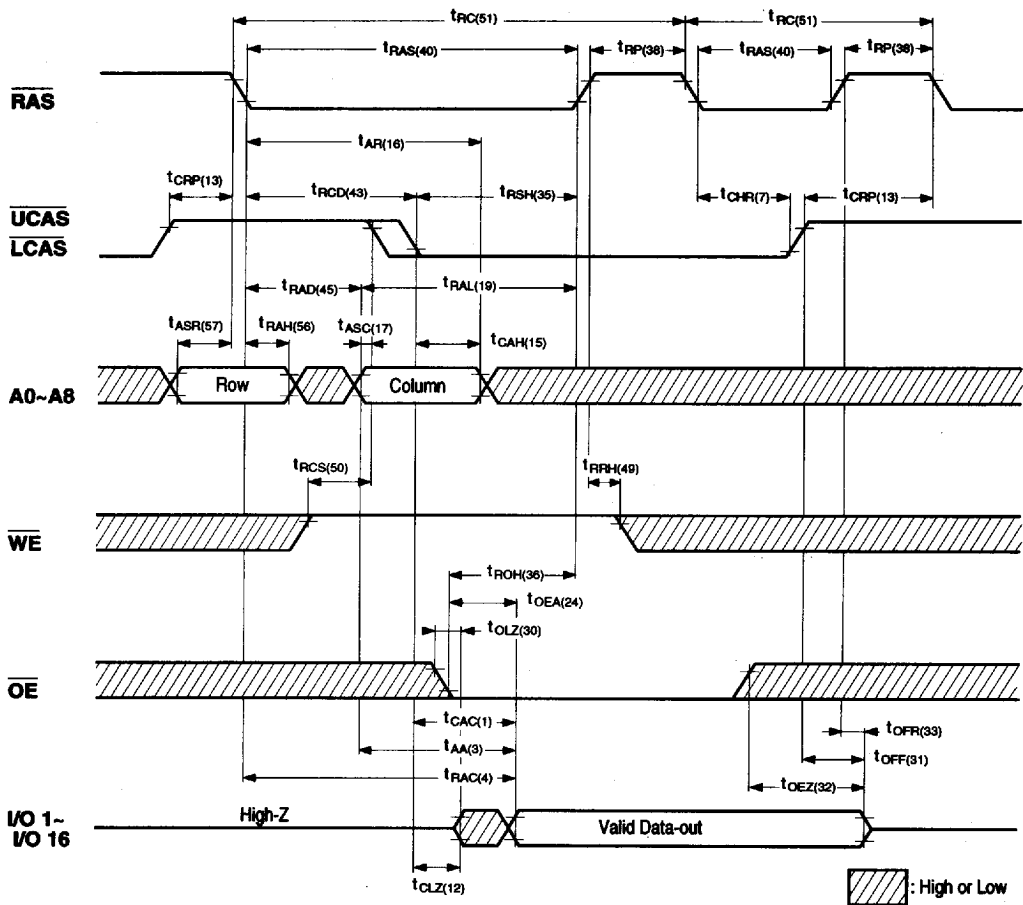


Note: $\overline{OE}$, A0~A8 = Don't care.

: High or Low

9005650 0001279 034

HIDDEN REFRESH CYCLE (WORD READ)

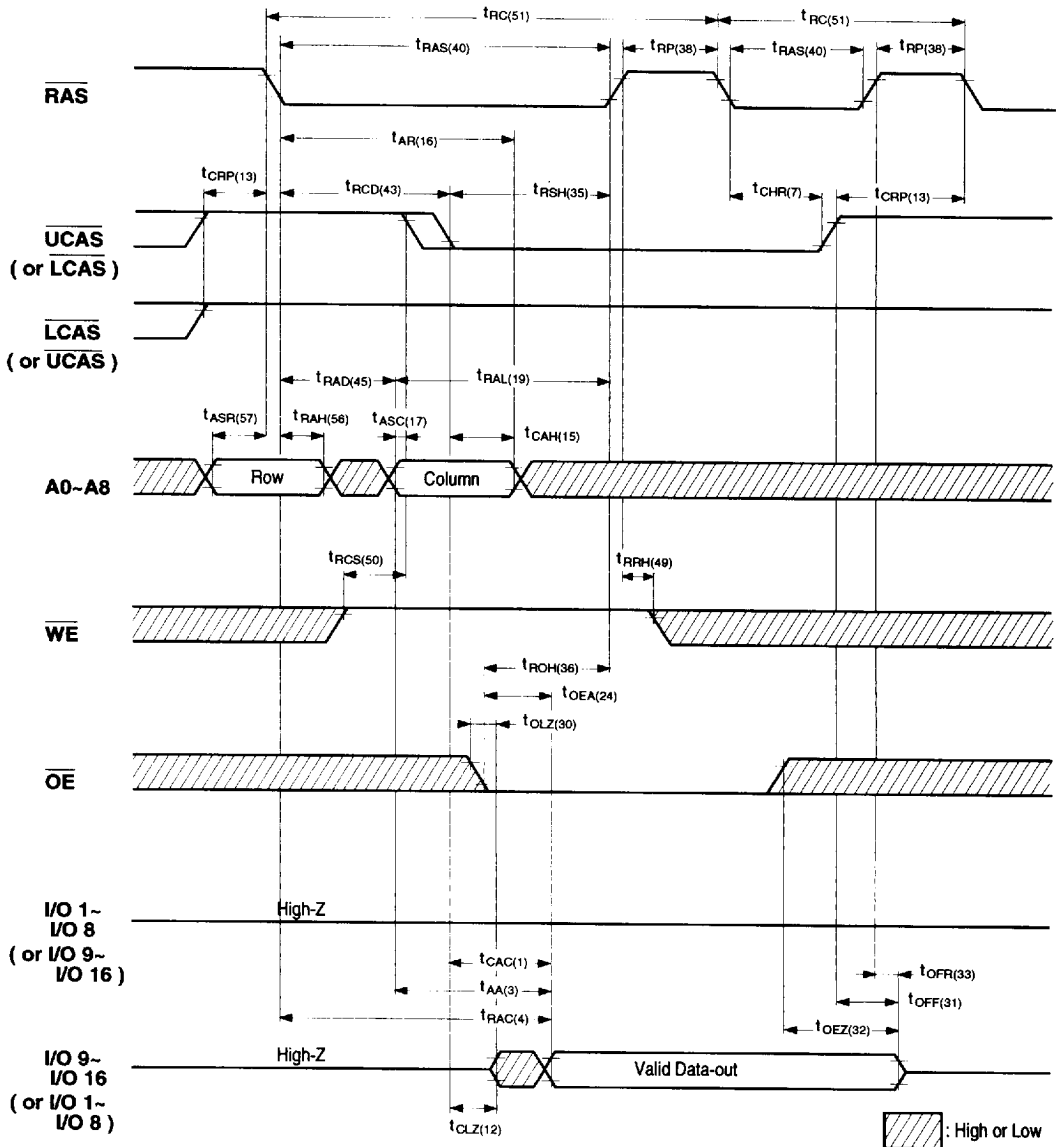


9005650 0001280 856

NPNX

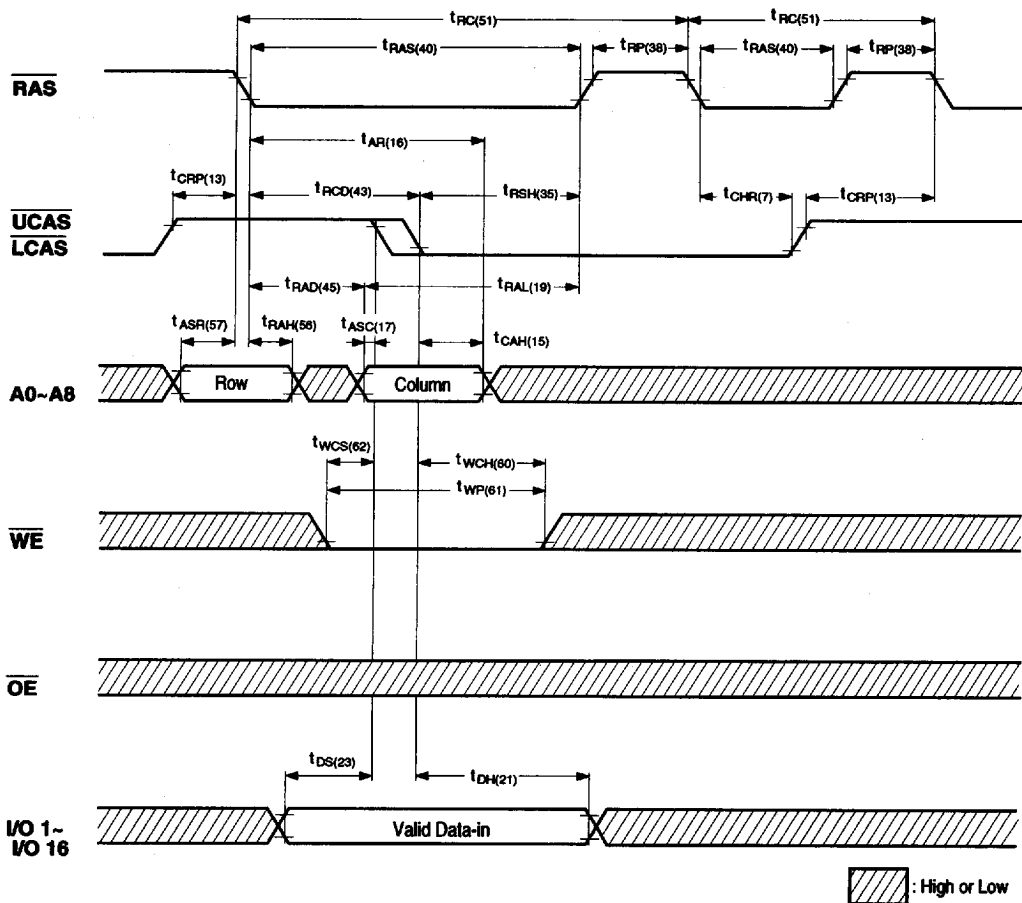
466

HIDDEN REFRESH CYCLE (BYTE READ)



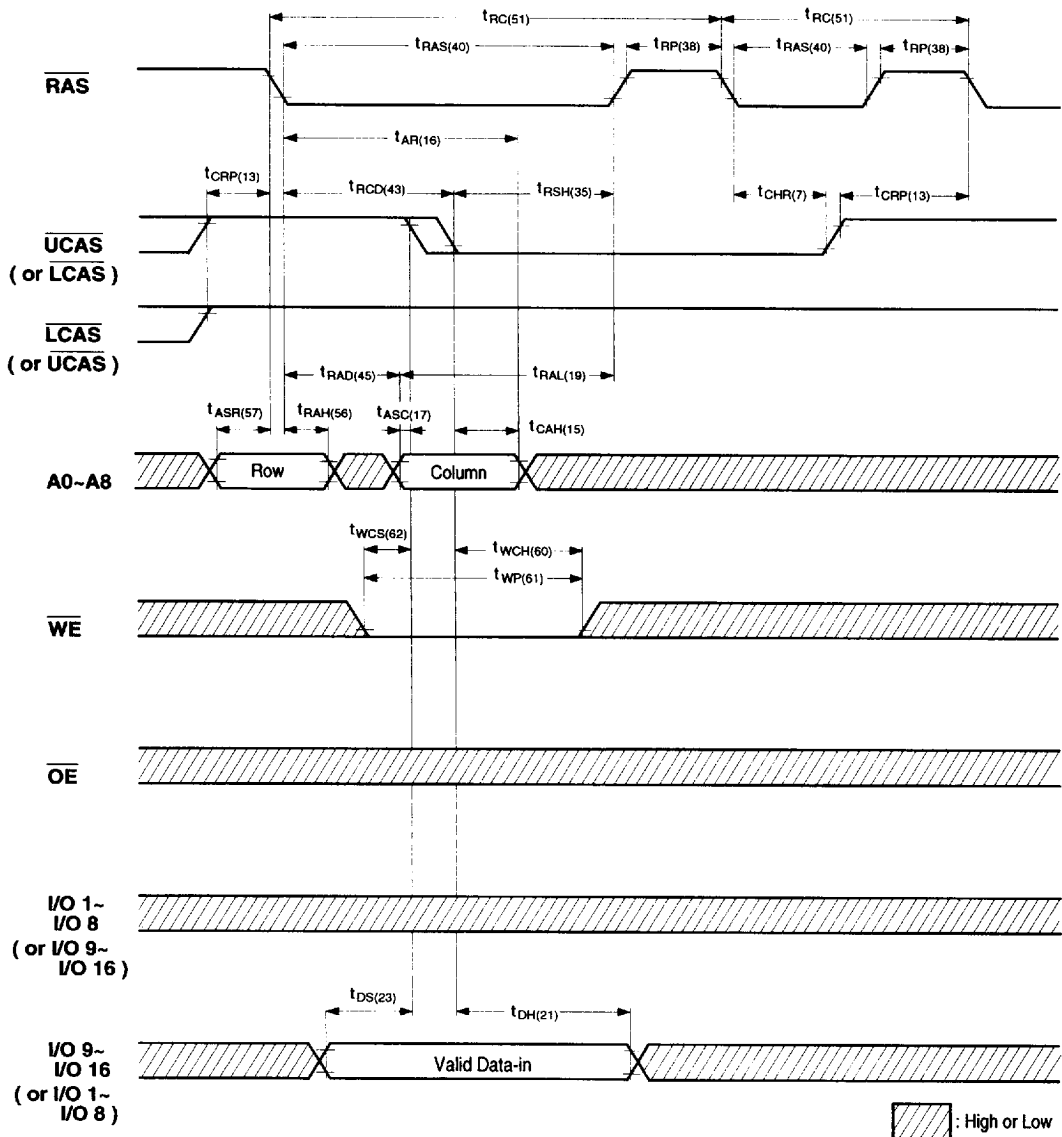
9005650 0001281 792

HIDDEN REFRESH CYCLE (EARLY WORD WRITE)



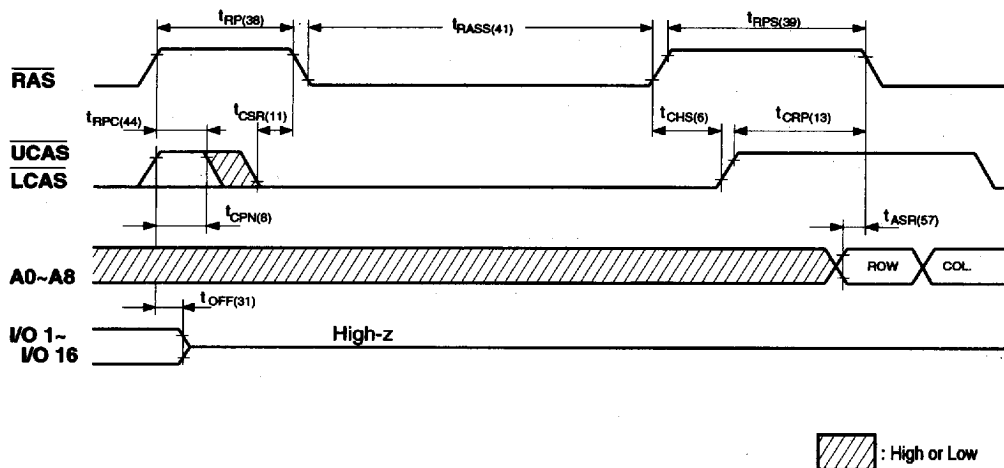
9005650 0001282 629

HIDDEN REFRESH CYCLE (EARLY BYTE WRITE)



9005650 0001283 565

SELF REFRESH MODE



■ The NN514265L/AL version has a Self Refresh Mode.

a. Entering the Self Refresh Mode:

The NN514265L/LA Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 300 μ s.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode. It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The NN514265L/LA exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

ORDERING INFORMATION

NN514265XX(X) - XX

	SPEED	45	:	45ns
		50	:	50ns
		60	:	60ns
		70	:	70ns
	PACKAGE	J	:	Plastic SOJ
		TT	:	Plastic TSOP TYPEII
	VERSION	BLANK	:	Standard Version
		L	:	Long Refresh Version 128ms Refresh
			:	
	MODE	4265	:	EDO (Hyper Page) 2CAS ,256K x 16 ,512refresh cycle

NN514265AXX(X) - XX

	SPEED	35	:	35ns
		40	:	40ns
		45	:	45ns
		50	:	50ns
		60	:	60ns
			:	
	PACKAGE	J	:	Plastic SOJ
		TT	:	Plastic TSOP TYPEII
	VERSION	BLANK	:	Standard Version
		L	:	Long Refresh Version 128ms Refresh
			:	
	DESIGN CODE	A	:	NN514260A
	MODE	4265	:	EDO (Hyper Page) 2CAS ,256K x 16 ,512refresh cycle

9005650 0001285 338