FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50111-1E

MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

8M (× 16) FLASH MEMORY & 2M (× 16) STATIC RAM

MB84VD2008-10/MB84VD2009-10

■ FEATURES

- **Power supply voltage of 2.7 to 3.6 V**
- **High performance**
  100 ns maximum access time
- **Operating Temperature**
  –20 to +85°C

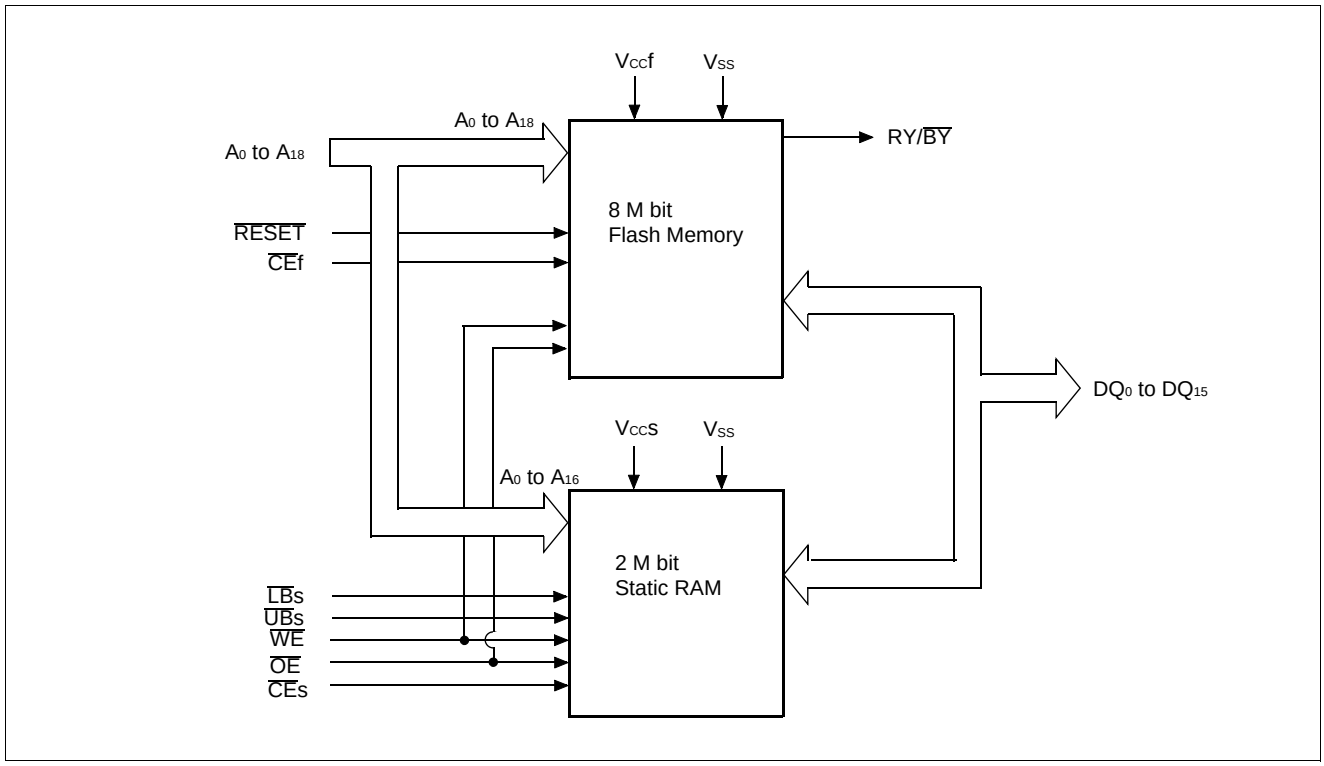
— FLASH MEMORY

- **Simultaneous operations Read-while Erase or Read-while-Program**
- **Minimum 100,000 write/erase cycles**
- **Sector erase architecture**
  Two 16 K byte, four 8 K bytes, two 32 K byte, and fourteen 64 K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VD2008: Top sector
  MB84VD2009: Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready-Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to "MBM29DL800TA/BA" data sheet in detailed function**

— SRAM

- **Power dissipation**
  Operating : 50 mA max.
  Standby : 50 µA max.
- **Data retention supply voltage: 2.0 V to 3.6 V**

■ BLOCK DIAGRAM



■ PIN ASSIGNMENTS

(Top View)

	A	B	C	D	E	F	G	H
6	$\overline{CE}$s	V_{SS}	DQ_1	A_1	A_2	A_4	N.C.	A_9
5	A_{10}	DQ_5	DQ_2	A_0	A_3	A_7	RY/$\overline{BY}$	A_{14}
4	$\overline{OE}$	DQ_7	DQ_4	DQ_0	A_6	A_{18}	$\overline{RESET}$	A_{15}
3	A_{11}	A_8	A_5	DQ_8	DQ_3	DQ_{12}	A_{12}	$\overline{LB}$s
2	A_{13}	A_{17}	$\overline{UB}$s	$\overline{CE}$f	DQ_{10}	V_{CC}f	DQ_6	DQ_{15}
1	$\overline{WE}$	V_{CC}s	A_{16}	V_{SS}	DQ_9	DQ_{11}	DQ_{13}	DQ_{14}

Table 1 Pin Configuration

Pin	Function	Input/ Output
A_0 to A_{16}	Address Inputs (Common)	I
A_{17} to A_{18}	Address Input (Flash)	I
DQ_0 to DQ_{15}	Data Inputs/Outputs (Common)	I/O
$\overline{CE}$f	Chip Enable (Flash)	I
$\overline{CE}$s	Chip Enable (SRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/$\overline{BY}$	Ready/Busy Outputs (Flash)	O
$\overline{UB}$s	Upper Byte Control (SRAM)	I
$\overline{LB}$s	Lower Byte Control (SRAM)	I
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}f	Device Power Supply (Flash)	Power
V_{CC}s	Device Power Supply (SRAM)	Power

■ PRODUCT LINE UP

		Flash Memory	SRAM
Ordering Part No.	V_{CC} = 3.0 V $^{+0.6\ V}_{-0.3\ V}$	MB84VD2008-10/MB84VD2009-10	
Max. Address Access Time (ns)		100	85
Max. $\overline{CE}$ Access Time (ns)		100	85
Max. $\overline{OE}$ Access Time (ns)		40	45

■ BUS OPERATIONS

Table 2 User Bus Operations

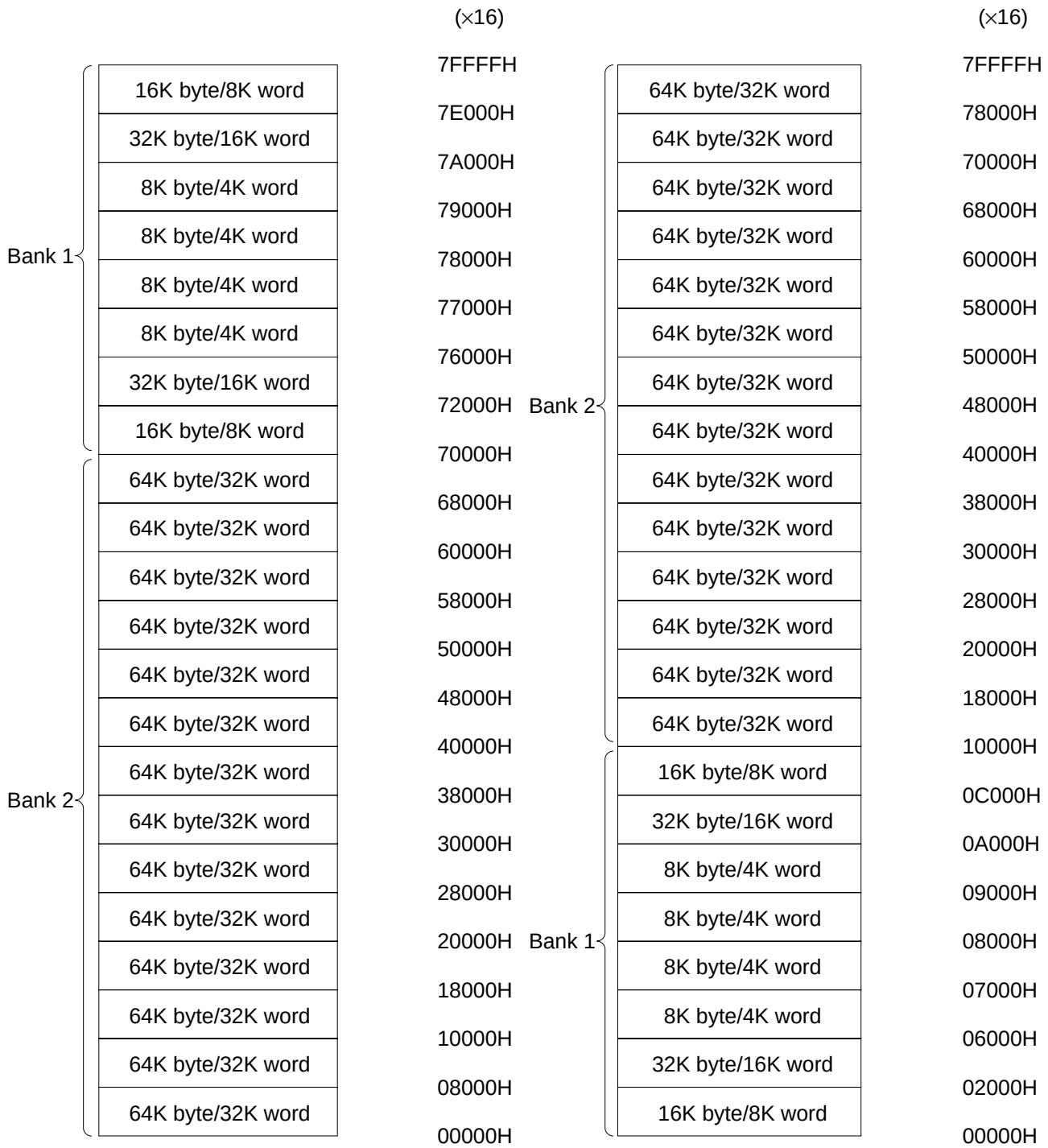
Operation (1), (3)	$\overline{CE}$f	$\overline{CE}$s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$s	$\overline{UB}$s	DQ_0 to DQ_7	DQ_8 to DQ_{15}	$\overline{RESET}$
Full Standby	H	H	X	X	X	X	HIGH-Z	HIGH-Z	H
Output Disable	H	L	H	H	X	X	HIGH-Z	HIGH-Z	H
			X	X	H	H	HIGH-Z	HIGH-Z	
	L	H	H	H	X	X	HIGH-Z	HIGH-Z	
Read from Flash (2)	L	H	L	H	X	X	D_{OUT}	D_{OUT}	H
Write to Flash	L	H	H	L	X	X	D_{IN}	D_{IN}	H
Read from SRAM	H	L	L	H	L	L	D_{OUT}	D_{OUT}	H
					H	L	HIGH-Z	D_{OUT}	
					L	H	D_{OUT}	HIGH-Z	
Write to SRAM	H	L	X	L	L	L	D_{IN}	D_{IN}	H
					H	L	HIGH-Z	D_{IN}	
					L	H	D_{IN}	HIGH-Z	
Flash Hardware Reset	X	H	X	X	X	X	HIGH-Z	HIGH-Z	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes: 1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE}$s = V_{IL} at a time.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Two 16 K byte, four 8 K bytes, two 32 K byte, and fourteen 64 K bytes.
- Individual-sector, multiple-sector, or bulk-erase capability.



MB84VD2008 Sector Architecture **MB84VD2009 Sector Architecture**

Table 4 Sector Address Tables (MB84DV2008)

Bank	Sector	Sector Address							Sector Size (Kbytes/ Kwords)	(×16) Address Range
		Bank Address								
		A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 2	SA0	0	0	0	0	X	X	X	64/32	00000H to 07FFFH
	SA1	0	0	0	1	X	X	X	64/32	08000H to 0FFFFH
	SA2	0	0	1	0	X	X	X	64/32	10000H to 17FFFH
	SA3	0	0	1	1	X	X	X	64/32	18000H to 1FFFFH
	SA4	0	1	0	0	X	X	X	64/32	20000H to 27FFFH
	SA5	0	1	0	1	X	X	X	64/32	28000H to 2FFFFH
	SA6	0	1	1	0	X	X	X	64/32	30000H to 37FFFH
	SA7	0	1	1	1	X	X	X	64/32	38000H to 3FFFFH
	SA8	1	0	0	0	X	X	X	64/32	40000H to 47FFFH
	SA9	1	0	0	1	X	X	X	64/32	48000H to 4FFFFH
	SA10	1	0	1	0	X	X	X	64/32	50000H to 57FFFH
	SA11	1	0	1	1	X	X	X	64/32	58000H to 5FFFFH
	SA12	1	1	0	0	X	X	X	64/32	60000H to 67FFFH
	SA13	1	1	0	1	X	X	X	64/32	68000H to 6FFFFH
Bank 1	SA14	1	1	1	0	0	0	X	16/8	70000H to 71FFFH
	SA15	1	1	1	0	0	1	X	32/16	72000H to 73FFFH, 74000H to 75FFFH
						1	0	X		
	SA16	1	1	1	0	1	1	0	8/4	76000H to 76FFFH
	SA17	1	1	1	0	1	1	1	8/4	77000H to 77FFFH
	SA18	1	1	1	1	0	0	0	8/4	78000H to 78FFFH
	SA19	1	1	1	1	0	0	1	8/4	79000H to 79FFFH
	SA20	1	1	1	1	0	1	X	32/16	7A000H to 7BFFFH, 7C000H to 7DFFFH
						1	0	X		
	SA21	1	1	1	1	1	1	X	16/8	7E000H to 7FFFFH

Table 5 Sector Address Tables (MB84DV2009)

Bank	Sector	Sector Address							Sector Size (Kbytes/ Kwords)	(×16) Address Range
		Bank Address								
		A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 2	SA21	1	1	1	1	X	X	X	64/32	78000H to 7FFFFH
	SA20	1	1	1	0	X	X	X	64/32	70000H to 77FFFH
	SA19	1	1	0	1	X	X	X	64/32	68000H to 6FFFFH
	SA18	1	1	0	0	X	X	X	64/32	60000H to 67FFFH
	SA17	1	0	1	1	X	X	X	64/32	58000H to 5FFFFH
	SA16	1	0	1	0	X	X	X	64/32	50000H to 57FFFH
	SA15	1	0	0	1	X	X	X	64/32	48000H to 4FFFFH
	SA14	1	0	0	0	X	X	X	64/32	40000H to 47FFFH
	SA13	0	1	1	1	X	X	X	64/32	38000H to 3FFFFH
	SA12	0	1	1	0	X	X	X	64/32	30000H to 37FFFH
	SA11	0	1	0	1	X	X	X	64/32	28000H to 2FFFFH
	SA10	0	1	0	0	X	X	X	64/32	20000H to 27FFFH
	SA9	0	0	1	1	X	X	X	64/32	18000H to 1FFFFH
	SA8	0	0	1	0	X	X	X	64/32	10000H to 17FFFH
Bank 1	SA7	0	0	0	1	1	1	X	16/8	0E000H to 0FFFFH
	SA6	0	0	0	1	1	0	X	32/16	0A000H to 0BFFFH, 0C000H to 0DFFFH
						0	1	X		
	SA5	0	0	0	1	0	0	1	8/4	09000H to 09FFFH
	SA4	0	0	0	1	0	0	0	8/4	08000H to 08FFFH
	SA3	0	0	0	0	1	1	1	8/4	07000H to 07FFFH
	SA2	0	0	0	0	1	1	0	8/4	06000H to 06FFFH
	SA1	0	0	0	0	1	0	X	32/16	04000H to 05FFFH, 02000H to 03FFFH
						0	1	X		
	SA0	0	0	0	0	0	0	X	16/8	00000H to 01FFFH

Table 6. 1 Flash Memory Autoselect Codes

Type		A_6	A_1	A_0	Code (HEX)
Manufacturer's Code		V_{IL}	V_{IL}	V_{IL}	04H
Device Code	MB84VD2008	V_{IL}	V_{IL}	V_{IH}	224AH
	MB84VD2009	V_{IL}	V_{IL}	V_{IH}	22CBH

Table 6. 2 Expanded Autoselect Code Table

Type		Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code		0004H	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MB84VD2008	224AH	0	0	1	0	0	0	1	0	0	1	0	0	1	0	1	0
	MB84VD2009	22CBH	0	0	1	0	0	0	1	0	1	1	0	0	1	0	1	1

Table 7 Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
Autoselect	3	555H	AAH	2AAH	55H	(BA) 555H	90H	—	—	—	—	—	—
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Erase Suspend	1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
Fast Program *	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode *	2	BA	90H	XXXH	F0H	—	—	—	—	—	—	—	—
Extended Sector Protect	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—

Notes: 1. Address bits A_{11} to A_{18} = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA).

2. Bus operations are defined in Tables 2 and 3.
3. RA = Address of the memory location to be read
   PA = Address of the memory location to be programmed
   Addresses are latched on the falling edge of the write pulse.
   SA = Address of the sector to be erased. The combination of A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
   BA = Bank Address (A_{16} to A_{18})
4. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.
5. SPA =Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0).
   SD = Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

* : This command is valid while Fast Mode.

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +125°C
Ambient Temperature with Power Applied ..... –25°C to +85°C
Voltage with Respect to Ground All pins (Note) ..... –0.3 V to $V_{CC}f$ +0.5 V
–0.3 V to $V_{CC}s$ +0.5 V
$V_{CC}f$/$V_{CC}s$ Supply (Note) ..... –0.3 V to +4.6 V

Note: Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negativeovershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{CC}f$ +0.5 V or $V_{CC}s$ +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Commercial Devices
Ambient Temperature (T_A) ..... –20°C to +85°C

$V_{CC}f$/$V_{CC}s$ Supply Voltages ..... +2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	—			–1.0	—	+1.0	µA
I_{LO}	Output Leakage Current	—			–1.0	—	+1.0	µA
$I_{CC1}f$	Flash V_{CC} Active Current (Read)	$V_{CC}f$ = V_{CC} Max., $\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}		t_{CYCLE} = 10 MHz	—	—	20	mA
				t_{CYCLE} = 5 MHz	—	—	10	
$I_{CC2}f$	Flash V_{CC} Active Current (Program/Erase)	$V_{CC}f$ = V_{CC} Max., $\overline{CE}f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
$I_{CC3}f$**	Flash V_{CC} Active Current (Read-While-Program)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	45	mA
$I_{CC4}f$**	Flash V_{CC} Active Current (Read-While-Erase)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	45	mA
$I_{CC5}f$	Flash V_{CC} Active Current (Erase-Suspend-Program)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
$I_{CC1}s$	SRAM V_{CC} Active Current	$V_{CC}s$ = V_{CC} Max., $\overline{CE}s$ = V_{IL}		t_{CYCLE} = min	—	—	60	mA
				t_{CYCLE} = 1 MHz	—	—	12	mA
$I_{CC2}s$	SRAM V_{CC} Active Current	$\overline{CE}s$ = 0.2 V, $\overline{WE}$ = $V_{CC}s$ – 0.2 V		t_{CYCLE} = min	—	—	50	mA
				t_{CYCLE} = 1 MHz	—	—	6	mA
$I_{SB1}f$	Flash V_{CC} Standby Current	$V_{CC}f$ = V_{CC} Max., $\overline{CE}f$ = $V_{CC}f$ ± 0.3 V, $\overline{RESET}$ = $V_{CC}f$ ± 0.3 V			—	—	5	µA
$I_{SB2}f$	Flash V_{CC} Standby Current ($\overline{RESET}$)	$V_{CC}f$ = V_{CC} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V			—	—	5	µA
$I_{SB1}s$	SRAM V_{CC} Standby Current	$\overline{CE}s$ = V_{IH}			—	—	2	mA
$I_{SB2}s$	SRAM V_{CC} Standby Current	$\overline{CE}s$ = V_{CC} –0.2 V	$V_{CC}s$ = 3.0 V ±10%	T_A = 25°C	—	1	2.5	µA
				T_A = –20 to +85°C	—	—	55	µA
			$V_{CC}s$ = 3.3 V ±0.3 V	T_A = 25°C	—	1.5	3	µA
				T_A = –20 to +85°C	—	—	60	µA
			$V_{CC}s$ = 3.0 V	T_A = 25°C	—	1	2	µA
				T_A = –20 to +40°C	—	—	5	µA
				T_A = –20 to +85°C	—	—	50	µA
V_{IL}	Input Low Level	—			–0.3	—	0.6	V
V_{IH}	Input High Level	—			2.2	—	V_{CC}+0.3*	V
V_{OL}	Output Low Voltage Level	I_{OL} = 2.1 mA, $V_{CC}f$ = $V_{CC}s$ = V_{CC} Min.			—	—	0.4	V
V_{OH}	Output High Voltage Level	I_{OH} = –500 µA, $V_{CC}f$ = $V_{CC}s$ = V_{CC} Min.			V_{CC} – 0.5	—	—	V
V_{LKO}	Flash Low V_{CC} Lock-Out Voltage	—			2.3	—	2.5	V

* : V_{CC} indicate lower of $V_{CC}f$ or $V_{CC}s$

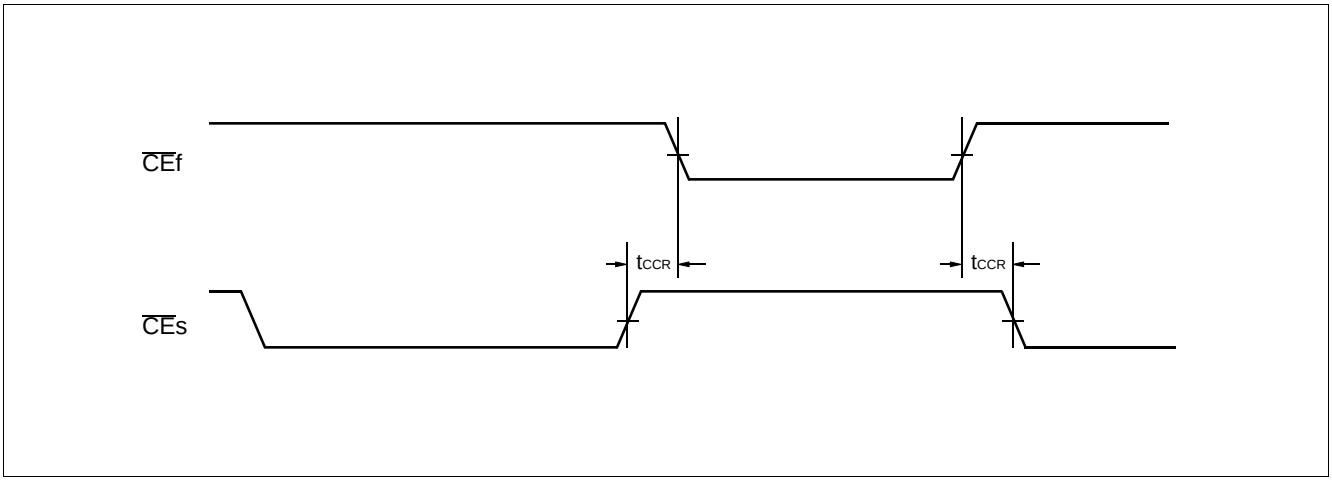
** :Embedded Algorithm (program or erase) is in progress. (@5 MHz)

■ AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

Parameter Symbols		Description	Test Setup		-10	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{CE}$ Recover Time	—	Min.	0	ns

- **Timing Diagram for alternating SRAM to Flash**

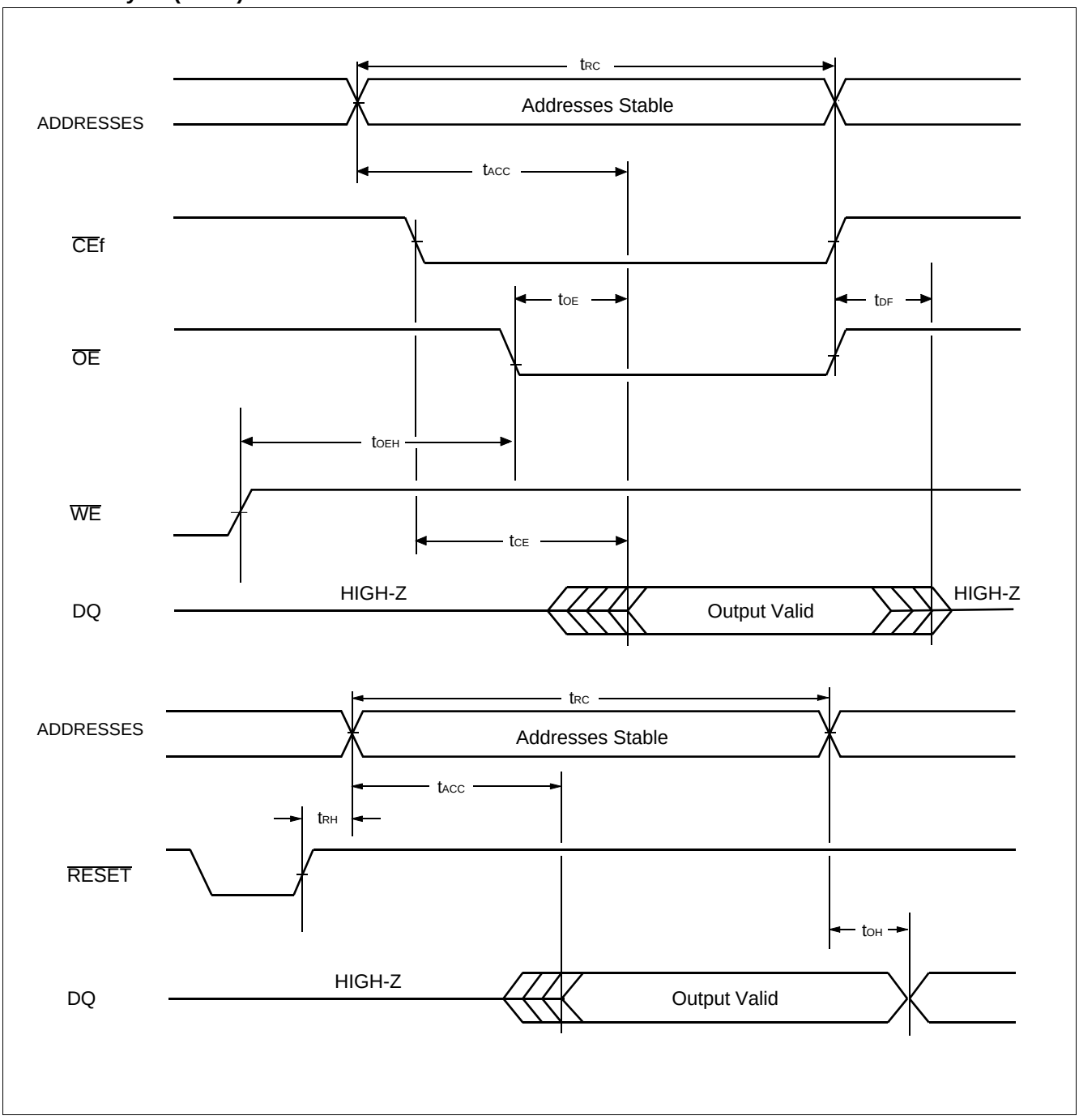


- **Read Only Operations Characteristics (Flash)**

Parameter Symbols		Description	Test Setup	-10 (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	100	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	100	ns
t_{ELQV}	$t_{CE}f$	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	—	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	—	5	ns

Note: Test Conditions–Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

- **Read Cycle (Flash)**



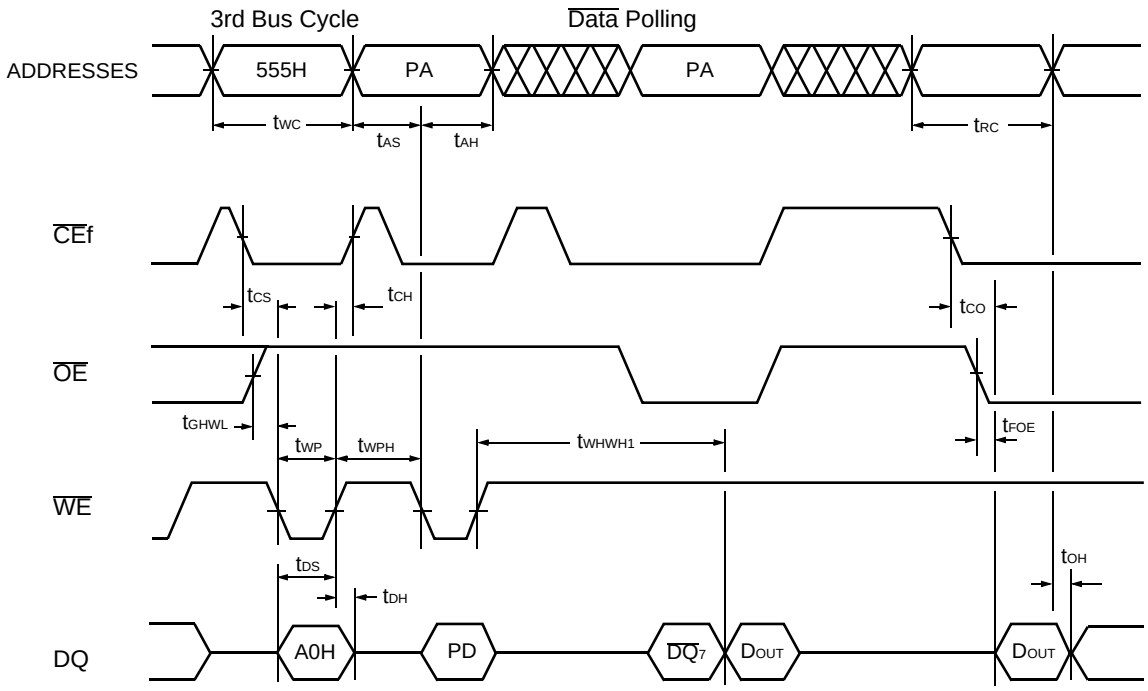
• **Erase/Program Operations (Flash)**

Parameter Symbols		Description		-10			Unit
JEDEC	Standard			Min.	Typ.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time		100	—	—	ns
t_{AVWL}	t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)		0	—	—	ns
t_{AVEL}	t_{AS}	Address Setup Time ($\overline{CE}$f to Addr.)		0	—	—	ns
—	t_{ASO}	Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		15	—	—	ns
t_{WLAX}	t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)		50	—	—	ns
t_{ELAX}	t_{AH}	Address Hold Time ($\overline{CE}$f to Addr.)		50	—	—	ns
—	t_{AHT}	Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		0	—	—	ns
t_{DVWH}	t_{DS}	Data Setup Time		50	—	—	ns
t_{WHDX}	t_{DH}	Data Hold Time		0	—	—	ns
—	t_{OEH}	Output Enable Hold Time	Read	0	—	—	ns
			Toggle and $\overline{Data}$ Polling	10	—	—	ns
—	t_{CEPH}	$\overline{CE}$ High During Toggle Bit Polling		20	—	—	ns
—	t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling		20	—	—	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)		0	—	—	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)		0	—	—	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{ELWL}	t_{CS}	$\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{WHEH}	t_{CH}	$\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		50	—	—	ns
t_{ELEH}	t_{CP}	$\overline{CE}$f Pulse Width		50	—	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		30	—	—	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$f Pulse Width High		30	—	—	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		—	8	—	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		—	1	—	sec
				—	—	15	sec
—	t_{VCS}	V_{CC}f Setup Time		50	—	—	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)		4	—	—	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		500	—	—	ns
—	t_{RB}	Recover Time from RY/$\overline{BY}$		0	—	—	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		500	—	—	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		200	—	—	ns
—	t_{EOE}	Delay Time from Embedded Output Enable		—	—	100	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		—	—	90	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z		—	—	30	ns
—	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Active		30	—	—	ns

Note : 1. This does not include the preprogramming time.

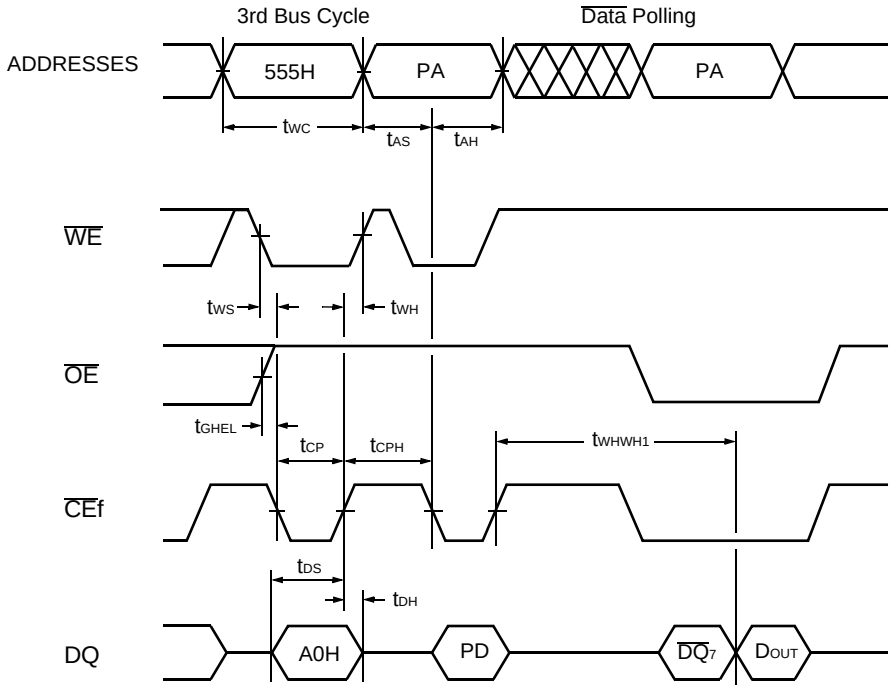
2. This timing is for Sector Protection Operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**



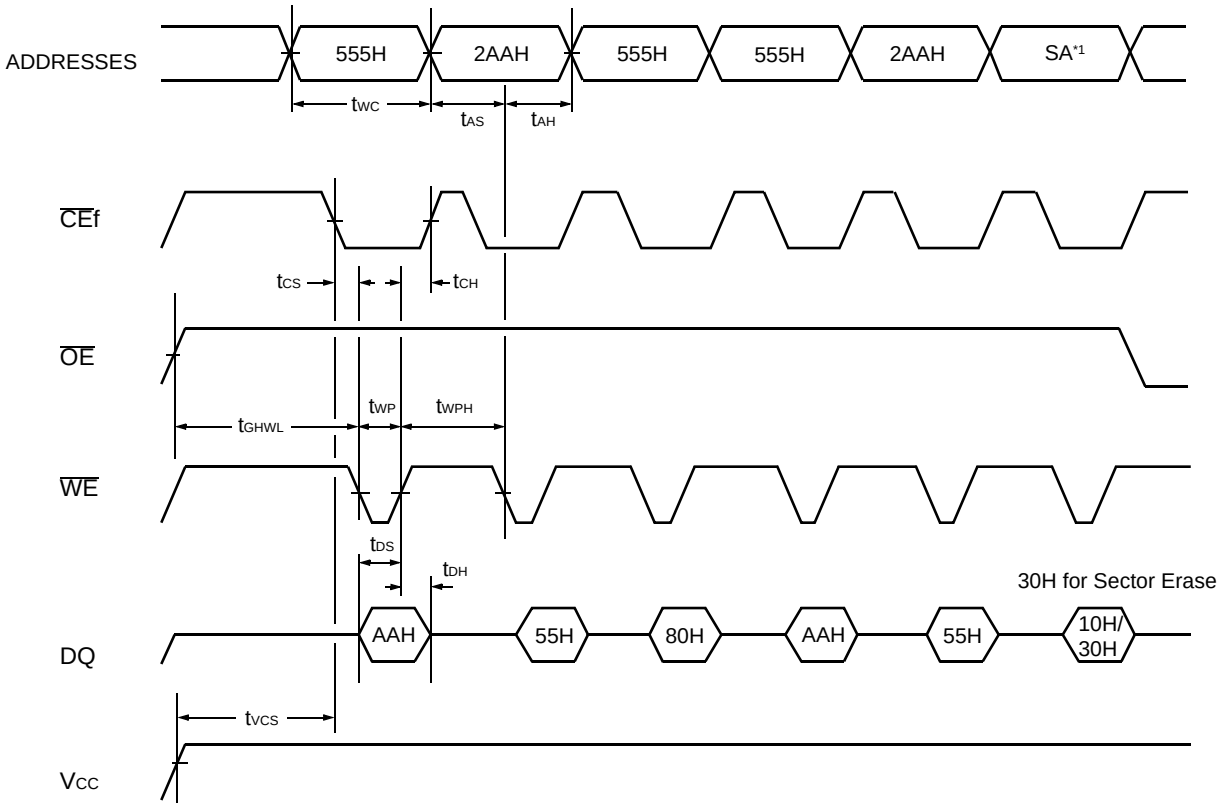
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence
6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

- **Write Cycle ($\overline{CE}$f control) (Flash)**



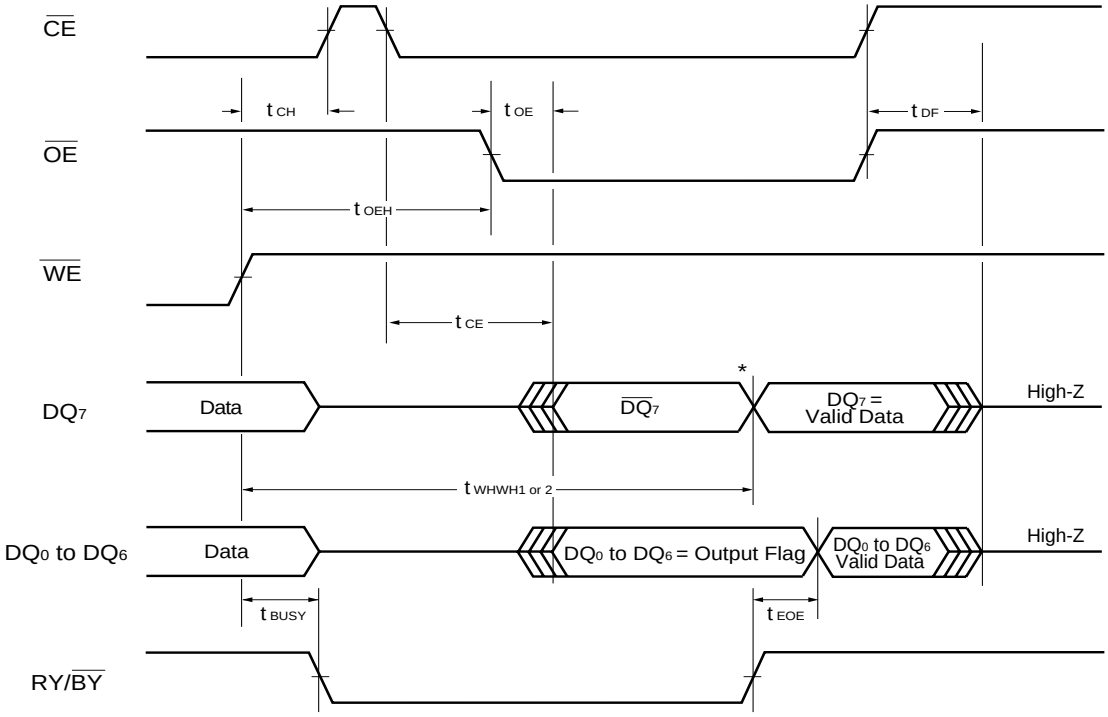
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence
6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



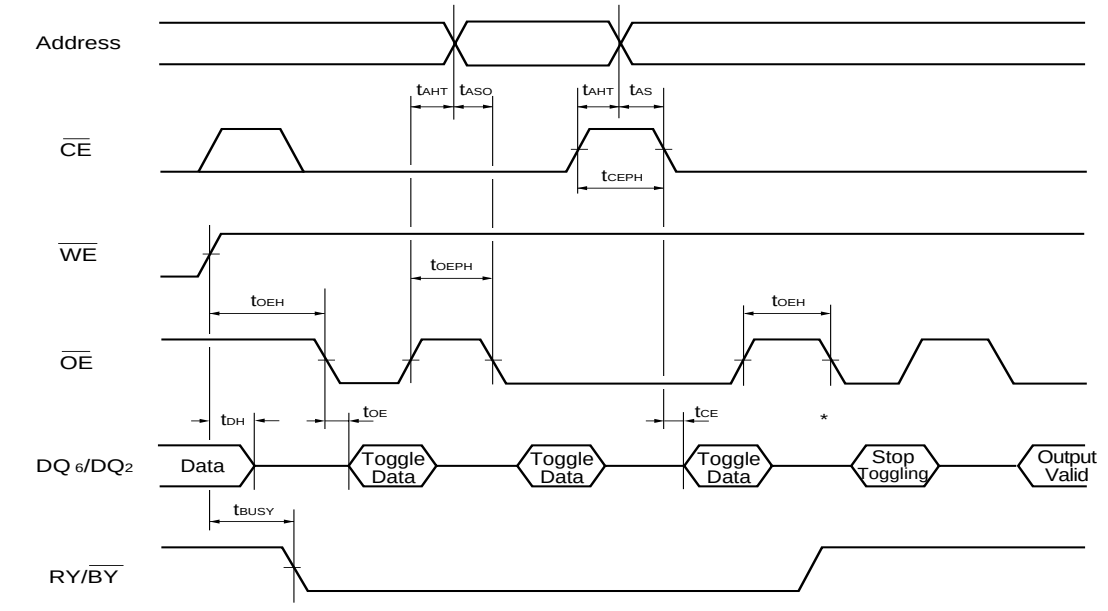
Notes: 1. SA is the sector address for Sector Erase. Addresses = 555H for Chip Erase.
2. These waveforms are for the x16 mode. The addresses differ from x8 mode.

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



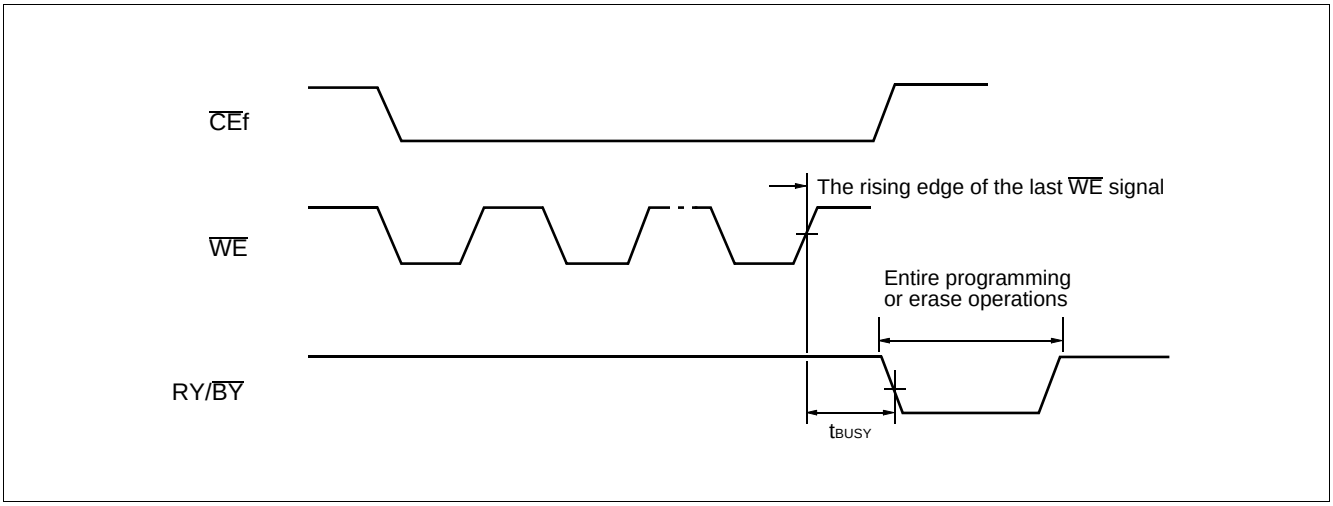
* : DQ_7 = Valid Data (The device has completed the Embedded operation).

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**

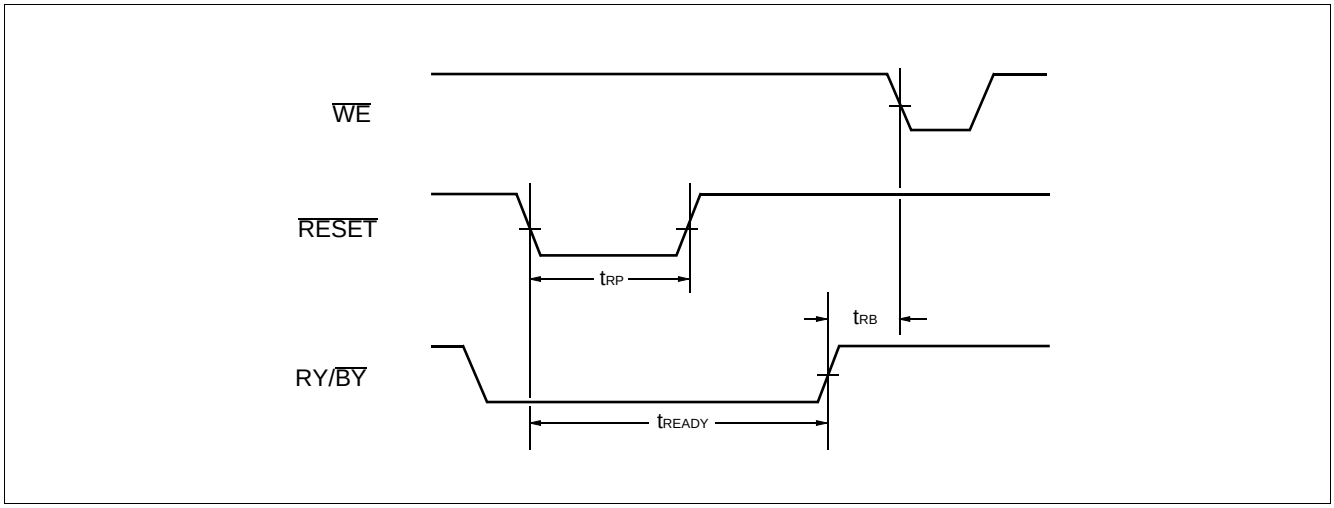


* : DQ_6 stops toggling (The device has completed the Embedded operation).

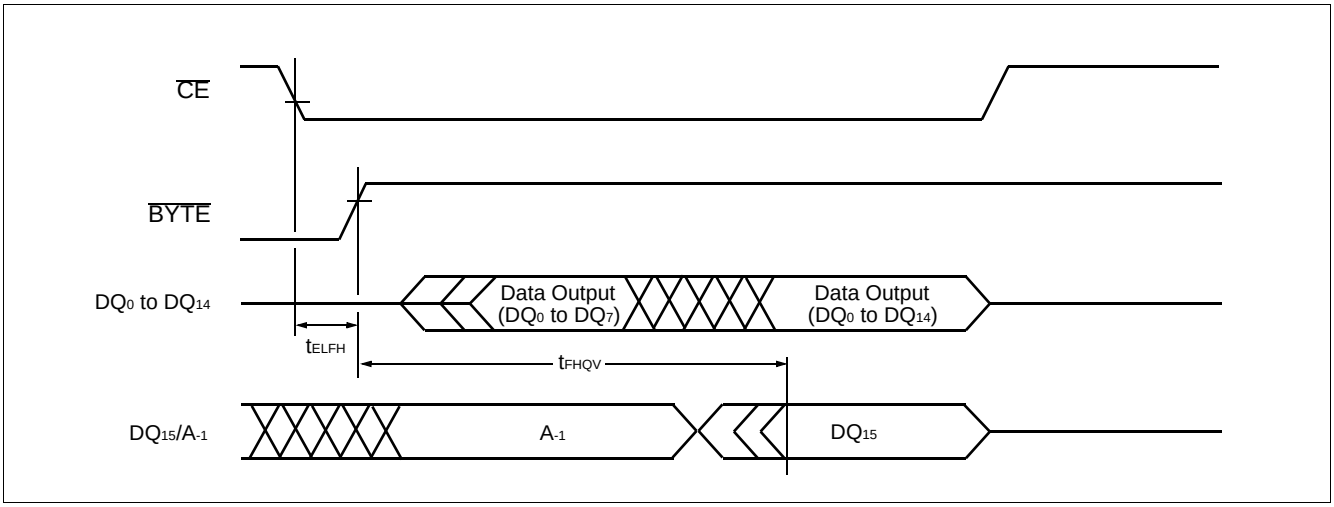
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



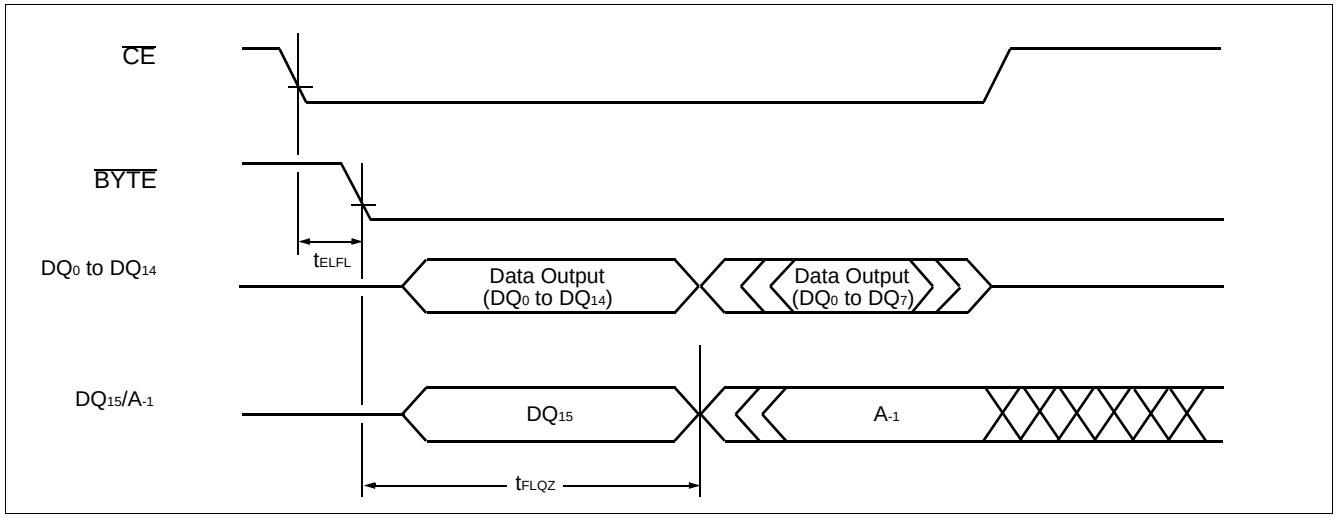
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



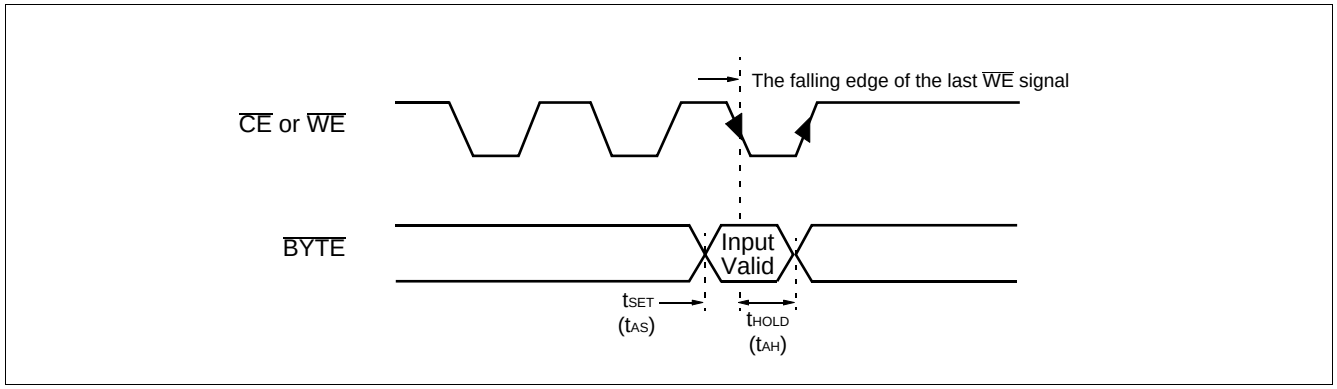
- **Timing Diagram for Word Mode Configuration (Flash)**



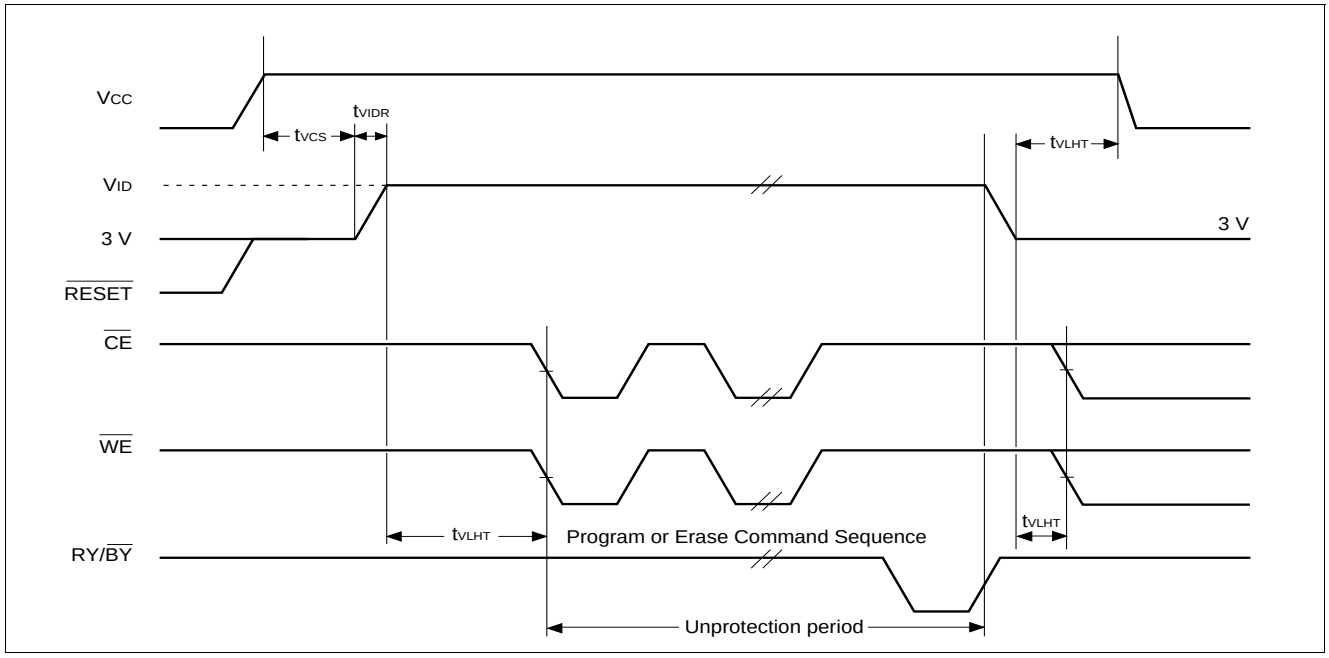
- **Timing Diagram for Byte Mode Configuration (Flash)**



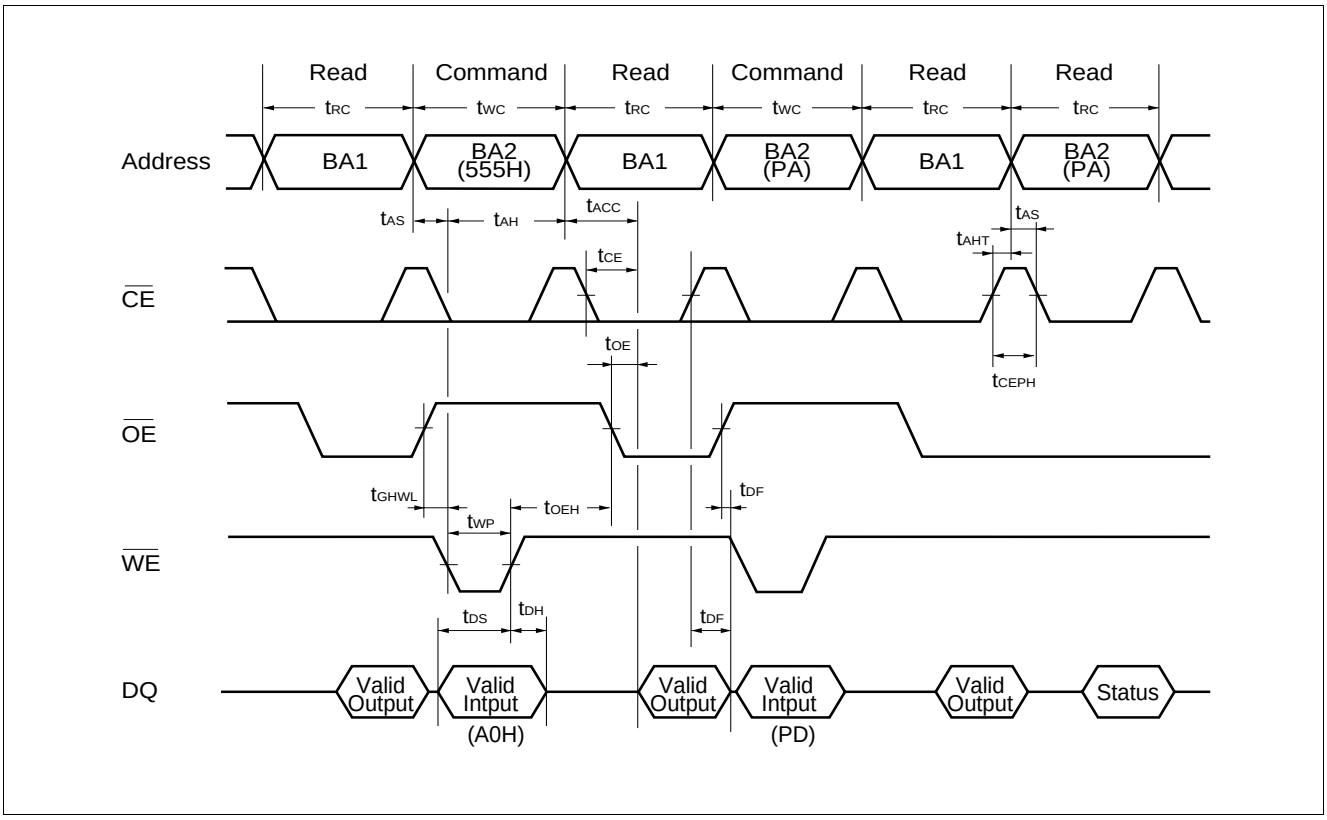
- **BYTE Timing Diagram for Write Operations (Flash)**



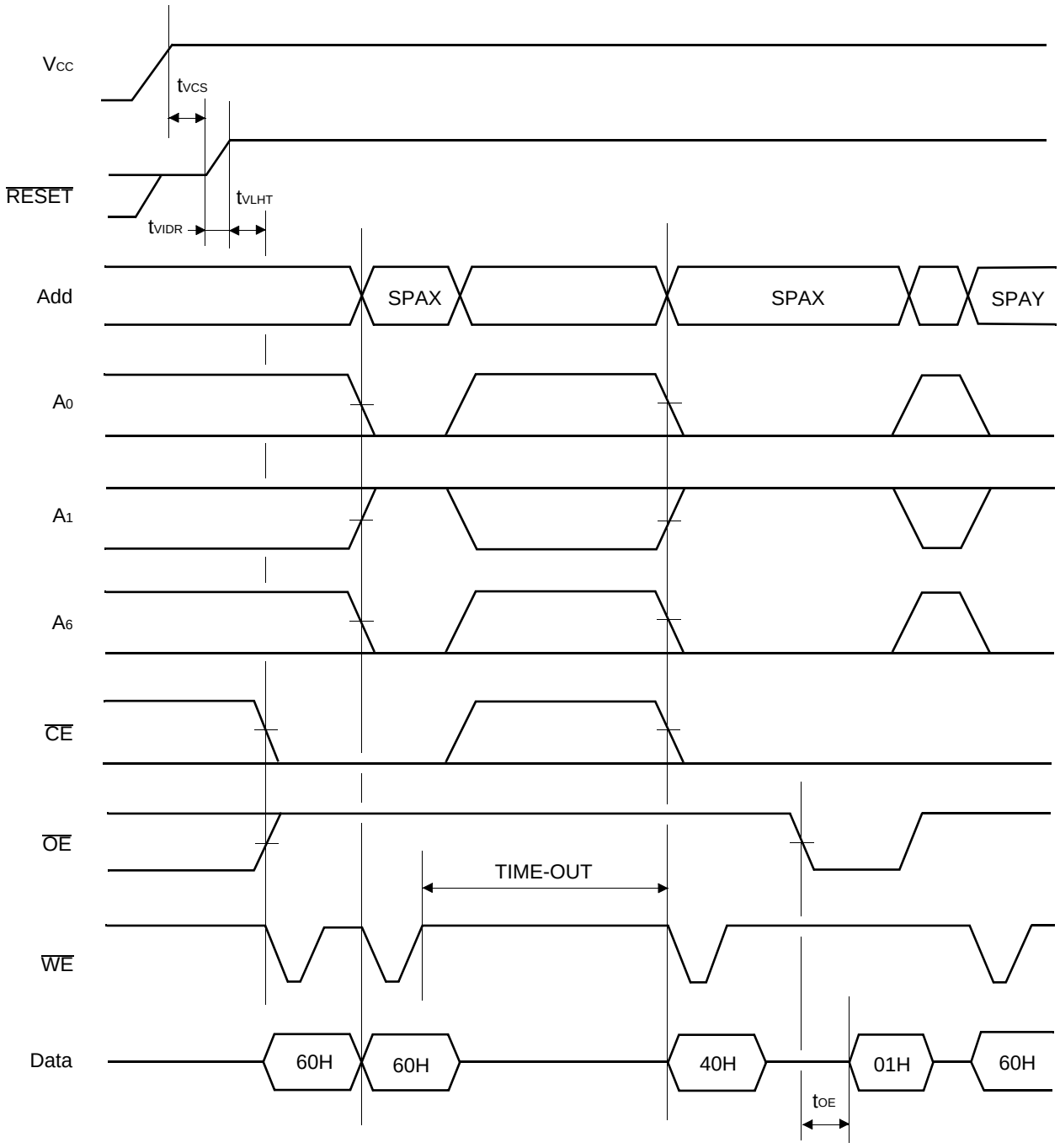
- **Temporary Sector Unprotection (Flash)**



- **Back-to-back Read/Write Timing Diagram**



- **Extended Sector Protection (Flash)**

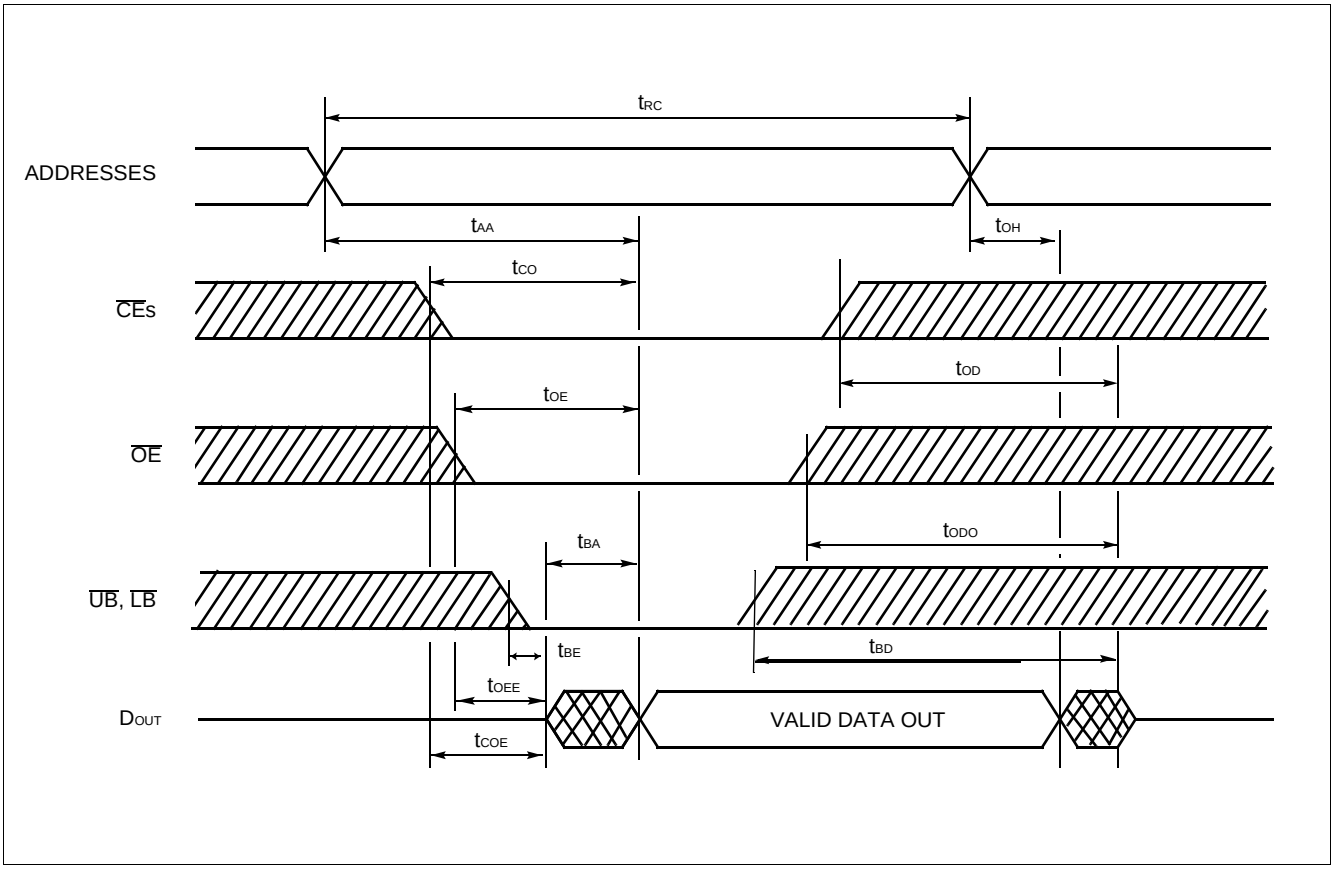


SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 150 µs (min)

- **Read Cycle (SRAM)**

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{RC}	Read Cycle Time	85	—	ns
t_{AA}	Address Access Time	—	85	ns
t_{CO}	Chip Enable ($\overline{CE}$s) Access Time	—	85	ns
t_{OE}	Output Enable Access Time	—	45	ns
t_{BA}	$\overline{UB}$, $\overline{LB}$ Access Time	—	45	ns
t_{COE}	Chip Enable Low to Output Active	5	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{BE}	$\overline{UB}$, $\overline{LB}$ Low to Output Active	0	—	ns
t_{OD}	Chip Enable High to Output High-Z	—	35	ns
t_{ODO}	Output Enable High to Output High-Z	—	35	ns
t_{BD}	$\overline{UB}$, $\overline{LB}$ High to Output High-Z	—	35	ns
t_{OH}	Output Data Hold Time	10	—	ns

- **Read Cycle (Note 1) (SRAM)**

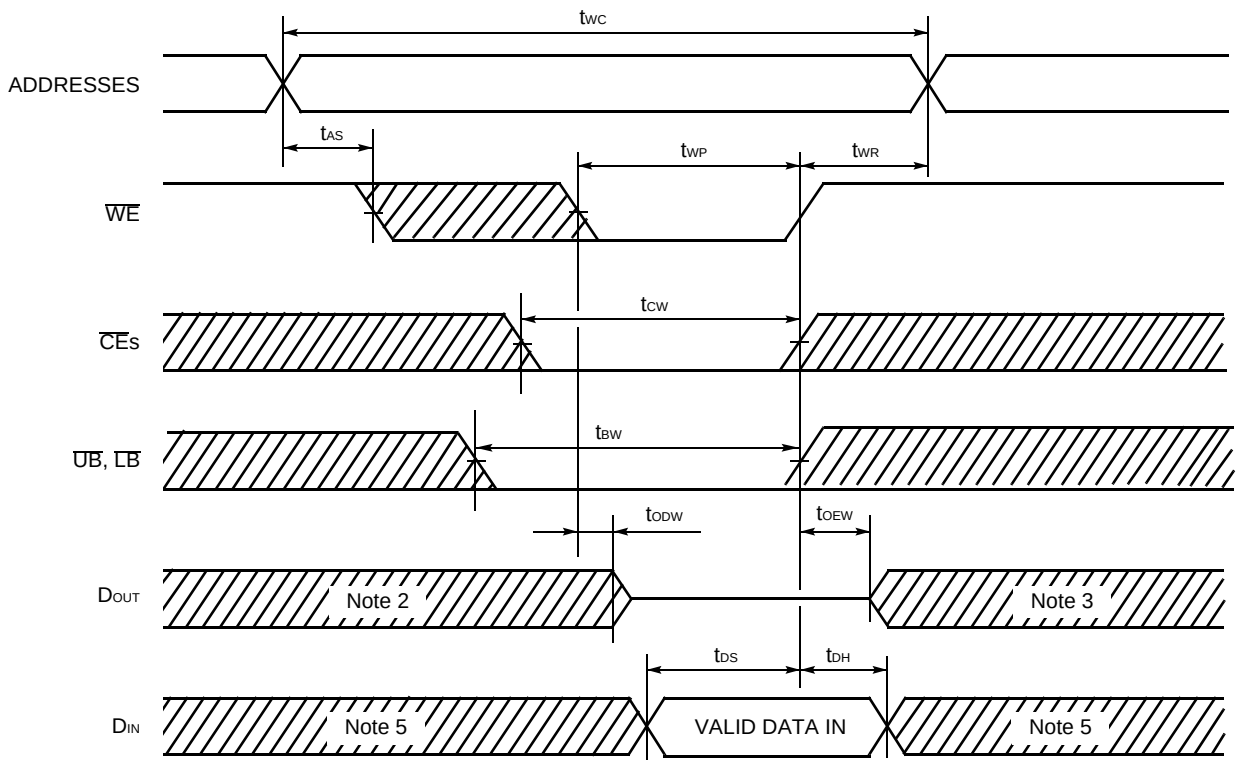


Note: 1. $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{WC}	Write Cycle Time	85	—	ns
t_{WP}	Write Pulse Width	60	—	ns
t_{CW}	Chip Enable to End of Write	75	—	ns
t_{BW}	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	55	—	ns
t_{AS}	Address Setup Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	—	35	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	—	ns
t_{DS}	Data Setup Time	35	—	ns
t_{DH}	Data Hold Time	0	—	ns

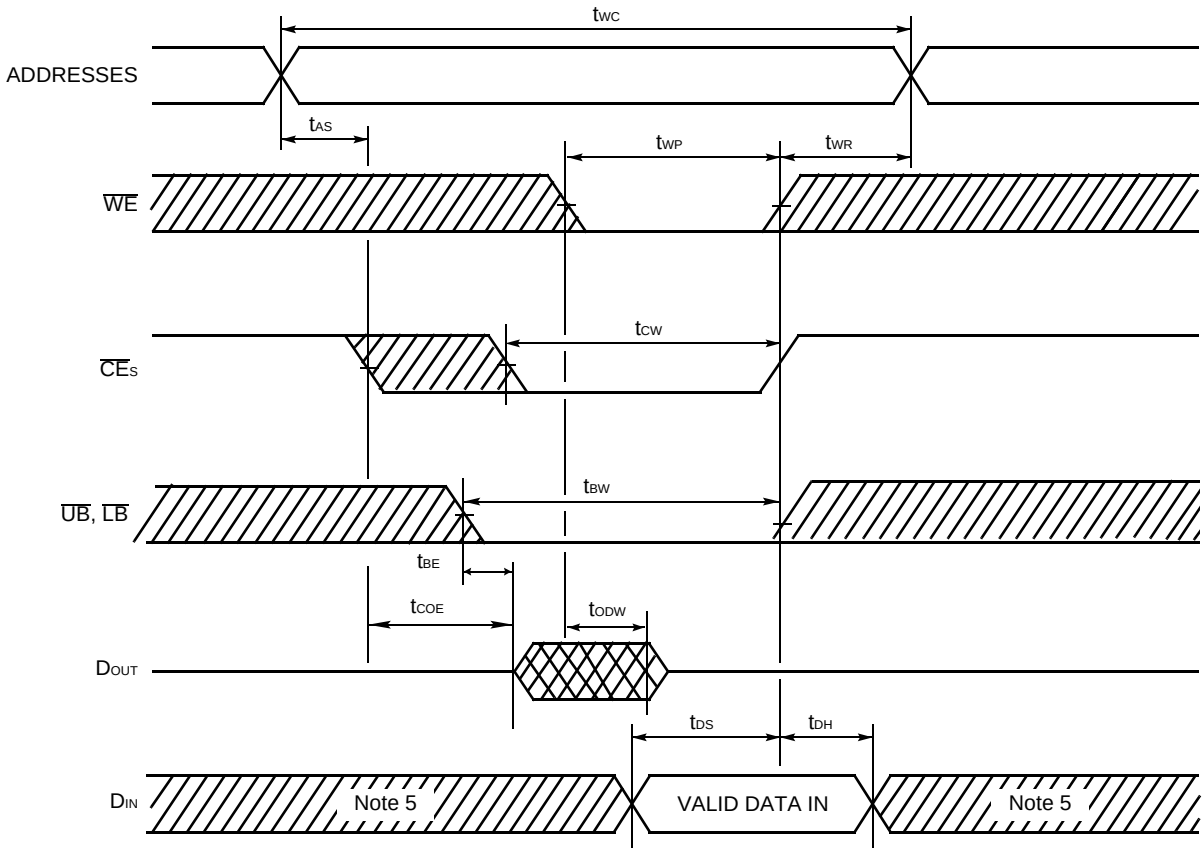
- **Write Cycle (Note 4) ($\overline{WE}$ control) (SRAM)**



Notes: 2. If $\overline{CE}$s goes LOW coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE}$s goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

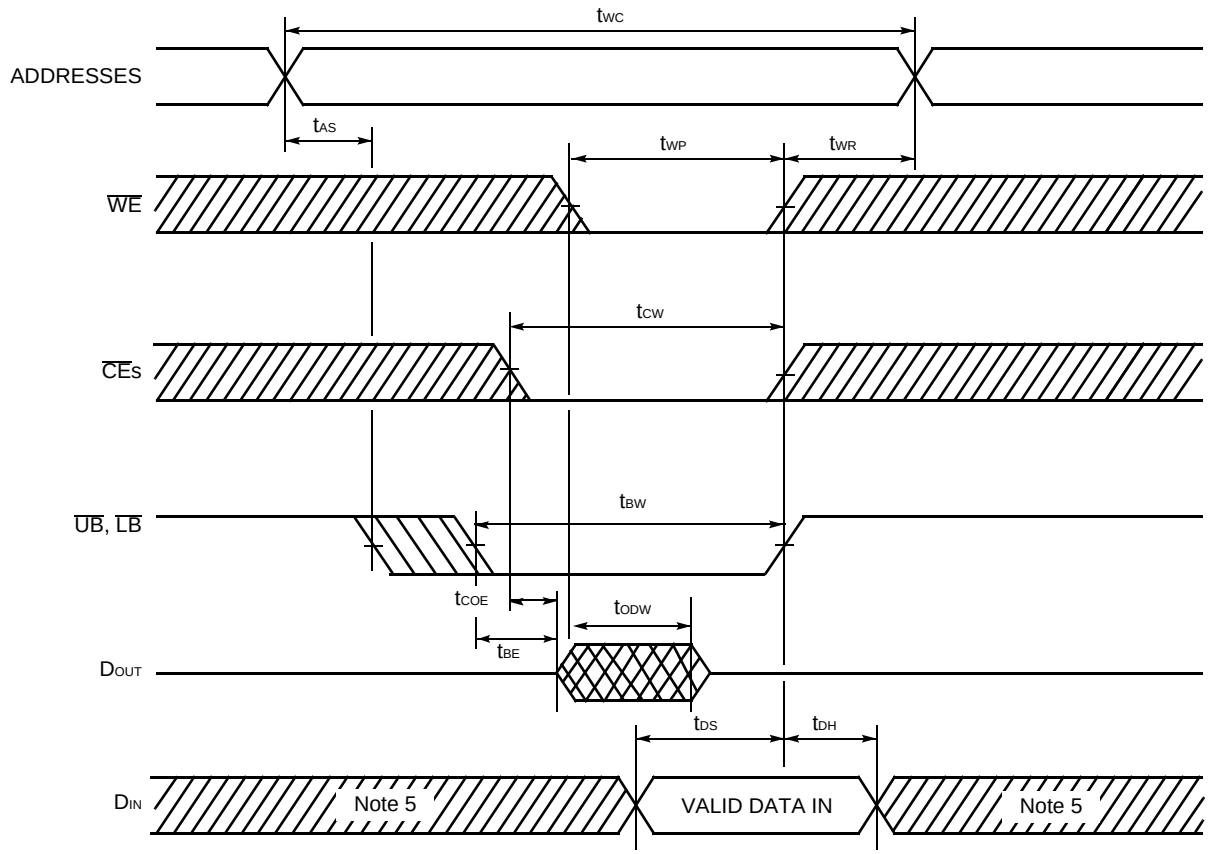
- **Write Cycle (Note 4) ($\overline{CE}$s control) (SRAM)**



Notes: 2. If $\overline{CE}$s goes LOW coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE}$s goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 4) ($\overline{UB}$, $\overline{LB}$ Control) (SRAM)**



Notes: 2. If $\overline{CE}$s goes LOW coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.

3. If $\overline{CE}$s goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

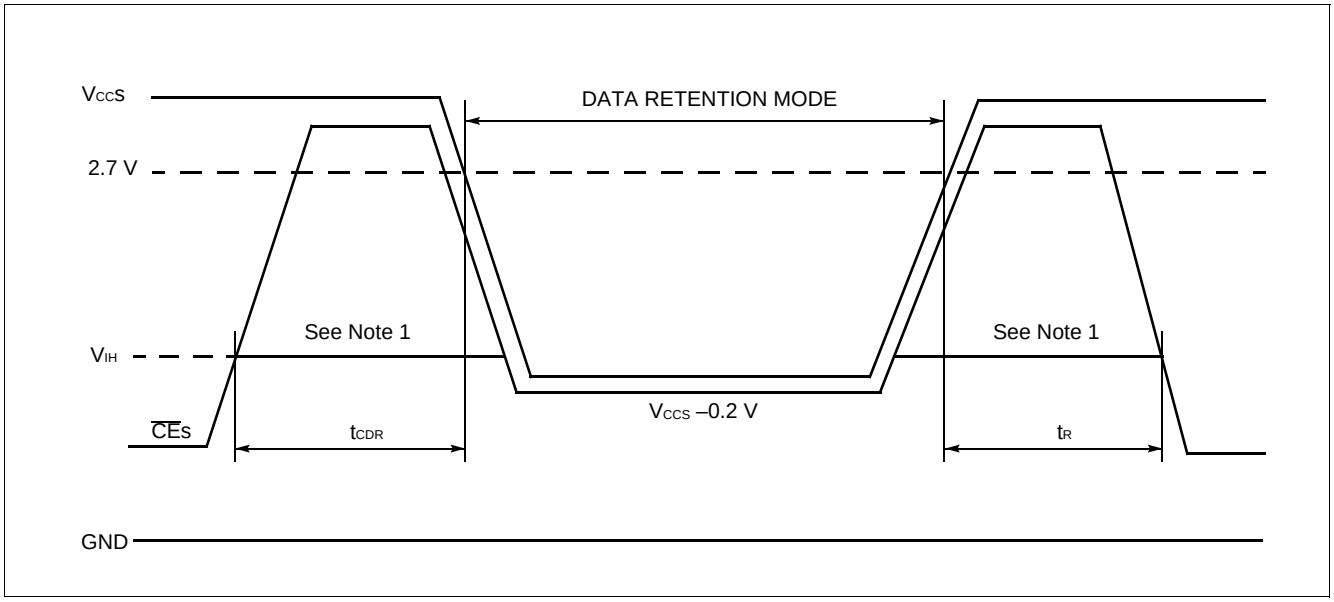
Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	µs	Excludes system-level overhead
Word Programming Time	—	16	360	µs	
Chip Programming Time	—	8.4	TBD	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ DATA RETENTION CHARACTERISTICS (SRAM)

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V_{DH}	Data Retention Supply Voltage		2.0	—	3.6	V
I_{DDS2}	Standby Current	V_{DH} = 3.0 V	—	—	50*	µA
t_{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t_R	Recovery Time		5	—	—	ms

* : 5 µA (Max.) at T_A = –20°C to +40°C

- **$\overline{CE1}$s Controlled Data Retention Mode**



Notes:1.) When $\overline{CE}$s is operating at the V_{IH} min. level (2.2 V), the standby current is given by I_{SB1}s during the transition of V_{CC}s from 3.6 to 2.2 V.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TBD	TBD	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TBD	TBD	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TBD	TBD	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ HANDRING OF PACKAGE

Please handle this package carefully since the sides of packages are right angle.

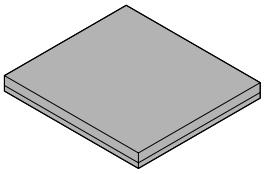
■ CAUTION

1.)The high voltage (VID) can not apply to address pins and control pins except $\overline{\text{RESET}}$. Therefore, it can not use autoselect and sector protect function by applying the high voltage (VID) to specific pins.

2.)For the sector protection, since the high voltage (VID) can be applied to the $\overline{\text{RESET}}$, it can be protected the sector useing "Extended sector protect" command.

■ PACKAGE

48-pin Plastic BGA

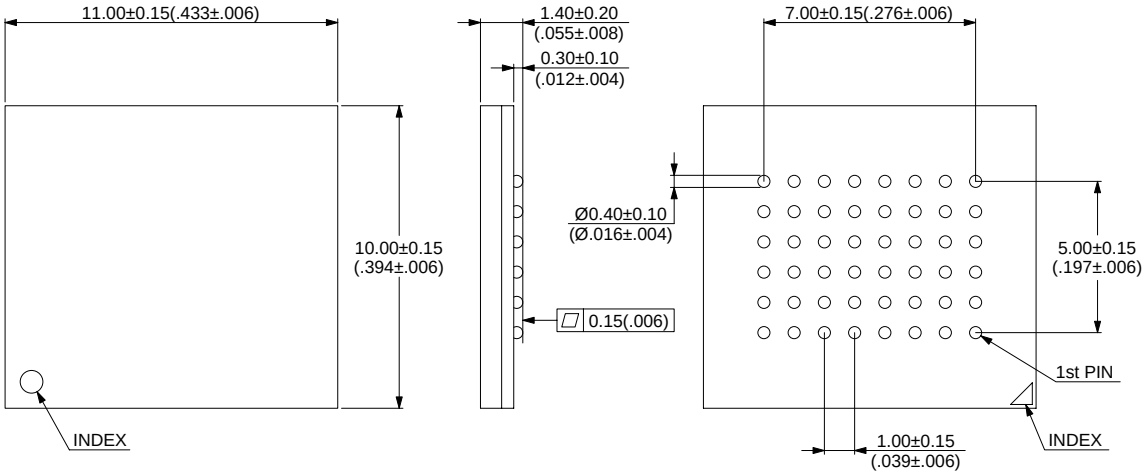


(BGA-48P-M06)

■ PACKAGE DIMENSIONS

48-pin Plastic BGA
(BGA-48P-M06)

Note: The actual shape of coners may differ from the dimension.



Dimension in mm (inches).

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