FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11411-2E

MEMORY

CMOS

2 × 1 M × 32-BIT SINGLE DATA RATE I/F FCRAM™

Consumer/Embedded Application Specific Memory for SiP

MB81ES653225-12/-12L

CMOS 2-Bank × 1,048,576-Word × 32-Bit
Fast Cycle Random Access Memory (FCRAM) with Single Data Rate for SiP

■ DESCRIPTION

The Fujitsu MB81ES653225 is a Single Data Rate Interface Fast Cycle Random Access Memory (FCRAM*) containing 67,108,864 memory cells accessible in a 32-bit format. The MB81ES653225 features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB81ES653225 is utilized using a Fujitsu advanced FCRAM core technology and designed for low power consumption and low voltage operation than regular synchronous DRAM (SDRAM) .

The MB81ES653225 is dedicated for SiP (System in a package) , and ideally suited for various embedded/ consumer applications including digital AVs and image processing where a large band width and low power consumption memory is needed.

* : FCRAM is a trademark of Fujitsu Limited, Japan.

■ PRODUCT LINE

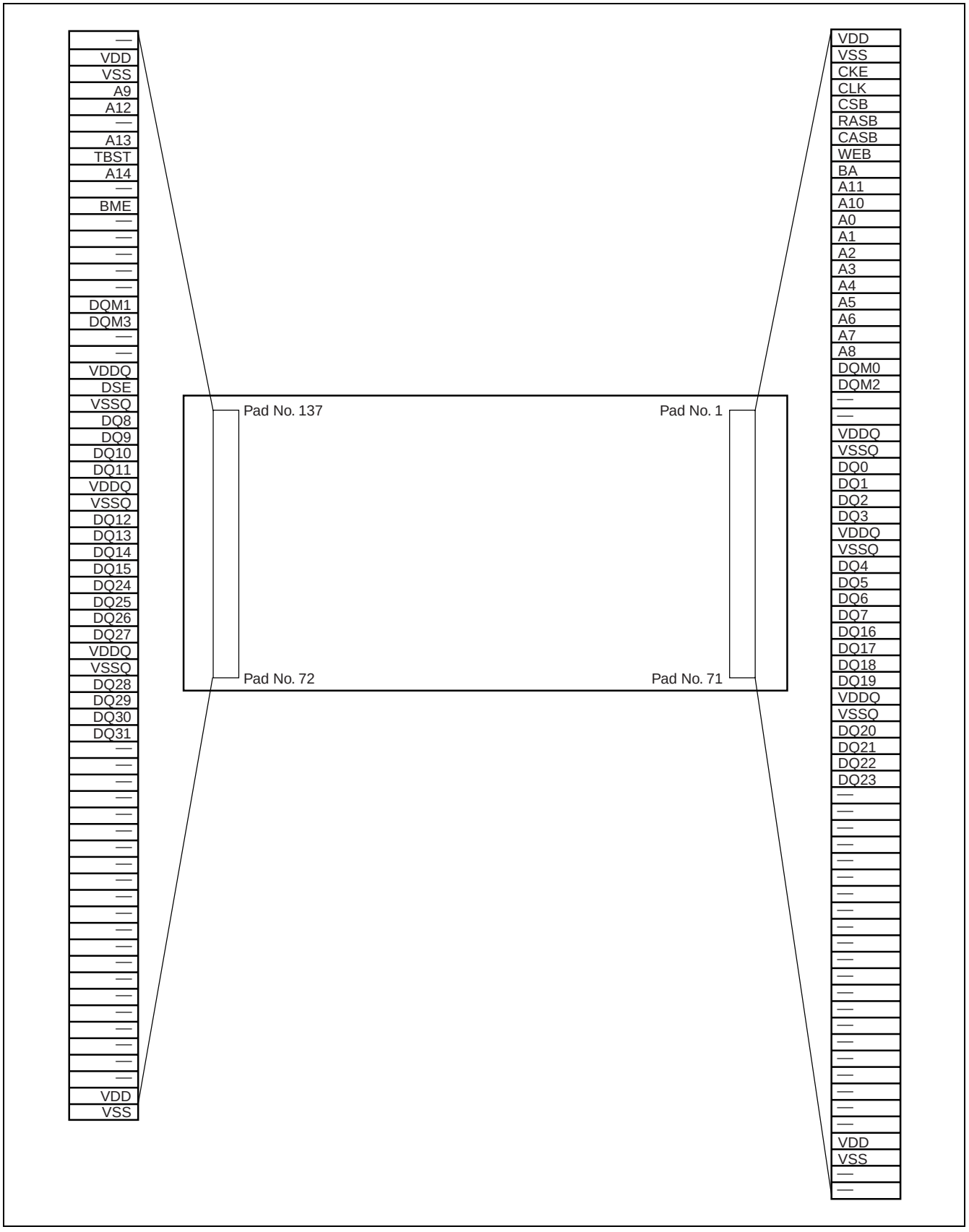
Parameter		MB81ES653225	
		12	12L
Clock Frequency (Max)	CL = 2	54.0 MHz	
	CL = 3	85.0 MHz	
Burst Mode Cycle Time (Min)	CL = 2	18.5 ns	
	CL = 3	11.7 ns	
Access Time from Clock (Max)	CL = 2	12 ns	
	CL = 3	8.7 ns	
Operating Current (Max) (32 page length)		35 mA	
Power Down Mode Current (Max)		0.5 mA	0.1 mA
Self Refresh Current (Max) (Ta = +85 °C)		1000 µA	450 µA

FUJITSU

■ FEATURES

- 1 M word × 32 bit × 2 banks organization
- Low power supply
  - V_{DD} : + 1.8 V ± 0.15 V
  - V_{DDQ} : + 1.8 V ± 0.15 V
- 1.8 V-CMOS I/O interface
- 8 K refresh cycles every 32 ms
- Auto-and Self-refresh
- Two banks operation
- Burst read/write operation and burst read/single write operation capability
- Programmable burst type, burst length, and CAS Latency
- Programmable page length function
- Programmable Partial Array Self Refresh (PASR)
- Programmable Temperature Compensated Self Refresh (TCSR)
- Deep power down mode
- Extended temperature operation
  - MB81ES653225-12 : From 0 °C to +85 °C (Ta)
  - MB81ES653225-12L : From −25 °C to +85 °C (Ta)
- CKE power down mode
- Output enable and input data mask
- Disable function for TEST
- Self burnin function for TEST
- Built In Self Test (BIST) function for TEST

■ PAD LAYOUT


Pad No. 137
Pad No. 1
Pad No. 72
Pad No. 71
—
VDD
VSS
A9
A12
—
A13
TBST
A14
—
BME
—
—
—
—
—
DQM1
DQM3
—
—
VDDQ
DSE
VSSQ
DQ8
DQ9
DQ10
DQ11
VDDQ
VSSQ
DQ12
DQ13
DQ14
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CKE
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CSB
RASB
CASB
WEB
BA
A11
A10
A0
A1
A2
A3
A4
A5
A6
A7
A8
DQM0
DQM2
—
—
VDDQ
VSSQ
DQ0
DQ1
DQ2
DQ3
VDDQ
VSSQ
DQ4
DQ5
DQ6
DQ7
DQ16
DQ17
DQ18
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VDD
VSS
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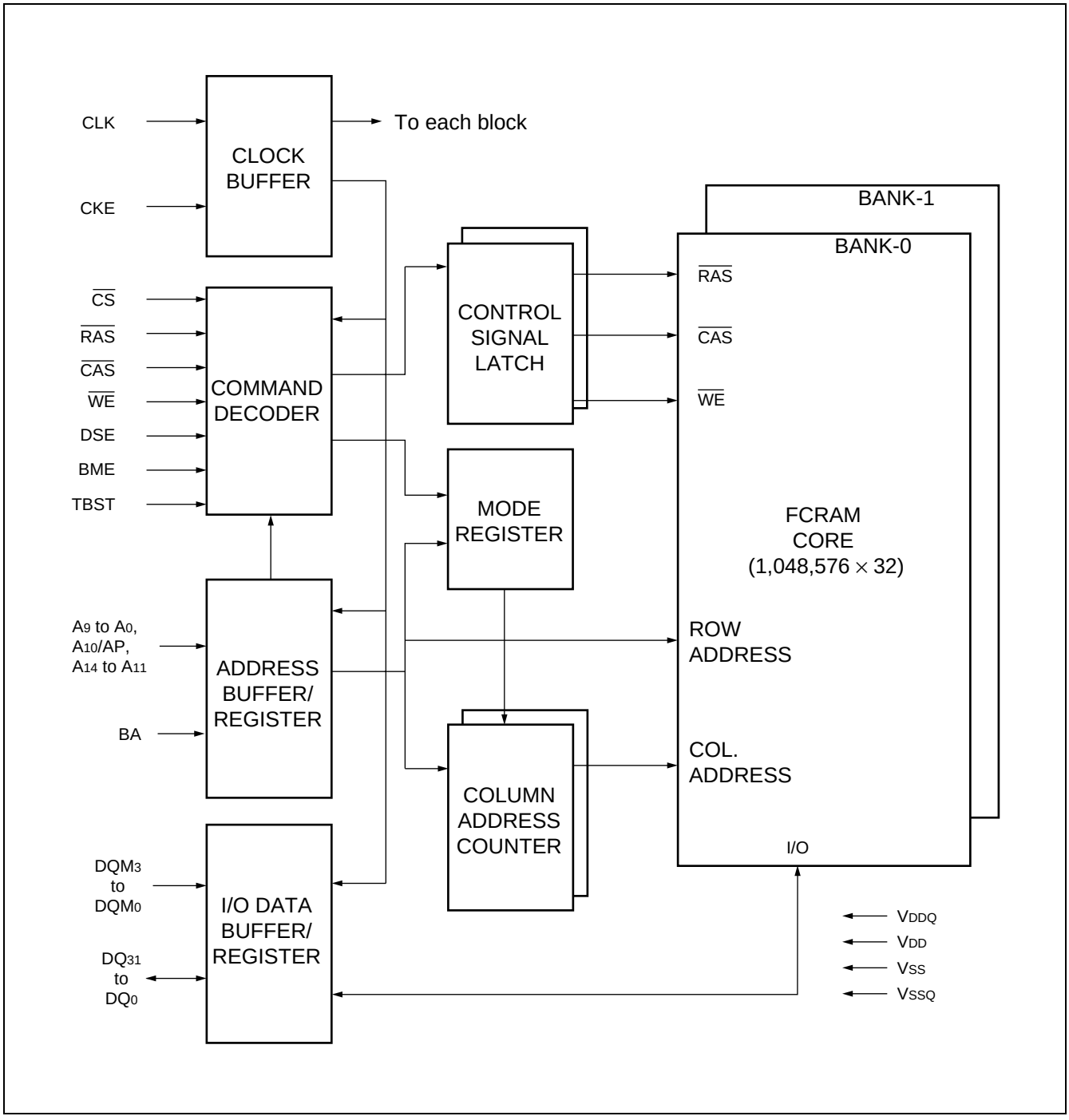
■ PAD DESCRIPTIONS

Symbol	Function			
V_{DDQ}, V_{DD}	Supply Voltage			
DQ_{31} to DQ_0	Data I/O			
V_{SSQ}, V_{SS}	Ground			
$\overline{WE}$ (WEB)	Write Enable			
$\overline{CAS}$ (CASB)	Column Address Strobe			
$\overline{RAS}$ (RASB)	Row Address Strobe			
$\overline{CS}$ (CSB)	Chip Select			
BA	Bank Select (Bank Address)			
AP	Auto Precharge Enable			
A_{14} to A_0 *	Address Input		Row	Column
		128 page	A_{12} to A_0	A_6 to A_0
		64 page	A_{13} to A_0	A_5 to A_0
		32 page	A_{14} to A_0	A_4 to A_0
CKE	Clock Enable			
CLK	Clock Input			
DQM_3 to DQM_0	Input Mask/Output Enable			
DSE	Disable Mode Entry (apply V_{SS} except Disable Mode)			
BME	Self Burn-in Mode Entry (apply V_{SS} except Self Burn-in Mode)			
TBST	BIST Mode Entry (apply V_{SS} except BIST Mode)			
—	Don’t Bond			

* : A_{13} must be connected to V_{SS} in 128 page length mode. A_{14} must be connected to V_{SS} in 128 page length mode and 64 page length mode.

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE *1

1. COMMAND TRUTH TABLE *2, *3, *4

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	Address (Except for A_{10})
		n-1	n							
Device Deselect *5	DESL	H	X	H	X	X	X	X	X	X
No Operation *5	NOP	H	X	L	H	H	H	X	X	X
Burst Stop *6, *7	BST	H	X	L	H	H	L	X	X	X
Read *7	READ	H	X	L	H	L	H	V	L	Column Address
Read with Auto-precharge *7	READA	H	X	L	H	L	H	V	H	Column Address
Write *7	WRIT	H	X	L	H	L	L	V	L	Column Address
Write with Auto-precharge *7	WRITA	H	X	L	H	L	L	V	H	Column Address
Bank Active *8	ACTV	H	X	L	L	H	H	V	Row Address	
Precharge Single Bank	PRE	H	X	L	L	H	L	V	L	X
Precharge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set *9, *10	MRS	H	X	L	L	L	L	V	V	V

*1 : V = Valid, L = Logic Low, H = Logic High, X = either L or H.
Row Address
128 page length : A_{12} to A_0
64 page length : A_{13} to A_0
32 page length : A_{14} to A_0
Column Address
128 page length : A_6 to A_0
64 page length : A_5 to A_0
32 page length : A_4 to A_0

*2 : All commands assume no CSUS command on previous rising edge of clock.

*3 : All commands are assumed to be valid state transitions.

*4 : All inputs are latched on the rising edge of clock.

*5 : NOP and DESL commands have the same effect. Unless specifically noted, NOP will represent both NOP and DESL command in later description.

*6 : When the current state is idle and CKE = L, BST command will represent Deep Power Down command. Refer to “3. CKE TRUTH TABLE” in section “■FUNCTION TRUTH TABLE”.

*7 : READ, READA, WRIT, WRITA and BST commands should only be issued after the corresponding bank has been activated (ACTV command) . Refer to “■STATE DIAGRAM”.

*8 : ACTV command should only be issued after corresponding bank has been precharged (PRE or PALL command) .

*9 : Required after power up. Refer to “22. POWER-UP INITIALIZATION” in section “■FUNCTIONAL DESCRIPTION”.

*10 : MRS command should only be issued after all banks have been precharged (PRE or PALL command) . Refer to “■STATE DIAGRAM”.

2. DQM TRUTH TABLE

Function	Symbol	CKE		DQMi *1, *2
		n-1	n	
Data Write/Output Enable	ENBi *1	H	X	L
Data Mask/Output Disable	MASKi *1	H	X	H

*1 : i = 0, 1, 2, 3

*2 : DQM_0 for DQ_7 to DQ_0, DQM_1 for DQ_{15} to DQ_8, DQM_2 for DQ_{23} to DQ_{16}, DQM_3 for DQ_{31} to DQ_{24}

3. CKE TRUTH TABLE *1

Current State	Function	Command	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A_{10} (AP)	Address (Except for A_{10})
			n-1	n							
Bank Active	Clock Suspend Mode Entry *2	CSUS	H	L	X	X	X	X	X	X	X
Any (Except Idle)	Clock Suspend Continue *2	—	L	L	X	X	X	X	X	X	X
Clock Suspend	Clock Suspend Mode Exit	—	L	H	X	X	X	X	X	X	X
Idle	Auto-refresh Command *3	REF	H	H	L	L	L	H	X	X	X
Idle	Self-refresh Entry *3, *4	SELF	H	L	L	L	L	H	X	X	X
Self Refresh	Self-refresh Exit *5	SELFX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Power Down Entry *3, *4	PD	H	L	L	H	H	H	X	X	X
			H	L	H	X	X	X	X	X	X
Power Down	Power Down Exit	PDX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X
Idle	Deep Power Down Entry *3, *4	DPD	H	L	L	H	H	L	X	X	X
Deep Power Down	Deep Power Down Exit	DPDX	L	H	L	H	H	H	X	X	X
			L	H	H	X	X	X	X	X	X

*1 : Address : A_{12} to A_0 @128 page length mode
: A_{13} to A_0 @64 page length mode
: A_{14} to A_0 @32 page length mode

*2 : The CSUS command requires that at least one bank is active. Refer to "■STATE DIAGRAM".

*3 : REF, SELF, DP and DPD commands should only be issued after all banks have been precharged (PRE or PALL command) . Refer to "■STATE DIAGRAM".

*4 : SELF, PD and DPD commands should only be issued after the last read data have been appeared on DQ.

*5 : CKE should be held high within one t_{RC} period after t_{CKSP}.

4. OPERATION COMMAND TABLE (single bank operation) *1

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	Bank Active after t_{RCD}
	L	L	H	L	BA, AP	PRE/PALL	NOP *5
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh *3, *6
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after t_{RSC}) *3, *7
Bank Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP
	L	L	H	H	BA, RA	ACTV	Illegal *2
	L	L	H	L	BA, AP	PRE/PALL	Precharge; Determine Precharge Type
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Stop → Bank Active
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, Start Write; Determine AP *4
	L	L	H	H	BA, RA	ACTV	Illegal *2
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Precharge → Idle
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Stop → Bank Active
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP *4
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP
	L	L	H	H	BA, RA	ACTV	Illegal *2
	L	L	H	L	BA, AP	PRE/PALL	Terminate Burst, Precharge → Idle
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Read with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Write with Auto-precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge → Idle)
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Precharging	H	X	X	X	X	DESL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	NOP (Idle after t_{RP}) *8
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	NOP (PALL may affect other bank) *5
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after t_{RCD})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *2
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACTV	
	L	L	H	L	BA, AP	PRE/PALL	
	L	L	L	H	X	REF/SELF	Illegal
	L	L	L	L	MODE	MRS	
Refreshing	H	X	X	X	X	DESL	NOP (Idle after t_{RC})
	L	H	H	X	X	NOP/BST	NOP (Idle after t_{RC}) *8
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal
	L	L	H	X	X	ACTV/ PRE/PALL	
	L	L	L	X	X	REF/SELF/ MRS	
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after t_{RSC})
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	X	X	READ/READA/ WRIT/WRITA	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	

RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

*1 : All command entries assume the CKE was High during the proceeding clock cycle and the current clock cycle.
After illegal commands are asserted, following command function and data could not be guaranteed.
If used, power up sequence be asserted after power shout down.

*2 : Illegal to bank in the specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.

*3 : Illegal if any bank is not idle.

*4 : Must satisfy bus contention, bus turn around, and/or write recovery requirements.
Refer to “11. READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4) ” and “12. WRITE TO READ TIMING (EXAMPLE @ CL = 2, BL = 4) ” in section “■TIMING DIAGRAMS”.

*5 : NOP to bank precharging or in idle state. May precharge bank specified by BA (and AP) .

*6 : SELF command should only be issued after the last read data have been appeared on DQ.

*7 : MRS command should only be issued on condition that all DQ are in Hi-Z.

*8 : BST command should only be issued with CKE = “H”.

5. COMMAND TRUTH TABLE FOR CKE *1

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function
Self-refresh	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after t_{RC})
	L	H	L	H	H	H	X	
	L	H	L	H	H	L	X	Illegal
	L	H	L	H	L	X	X	
	L	H	L	L	X	X	X	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid
	H	H	H	X	X	X	X	Idle after t_{RC}
	H	H	L	H	H	H	X	
	H	H	L	H	H	L	X	Illegal
	H	H	L	H	L	X	X	
	H	H	L	L	X	X	X	
	H	H	X	X	X	X	X	
	H	L	X	X	X	X	X	Illegal *2
Power Down	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Power Down Mode → Idle
	L	H	L	H	H	H	X	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)
	L	H	L	L	X	X	X	Illegal
	L	H	L	H	L	X	X	
Deep Power Down	H	X	X	X	X	X	X	Invalid
	L	H	H	X	X	X	X	Exit Deep Power Down Mode → Idle *3
	L	H	L	H	H	H	X	
	L	L	X	X	X	X	X	NOP (Maintain Deep Power Down Mode)
	L	H	L	L	X	X	X	Illegal
	L	H	L	H	L	X	X	

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Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function
Bank Active Bank Activating Read/Write All Banks Idle	H	H	X	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	X	X	X	X	X	Refer to “4. Operation Command table”. Start Clock Suspend next cycle
	L	X	X	X	X	X	X	Invalid
Precharging Refreshing	H	H	X	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	L	H	H	L	X	Illegal
	H	L	H	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	L	L	X	X	X	
	H	L	L	H	L	X	X	
	H	L	L	H	H	H	X	
	L	X	X	X	X	X	X	Invalid
Clock Suspend	H	X	X	X	X	X	X	Invalid
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle
	L	L	X	X	X	X	X	Maintain Clock Suspend
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid
	H	H	X	X	X	X	X	Refer to “4. Operation Command Table”.
	H	L	X	X	X	X	X	Illegal

*1 : All entries are specified at CKE (n) state. CKE input must satisfy corresponding set up and hold time for CKE.

*2 : CKE should be held High for t_{RC} period after t_{CKSP}.

*3 : After deep power down exit, it requires “19. DEEP POWER DOWN EXIT TIMINIG” procedure in section “■TIMING DIAGRAMS”.

■ FUNCTIONAL DESCRIPTION

1. SDR I/F FCRAM BASIC FUNCTION

Three major differences between this SDR I/F FCRAMs and conventional DRAMs are : synchronized operation, burst mode, and mode register.

The synchronized operation is the fundamental difference. An SDR I/F FCRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory although it has been using two clocks, $\overline{RAS}$ and $\overline{CAS}$. Each operation of DRAM is determined by their timing phase differences while each operation of SDR I/F FCRAM is determined by commands and all operations are referenced to a positive clock edge.

The burst mode is a very high speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The mode register is to justify the SDR I/F FCRAM operation and function into desired system conditions. Refer to "■MODE REGISTER TABLE".

2. FCRAM™

The MB81ES653225 utilizes FCRAM core technology. The FCRAM is an acronym of Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

3. CLOCK INPUT (CLK) and CLOCK ENABLE (CKE)

All input and output signals of SDR I/F FCRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged) , the Power Down mode (standby) is entered with CKE = Low and this will make low standby current. The standby current of the Deep Power Down mode is lower than that of the Power Down mode. This mode is entered with CKE = Low, $\overline{RAS}$ = $\overline{CAS}$ = High and $\overline{WE}$ = Low.

4. CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address input. When $\overline{CS}$ is High, command signals are negated but internal operation such as burst cycle will not be suspended. If such a control isn't needed, $\overline{CS}$ can be tied to ground level.

5. COMMAND INPUT ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ do not directly imply SDR I/F FCRAM operation, such as Row address strobe by $\overline{RAS}$. Instead, each combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SDR I/F FCRAM operation. Refer to "1. COMMAND TRUTH TABLE" in section "■FUNCTIONAL TRUTH TABLE."

6. ADDRESS INPUT (A_{14} to A_0)

Address input selects an arbitrary location of a total of 1,048,576 words of each memory cell matrix. Address field is defined for selected page length by the Programmable Page Length mode : 128 page length = A_{12} to A_0, 64 page length = A_{13} to A_0, 32 page length = A_{14} to A_0. A total of twenty address input signals are required to decode such a matrix. SDR I/F FCRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV) , Row addresses are initially latched and the remainder of Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA) .

7. BANK SELECT (BA)

This SDR I/F FCRAM has two banks in one part and each bank is organized as 1 Mwords by 32-bit. Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA) , write (WRIT or WRITA) , and precharge command (PRE) .

8. DATA INPUT AND OUTPUT (DQ_{31} to DQ_0)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input :

t_{RAC}; from the bank active command when t_{RCD} (Min) is satisfied. (This parameter is reference only.)
t_{CAC}; from the read command when t_{RCD} is greater than t_{RCD} (Min) . (This parameter is reference only.)
t_{AC} ; from the clock edge after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of the input. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}) .

9. DATA I/O MASK (DQM)

DQM is an active high enable input and has an output disable and input mask function. During burst cycle and when DQM_0 to DQM_3 = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type. DQM_0, DQM_1, DQM_2, DQM_3, controls DQ_7 to DQ_0, DQ_{15} to DQ_8, DQ_{23} to DQ_{16}, DQ_{31} to DQ_{24}, respectively.

10. BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same row address and by automatic strobing column address. Access time and cycle time of burst mode is specified as t_{AC} and t_{CK}, respectively. The internal column address counter operation is determined by a mode register which defines burst type and burst count length of 1, 2, 4 or 8 bits of boundary or full column. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required.

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after l_{OWD}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns + 1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0) . The interleave mode is a scrambled decoding scheme for A_2 and A_0. If the first access of column address is even (0) , the next address will be odd (1) , or vice-versa. When the full column burst operation is executed at single write mode, Auto-precharge command is valid only at write operation.

Burst Length	Starting Column Address A_2 A_1 A_0	Sequential Mode	Interleave Mode
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

11. FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same row. If burst mode reaches the end of column address, then it wraps around to the first column address (= 0) and continues to count until interrupted by the new read (READ) /write (WRIT) , precharge (PRE) , or burst stop (BST) commands. The selection of Auto-precharge option is illegal during the full column burst operation.

The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When a read mode is interrupted by the BST command, the output will be in High-Z. For the detailed rule, please refer to “8. READ INTERRUPTED BY BURST STOP (EXAMPLE @CL = 2, BL = Full Column” in section “■TIMING DIAGRAMS”. When a write mode is interrupted by the BST command, the data to be applied at the same time with the BST command will be ignored.

12. BURST READ & SINGLE WRITE

The burst read and single write mode provides single word write operation regardless of its burst length. In this mode, burst read operation does not be affected by this mode.

13. PROGRAMMABLE PAGE LENGTH FUNCTION

The programmable page length function provides lower operation current than regular SDRAM. Page length is selected by Mode Register Set, and row address field and column address field are defined for selected page length as below.

	Row address	Column address
128 page length	A_{12} to A_0	A_6 to A_0
64 page length	A_{13} to A_0	A_5 to A_0
32 page length	A_{14} to A_0	A_4 to A_0

Row/column address allocation at each page length is shown as the following table. For example, A_{14} (row address) at 32 page length mode is corresponded to A_5 (column address) at 64 page length mode.

32 page	Row : A_{14} to A_0															Column : A_4 to A_0				
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	4	3	2	1	0
64 page	Row : A_{13} to A_0														Column : A_0 to A_5					
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	5	4	3	2	1	0
128 page	Row : A_{12} to A_0													Column : A_6 to A_0						
	0	1	2	3	4	5	6	7	8	9	10	11	12	6	5	4	3	2	1	0

14. PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SDR I/F FCRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the Precharge command (PRE) . With the Precharge command, SDR I/F FCRAM will automatically be in standby state after precharge time (t_{RP}) . The precharged bank is selected by combination of AP and BA when Precharge command is asserted. If AP = High, all banks are precharged regardless of BA (PALL) . If AP = Low, a bank to be selected by BA is precharged (PRE) . The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion. This auto precharge is entered by AP = High when a read or write command is asserted. Refer to "1. COMMAND TRUTH TABLE" in section "■FUNCTIONAL TRUTH TABLE".

15. AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SDR I/F FCRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDR I/F FCRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 3.9 μs or a total 8192 refresh commands within 32 ms period.

16. SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX. The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF) . Once SDR I/F FCRAM enters the self-refresh mode, all inputs except for CKE will be "don't care" (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ

Note : When the burst refresh method is used, a total of 8,192 auto-refresh commands within 2 ms must be asserted prior to the self-refresh mode entry.

17. SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum t_{CKSP} after CKE brought high, and then the No Operation command (NOP) or the Deselect command (DESL) should be asserted within one t_{RC} period. CKE should be held High within one t_{RC} period after t_{CKSP}. Refer to "16. SELF-REFRESH ENTRY AND EXIT TIMING" in section "■TIMING DIAGRAMS" for the detail. It is recommended to assert an Auto-refresh command just after the t_{RC} period to avoid the violation of refresh period.

Note : When the burst refresh method is used, a total of 8,192 auto-refresh commands within 2 ms must be asserted after the self-refresh exit.

18. MODE REGISTER SET (MRS)

The mode register of SDR I/F FCRAM provides a variety of different operations. The register consists of five operation fields; Burst Length, Burst Type, CAS latency, Operation Code and Page length. Refer to "■MODE REGISTER TABLE". The mode register can be programmed by the Mode Register Set command (MRS) . Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command. MRS command should only be issued on condition that all DQ is in Hi-Z. The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDR I/F FCRAM. Refer to "22. POWER-UP INITIALIZATION".

19. EXTENDED MODE REGISTER SET (EMRS)

The extended mode register consists of two operation fields; Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR) . Refer to "■MODE REGISTER TABLE". The condition of the extended mode register is undefined after the Power-up stage. It is required to set each field after initialization of SDR I/F FCRAM. Refer to "22. POWER-UP INITIALIZATION".

20. PARTIAL ARRAY SELF REFRESH (PASR)

Memory array size to be refreshed during self refresh operation is programmable in order to reduce self refresh current. Data outside the defined area will not be retained during self refresh.

21. TEMPERATURE COMPENSATED SELF REFRESH (TCSR)

Programmable refresh rate for self refresh mode allows the system to control power as a function of temperature.

22. POWER-UP INITIALIZATION

The SDR I/F FCRAM internal condition after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply power (V_{DD} should be applied before or in parallel with V_{DDQ}) and start clock. Attempt to maintain either NOP or DESL command at the input.
2. Maintain stable power, stable clock, and NOP condition for a minimum of 100 µs.
3. Precharge all banks by Precharge (PRE) or Precharge All command (PALL) .
4. Assert minimum of 2 Auto-refresh command (REF) .
5. Program the mode register by Mode Register Set command (MRS) .
6. Program the extended mode register by Extended Mode Register Set command (EMRS) .

In addition, it is recommended DQM and CKE track V_{DD} to insure that output is High-Z state. The Mode Register Set command (MRS) and Extended Mode Register Set command (EMRS) can be set before 2 Auto-refresh command (REF) .

23. DISABLE MODE

When DSE is applied high level, SDR I/F FCRAM entries Disable mode. Disable mode entry doesn't require clock. In Disable mode, SDR I/F FCRAM current consumption is less than I_{DD2PS} and the output is High-Z. Any command isn't accepted in this mode. To exit Disable mode, apply Low level to DSE.

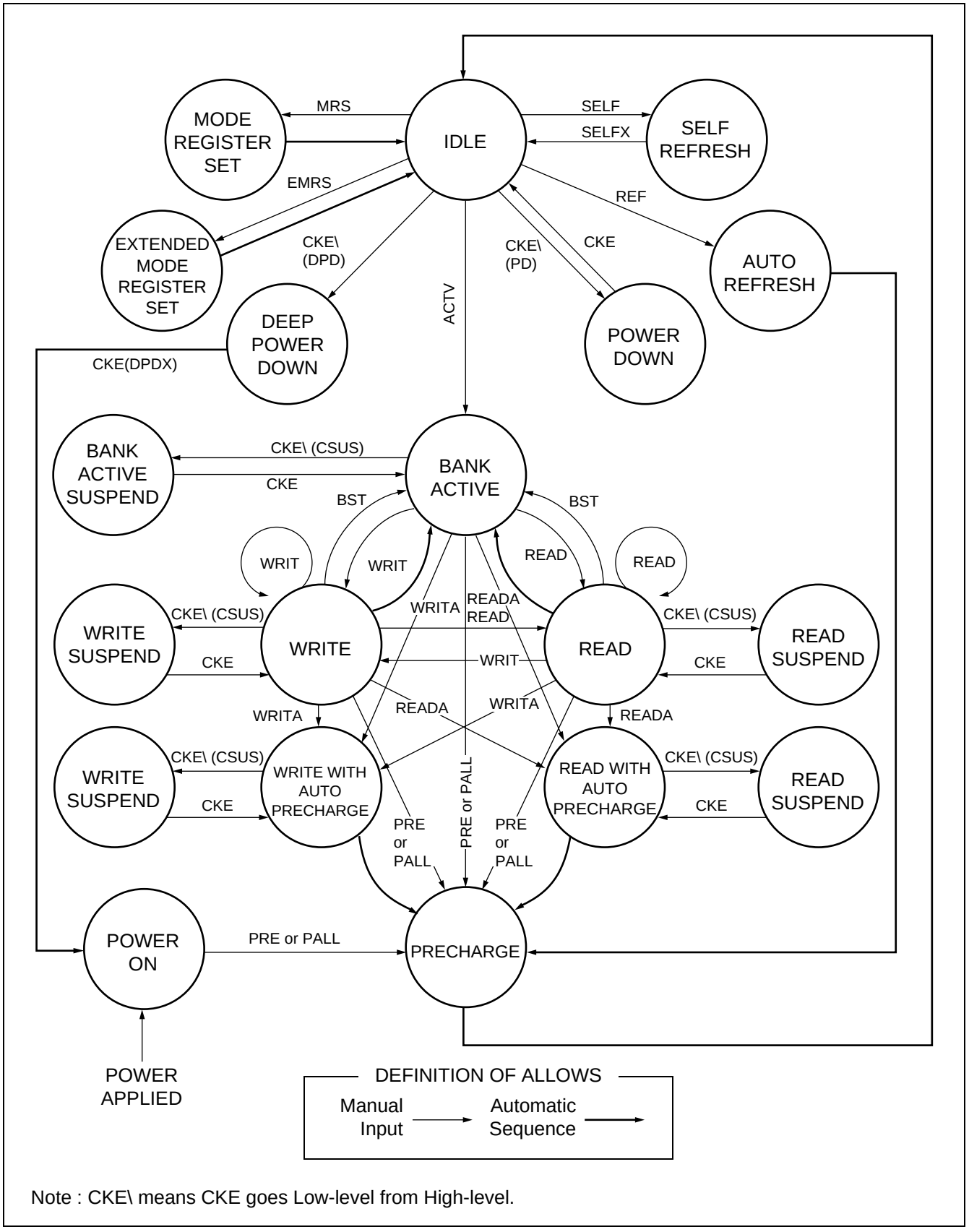
24. SELF BURNIN MODE

When BME is applied High level, SDR I/F FCRAM entries Self Burnin mode. Self Burnin mode entry doesn't require clock. In SELF BURNIN mode, self refresh command is asserted internally. Any command isn't accepted in this mode. To exit Self Burnin mode, apply Low level to BME.

25. BIST MODE

When TBST is applied High level, SDR I/F FCRAM entries BIST mode. BIST mode entry dosen’t require clock. To exit BIST mode, apply Low level to TBST.

■ STATE DIAGRAM



Note : CKE\ means CKE goes Low-level from High-level.

■ BANK OPERATION COMMAND TABLE

MINIMUM CLOCK LATENCY OR DELAY TIME FOR 1 BANK OPERATION

Second command (same bank) / First command	MRS	ACTV	READ	*4 READA	WRIT	*4 WRITA	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}	—	—	—	—	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV	—	—	t_{RCD}	t_{RCD}	t_{RCD}	t_{RCD}	t_{RAS}	t_{RAS}	—	—	1
READ	—	—	1	1	*5 1	*5 1	*4 1	*4 1	—	—	1
READA	*1, *2 BL + t_{RP}	BL + t_{RP}	—	—	—	—	*4 BL + t_{RP}	*4 BL + t_{RP}	*2 BL + t_{RP}	*2, *7 BL + t_{RP}	—
WRIT	—	—	t_{WR}	t_{WR}	1	1	*4 t_{DPL}	*4 t_{DPL}	—	—	1
WRITA	*2 BL–1 + t_{DAL}	BL–1 + t_{DAL}	—	—	—	—	*4 BL–1 + t_{DAL}	*4 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	—
PRE	*2, *3 t_{RP}	t_{RP}	—	—	—	—	1	*4 1	*2 t_{RP}	*2, *6 t_{RP}	1
PALL	*3 t_{RP}	t_{RP}	—	—	—	—	1	1	t_{RP}	*6 t_{RP}	1
REF	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

— : Illegal Command

*1 : If t_{RP} (Min) < CL × t_{CK}, minimum latency is a sum of (BL + CL) × t_{CK}.

*2 : Assume all banks are in Idle state.

*3 : Assume output is in High-Z state.

*4 : Assume t_{RAS} (Min) is satisfied.

*5 : Assume no I/O conflict.

*6 : Assume after the last data have been appeared on DQ.

*7 : If t_{RP} (Min) < (CL – 1) × t_{CK}, minimum latency is a sum of (BL + CL – 1) × t_{CK}.

MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTI BANK OPERATION

Second command (other bank) / First command	MRS	ACTV	READ *5	READA *5,*6	WRIT *5	WRITA *5, *6	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}	—	—	—	—	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV	—	*2 t_{RRD}	*7 1	*7 1	*7 1	*7 1	*6, *7 1	*7 t_{RAS}	—	—	1
READ	—	*2, *4 1	1	1	*10 1	*10 1	*6 1	*6 1	—	—	1
READA	*1, *2 BL + t_{RP}	*2, *4 1	*6 1	*6 1	*6, *10 1	*6, *10 1	*6 1	*6 BL + t_{RP}	*2 BL + t_{RP}	*2, *9 BL + t_{RP}	—
WRIT	—	*2, *4 1	1	1	1	1	*6 1	*6 t_{DPL}	—	—	1
WRITA	*2 BL–1 + t_{DAL}	*2, *4 1	*6 1	*6 1	*6 1	*6 1	*6 1	*6 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	*2 BL–1 + t_{DAL}	—
PRE	*2, *3 t_{RP}	*2, *4 1	*7 1	*7 1	*7 1	*7 1	*6, *7 1	*7 1	*2 t_{RP}	*2, *8 t_{RP}	1
PALL	*3 t_{RP}	t_{RP}	—	—	—	—	1	1	t_{RP}	*8 t_{RP}	1
REF	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}	—	—	—	—	t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

— : Illegal Command

*1 : If t_{RP} (Min) < CL × t_{CK}, minimum latency is a sum of (BL + CL) × t_{CK}.

*2 : Assume bank of the object is in Idle state.

*3 : Assume output is in High-Z state.

*4 : t_{RRD} (Min) of other bank (second command will be asserted) is satisfied.

*5 : Assume other bank is in active, read or write state.

*6 : Assume t_{RAS} (Min) is satisfied.

*7 : Assume other banks are not in READA/WRITA state.

*8 : Assume after the last data have been appeared on DQ.

*9 : If t_{RP} (Min) < (CL – 1) × t_{CK}, minimum latency is a sum of (BL + CL – 1) × t_{CK}.

*10 : Assume no I/O conflict.

■ MODE REGISTER TABLE

MODE REGISTER SET

BA	A_{14}*5	A_{13}*4	A_{12}	A_{11}	A_{10}	A_9	A_8*3	A_7*3	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
0	PL			0	0	Opcode	0	0	CL			BT	BL			MODE REGISTER

A_{14}	A_{13}	A_{12}	PAGE LENGTH
GND	GND	1	128 page
GND	1	0	64 page
GND	1	1	Reserved
1	0	0	32 page
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_6	A_5	A_4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Length	
			BT = 0	BT = 1*2
0	0	0	1	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Column	Reserved

A_9	Op-code
0	Burst Read & Burst Write
1	Burst Read & Single Write *1

A_3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round, Binary-up)

EXTENDED MODE REGISTER

BA	A_{14}*5	A_{13}*4	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	ADDRESS
1	0	0	0	0	0	0	0	0	0	0	TCSR		PASR			EXTENDED MODE REGISTER

A_4	A_3	MAX TEMPERATURE (T_a) *6
0	0	+ 70 °C
0	1	+ 45 °C
1	0	+ 15 °C
1	1	+ 85 °C

A_2	A_1	A_0	SELF REFRESH AREA
0	0	0	64 M bit
0	0	1	32 M bit (RA_{11} = 0)
0	1	0	16 M bit (RA_{11} = RA_{10} = 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

*1. When A_9 = 1, burst length at Write is always one regardless of BL value.
*2. BL = 1 and Full column are not applicable to the interleave mode.
*3. A_7 = 1 and A_8 = 1 are reserved for vender test.
*4. A_{13} exists at operation with 32 and 64 page length mode.
*5. A_{14} exists at operation with 32 page length mode.
*6. T_a is ambient temperature.

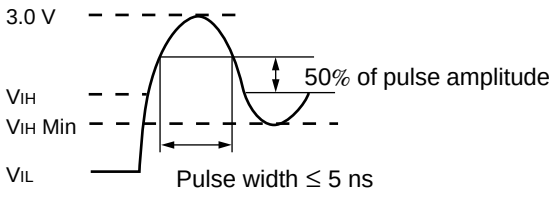
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage Relative to V_{SS}	V_{DD}, V_{DDQ}	− 0.5	+ 3.0	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	− 0.5	+ 3.0	V
Short Circuit Output Current	I_{OUT}	− 50	+ 50	mA
Power Dissipation	P_D	—	1.0	W
Storage Temperature	T_{STG}	− 55	+ 125	°C

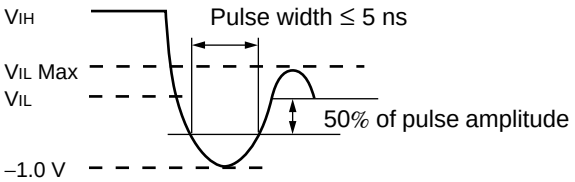
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply Voltage		V_{DD}, V_{DDQ}	1.65	1.8	1.95	V
		V_{SS}, V_{SSQ}	0	0	0	V
Input High Voltage *1		V_{IH}	$V_{DDQ} \times 0.8$	—	$V_{DDQ} + 0.3$	V
Input Low Voltage *2		V_{IL}	–0 .3	—	$V_{DDQ} \times 0.2$	V
Ambient Temperature	MB81ES653225-12	Ta	0	—	+ 85	°C
	MB81ES653225-12L		− 25	—	+ 85	°C
Junction Temperature *3	MB81ES653225-12	Tj	0	—	+ 100	°C
	MB81ES653225-12L		− 25	—	+ 100	°C



*1 : Overshoot limit :
V_{IH} (Max) = 3.0 V for pulse width ≤ 5 ns,
pulse width measured at 50% of pulse amplitude.



*2 : Undershoot limit :
V_{IL} (Min) = V_{SSQ} − 1.0 V for pulse width ≤ 5 ns,
pulse width measured at 50% of pulse amplitude.

*3 : The maximum junction temperature of FCRAM (Tj) should not be more than 100 °C.
Tj is represented by the power consumption of FCRAM (P_{FCRAM}) and Logic LSI (PD) , the thermal resistance of the package (θ ja) , and the maximum ambient temperature of the SiP (Tamax) .

Σ pmax[W] = P_{FCRAM} + PD
Tjmax[°C] = Tamax[°C] + θ ja[°C/W] × Σ pmax[W]

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ CAPACITANCE

(T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance, Except for CLK	C_{IN1}	1.5	—	3.0	pF
Input Capacitance for CLK	C_{IN2}	1.5	—	3.0	pF
I/O Capacitance	$C_{I/O}$	2.0	—	4.0	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter		Symbol	Condition		Value Min	Value Max	Unit
Output High Voltage		$V_{OH\ (DC)}$	I_{OH} = –0.1 mA		V_{DDQ} – 0.2	—	V
Output Low Voltage		$V_{OL\ (DC)}$	I_{OL} = 0.1 mA		—	0.2	V
Input Leakage Current		I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}; All other pins not under test = 0 V		–5	5	µA
Output Leakage Current		I_{LO}	0 V ≤ V_{IN} ≤ V_{DDQ}; Data out disabled		–5	5	µA
Operating Current (Average Power Supply Current)		I_{DD1}	Burst Length = 1 t_{RC} = Min, t_{CK} = Min One bank active Output pin open Address changed up to 1 time during t_{RC} (Min) 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	128 page length	—	50	mA
				64 page length	—	40	
				32 page length	—	35	
Precharge Standby Current (Power Supply Current)	-12	I_{DD2P}	CKE = V_{IL} All banks idle t_{CK} = Min Power down mode 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}		—	1	mA
	-12L				—	0.4	
	-12	I_{DD2PS}	CKE = V_{IL} All banks idle CLK = V_{IH} or V_{IL} Power down mode 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}		—	0.5	mA
	-12L				—	0.1	
		I_{DD2N}	CKE = V_{IH} All banks idle, t_{CK} = 20 ns NOP commands only, Input signals (except for CMD) are changed 1 time during 2 clocks. 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}		—	8	mA
		I_{DD2NS}	CKE = V_{IH} All banks idle CLK = V_{IH} or V_{IL} Input signal are stable. 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}		—	1	mA

(Continued)

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter		Symbol	Condition	Value		Unit
				Min	Max	
Active Standby Current (Power Supply Current)	-12	I_{DD3P}	CKE = V_{IL} Any bank active t_{CK} = Min 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	—	1	mA
	-12L			—	0.7	
	-12	I_{DD3PS}	CKE = V_{IL} Any bank active CLK = V_{IH} or V_{IL} 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	—	0.7	mA
	-12L			—	0.5	
		I_{DD3N}	CKE = V_{IH} Any bank active t_{CK} = 20 ns NOP commands only, Input signals (except for CMD) are changed 1 time during 2 clocks. 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	—	14	mA
		I_{DD3NS}	CKE = V_{IH} Any bank active CLK = V_{IH} or V_{IL} Input signals are stable. 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	—	1	mA
Burst mode Current (Average Power Supply Current)		I_{DD4}	t_{CK} = Min Burst Length = 4 Output pin open All-banks active Gapless data 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	—	68	mA
Refresh Current#1 (Average Power Supply Current)		I_{DD5}	Auto-refresh; t_{CK} = Min t_{RC} = Min 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}	—	50	mA

(Continued)

(Continued)

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter		Symbol	Condition			Value		Unit
						Min	Max	
Refresh Current #2 *4 (Average Power Supply Current)	-12	I_{DD6}	Self-refresh; t_{CK} = Min CKE ≤ 0.2 V 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DDQ}	TCSR = “00” (Ta ≤ +70 °C)	PASR = “000” (64 Mbit)	—	760	µA
	-12L					—	285	
	-12				PASR = “001” (32 Mbit)	—	640	
	-12L					—	200	
	-12				PASR = “010” (16 Mbit)	—	580	
	-12L					—	155	
	-12			TCSR = “01” (Ta ≤ +45 °C)	PASR = “000” (64 Mbit)	—	640	
	-12L					—	200	
	-12				PASR = “001” (32 Mbit)	—	580	
	-12L					—	150	
	-12				PASR = “010” (16 Mbit)	—	550	
	-12L					—	130	
	-12			TCSR = “10” (Ta ≤ +15 °C)	PASR = “000” (64 Mbit)	—	560	
	-12L					—	130	
	-12				PASR = “001” (32 Mbit)	—	540	
	-12L					—	115	
	-12				PASR = “010” (16 Mbit)	—	530	
	-12L					—	105	
	-12			TCSR = “11” (Ta ≤ +85 °C)	PASR = “000” (64 Mbit)	—	1000	
	-12L					—	450	
	-12				PASR = “001” (32 Mbit)	—	760	
	-12L					—	290	
	-12				PASR = “010” (16 Mbit)	—	640	
	-12L					—	205	
Precharge Stand-by Current in Deep Power Down mode	-12	I_{DD7}	CKE ≤ 0.2 V All banks idle Deep Power Down mode 0 V ≤ V_{IN} ≤ V_{IL} Max V_{IH} Min ≤ V_{IN} ≤ V_{DD}			—	50	µA
	-12L					—	10	

*1 : All voltages are referenced to V_{SS}.

*2 : DC characteristics are measured after following the “22. POWER-UP INITIALIZATION” procedure in section “■FUNCTIONAL DESCRIPTION.”

*3 : I_{DD} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open and no termination resistor.

*4 : The measurement conditions of I_{DD6} is assumed below.
Total power of devices in package (Σ pmax) = 0.75 W
The thermal resistance of the package (θ ja) = 20 °C/W

■ AC CHARACTERISTICS

1. BASIC AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) *1, *2, *3

Parameter			Symbol	Value		Unit
				Min	Max	
Clock Period	CL = 2		t_{CK2}	18.5	—	ns
	CL = 3		t_{CK3}	11.7	—	ns
Clock High Time *5			t_{CH}	$t_{CK} \times 0.3$	—	ns
Clock Low Time *5			t_{CL}	$t_{CK} \times 0.3$	—	ns
Input Setup Time *5			t_{SI}	2.5	—	ns
Input Hold Time *5			t_{HI}	1	—	ns
Access Time from Clock (T_{CK} = Min) *5, *6, *7	CL = 2		t_{AC2}	—	12	ns
	CL = 3		t_{AC3}	—	8.7	ns
Output in Low-Z *5			t_{LZ}	0	—	ns
Output in High-Z *5, *7, *8	CL = 2	-12	t_{HZ2}	2	12	ns
		-12L		1.5		
	CL = 3	-12	t_{HZ3}	2	8.7	ns
		-12L		1.5		
Output Hold Time *4		-12	t_{OH}	2	—	ns
		-12L		1.5		
Time between Auto-Refresh command interval			t_{REFI}	—	3.9	µs
Time between Refresh			t_{REF}	—	32	ms
Transition Time			t_T	0.5	10	ns
CKE Setup Time for Power Down Exit Time *5			t_{CKSP}	2.5	—	ns

*1 : AC characteristics are measured after following the “22. POWER-UP INITIALIZATION” procedure in section “■FUNCTIONAL DESCRIPTION”.

*2 : AC characteristics assume t_T = 1 ns, 10 pF of capacitive load and 50 Ω of terminated load.
Refer to “5. MEASUREMENT CONDITION OF THE AC CHARACTERISTICS”.

*3 : 0.9 V is the reference level for 1.8 V I/O for measuring timing of input/output signals. Transition times are measured between V_{IH} (Min) and V_{IL} (Max) .

*4 : This value is for reference only.

*5 : If input signal transition time (t_T) is longer than 1 ns; [(t_T/2) – 0.5] ns should be added to t_{AC} (Max) , t_{HZ} (Max) , and t_{CKSP} (Min) spec values, [(t_T/2) – 0.5] ns should be subtracted from t_{LZ} (Min) , t_{HZ} (Min) , and t_{OH} (Min) spec values, and (t_T – 1.0) ns should be added to t_{CH} (Min) , t_{CL} (Min) , t_{SI} (Min) , and t_{HI} (Min) spec values.

*6 : t_{AC} also specifies the access time at burst mode.

*7 : t_{AC} and t_{OH} are measured under output load circuit shown in “5. MEASUREMENT CONDITION OF THE AC CHARACTERISTICS”.

*8 : Specified where output buffer is no longer driven.

2. BASE VALUES FOR CLOCK COUNT/LATENCY

Parameter			Symbol	Value		Unit
				Min	Max	
$\overline{RAS}$ Cycle Time *			t_{RC}	80	—	ns
$\overline{RAS}$ Precharge Time			t_{RP}	20	—	ns
$\overline{RAS}$ Active Time			t_{RAS}	60	110000	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time			t_{RCD}	20	—	ns
Write Recovery Time			t_{WR}	11.7	—	ns
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time			t_{RRD}	20	—	ns
Data-in to Precharge Lead Time			t_{DPL}	18.5/20	—	ns
Data-in to Active/Refresh Command Period	CL = 2	-12	t_{DAL2}	1 cyc + t_{RP}	—	ns
		-12L		2 cyc + t_{RP}		
	CL = 3	-12	t_{DAL3}	2 cyc + t_{RP}	—	ns
		-12L		2 cyc + t_{RP}		
Mode Register Set Cycle Time			t_{RSC}	20	—	ns

* : Actual clock count of t_{RC} (l_{RC}) will be sum of clock count of t_{RAS} (l_{RAS}) and t_{RP} (l_{RP}) .

3. CLOCK COUNT FORMULA

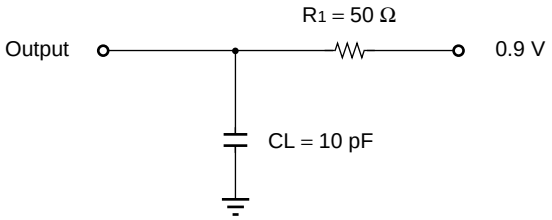
$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round up a whole number)}$$

Note : All base values are measured from the clock edge at the command input to the clock edge for the next command input. All clock counts are calculated by a simple formula : clock count equals base value divided by clock period (round off to a whole number) .

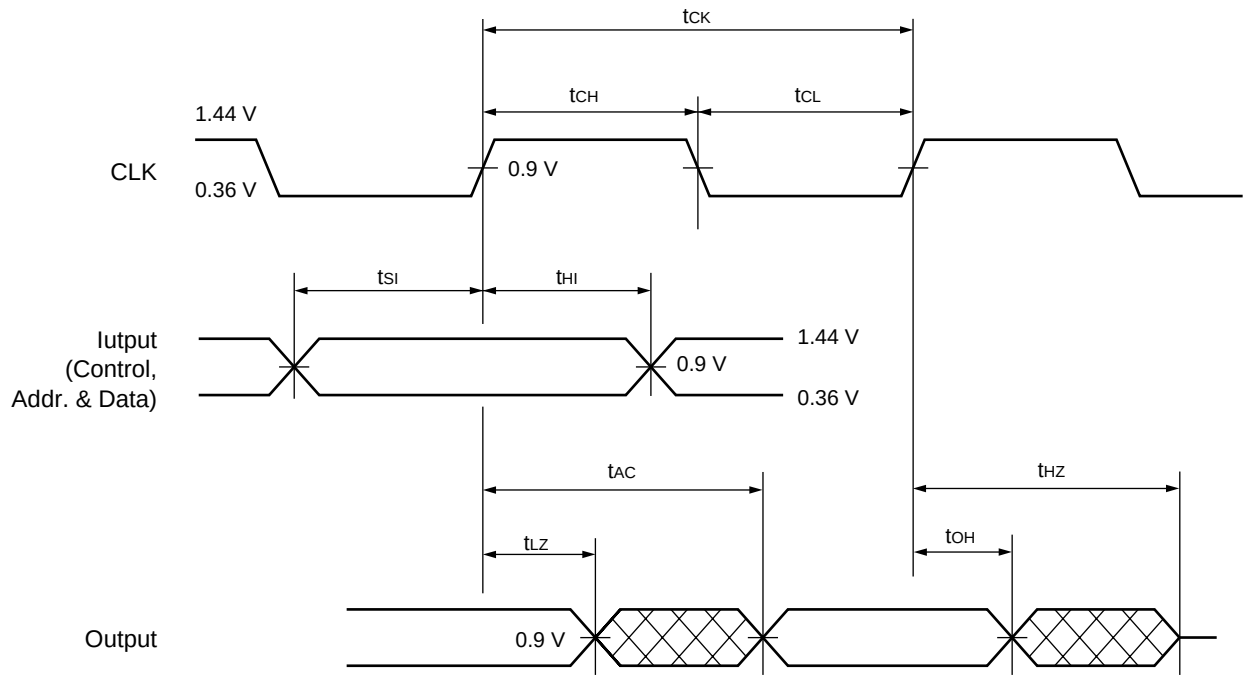
4. LATENCY (The latency values on these parameters are fixed regardless of clock period.)

Parameter		Symbol	MB81ES653225-12	MB81ES653225-12L	Unit
CKE to Clock Disable		l_{CKE}	1	1	cycle
DQM to Output in High-Z		l_{DQZ}	2	2	cycle
DQM to Input Data Delay		l_{DQD}	0	0	cycle
Last Output to Write Command Delay		l_{OWD}	2	2	cycle
Write Command to Input Data Delay		l_{DWD}	0	0	cycle
Precharge to Output in High-Z Delay	CL = 2	l_{ROH2}	2	2	cycle
	CL = 3	l_{ROH3}	3	3	cycle
Burst Stop Command to Output in High-Z Delay	CL = 2	l_{BSH2}	2	2	cycle
	CL = 3	l_{BSH3}	3	3	cycle
$\overline{CAS}$ to $\overline{CAS}$ Delay (Min)		l_{CCD}	1	1	cycle
$\overline{CAS}$ Bank Delay (Min)		l_{CBD}	1	1	cycle

5. MEASUREMENT CONDITION OF AC CHARACTERISTICS

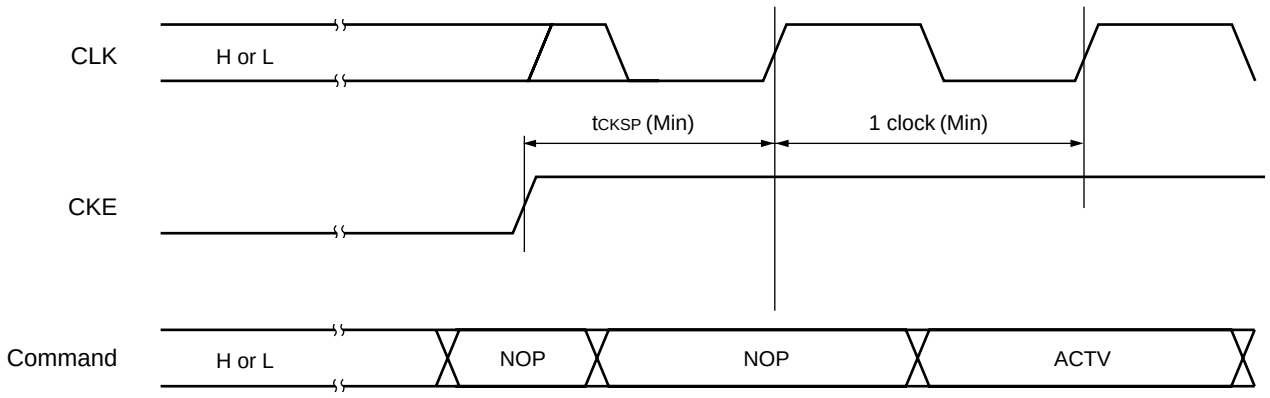


6. SETUP, HOLD AND DELAY TIME

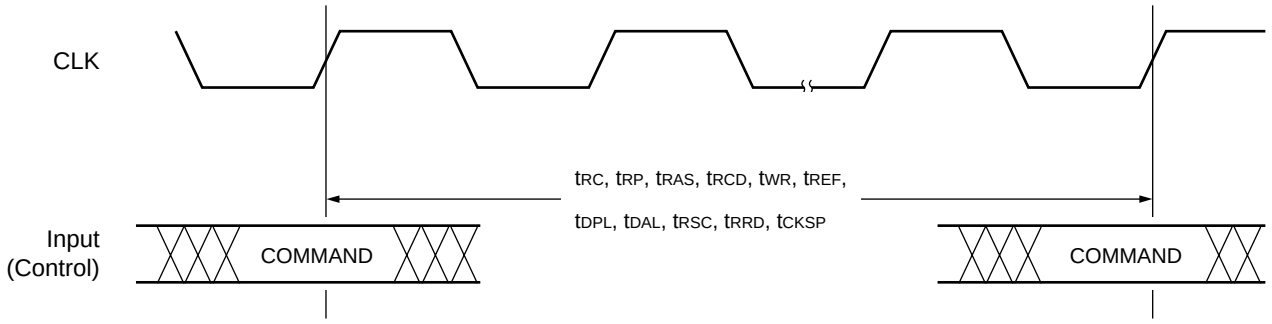


Note : Reference level of input signal is 0.9 V for LVCMOS.
Access time is measured at 0.9 V for LVCMOS.
AC characteristics are also measured in this condition.

7. DELAY TIME FOR POWER DOWN EXIT

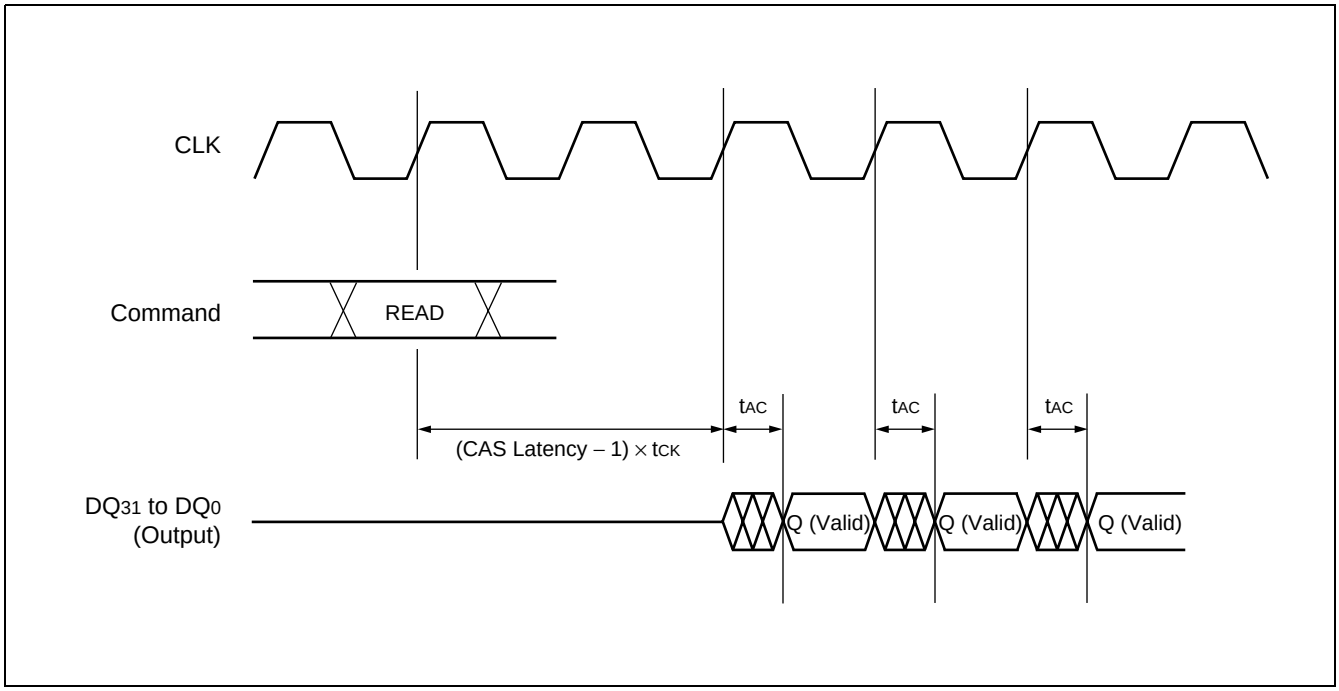


8. PULSE WIDTH



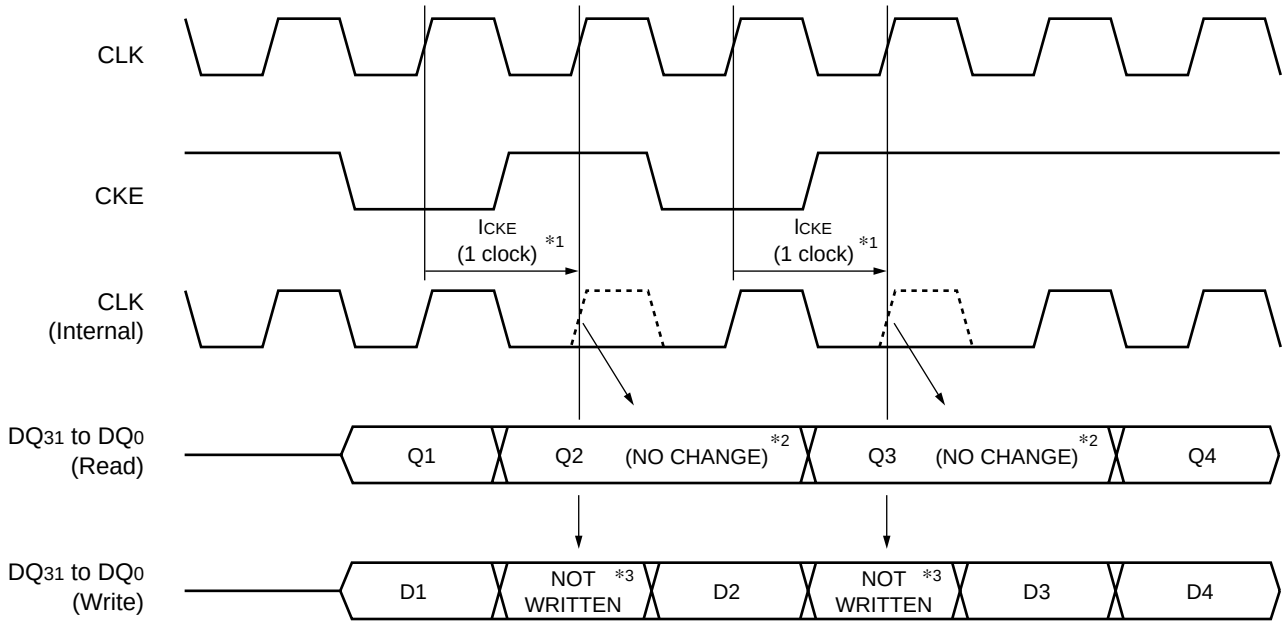
Note : These parameters are a limit value of the rising edge of the clock from one command input to next input.
t_{CKSP} is the latency value from the rising edge of CKE.
Measurement reference voltage is 0.9 V.

9. ACCESS TIME



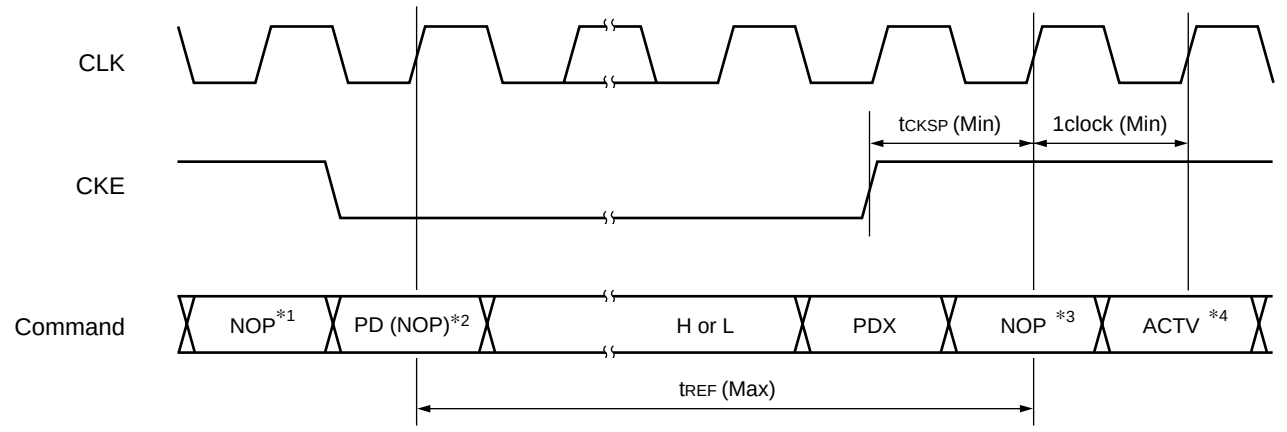
■ TIMING DIAGRAMS

1. CLOCK ENABLE-READ AND WRITE SUSPEND (@ BL = 4)



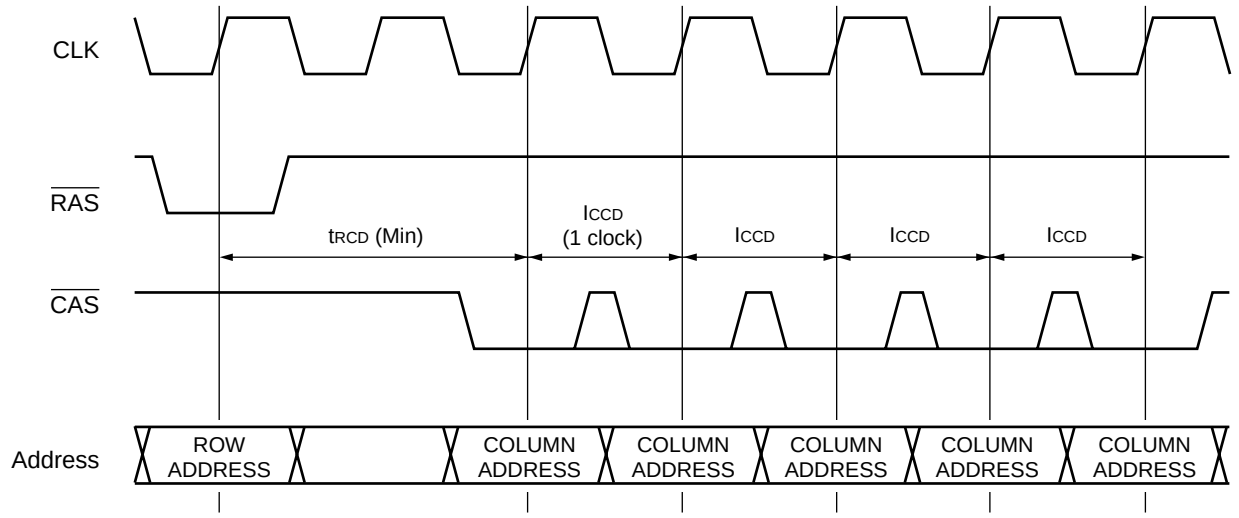
*1 : The latency of CKE (l_{CKE}) is one clock.
*2 : During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output data remain the same data.
*3 : During the write mode, data at the next clock of CSUS command is ignored.

2. POWER DOWN ENTRY AND EXIT



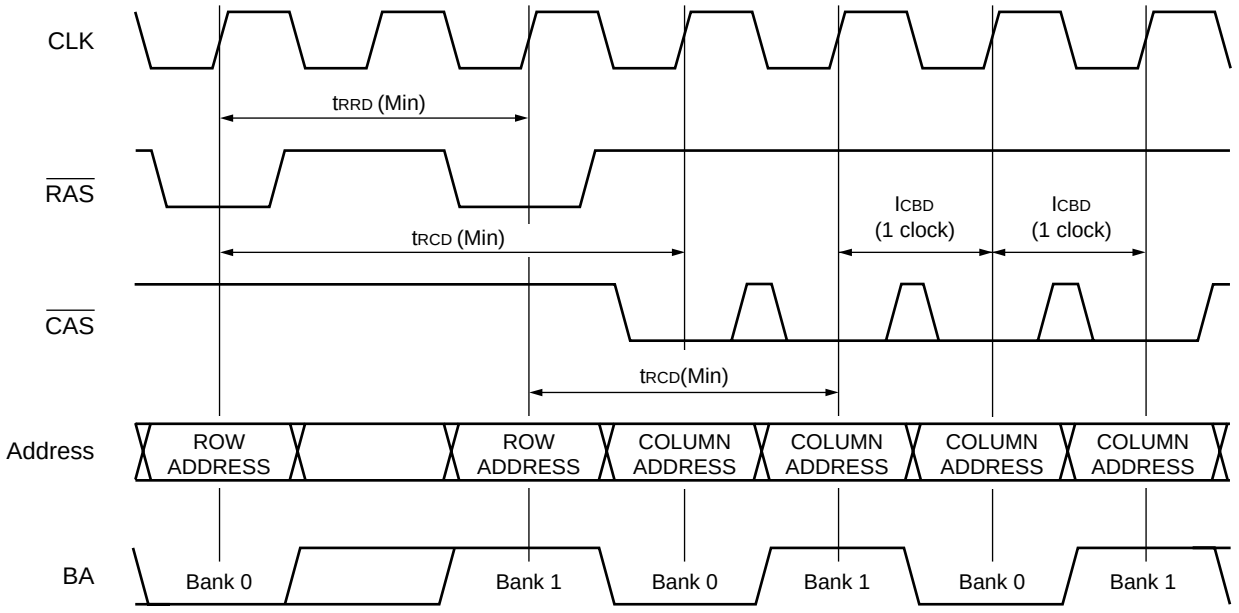
*1 : Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.
*2 : Precharge command can be posted in conjunction with CKE after the last read data have been appeared on DQ.
*3 : It is recommended to apply NOP command in conjunction with CKE.
*4 : The ACTV command can be latched after t_{CKSP} (Min) + 1 clock (Min) .

3. COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY



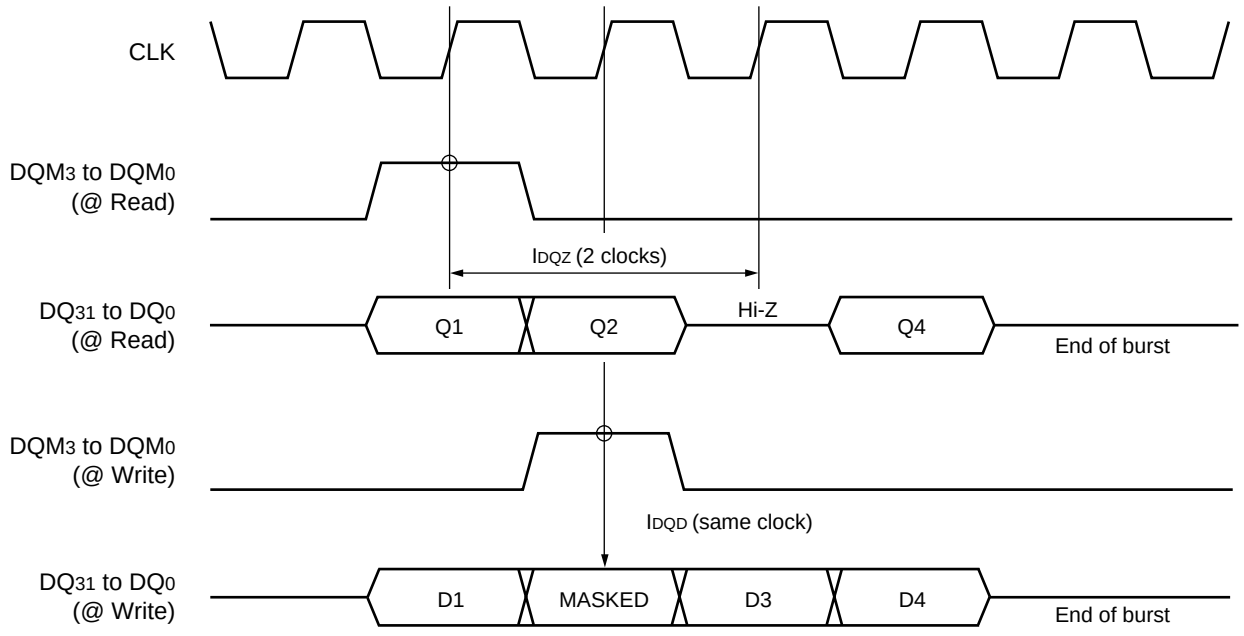
Note : $\overline{CAS}$ to $\overline{CAS}$ delay (l_{CCD}) can be one or more clock period.

4. DIFFERENT BANK ADDRESS INPUT DELAY

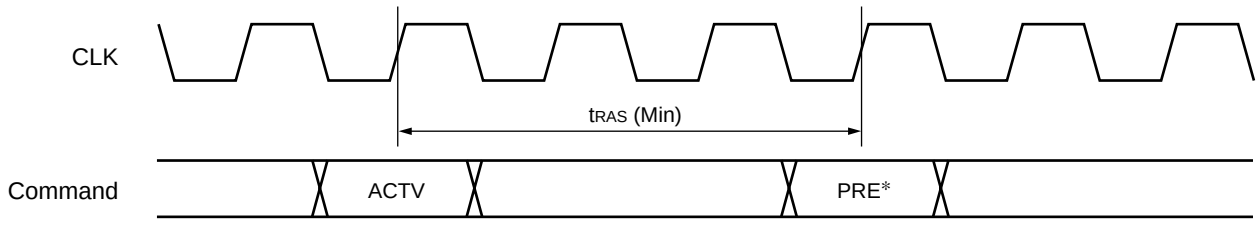


Note : $\overline{CAS}$ Bank delay (l_{CBD}) can be one or more clock period.

5. INPUT MASK AND OUTPUT DISABLE (@ BL = 4)

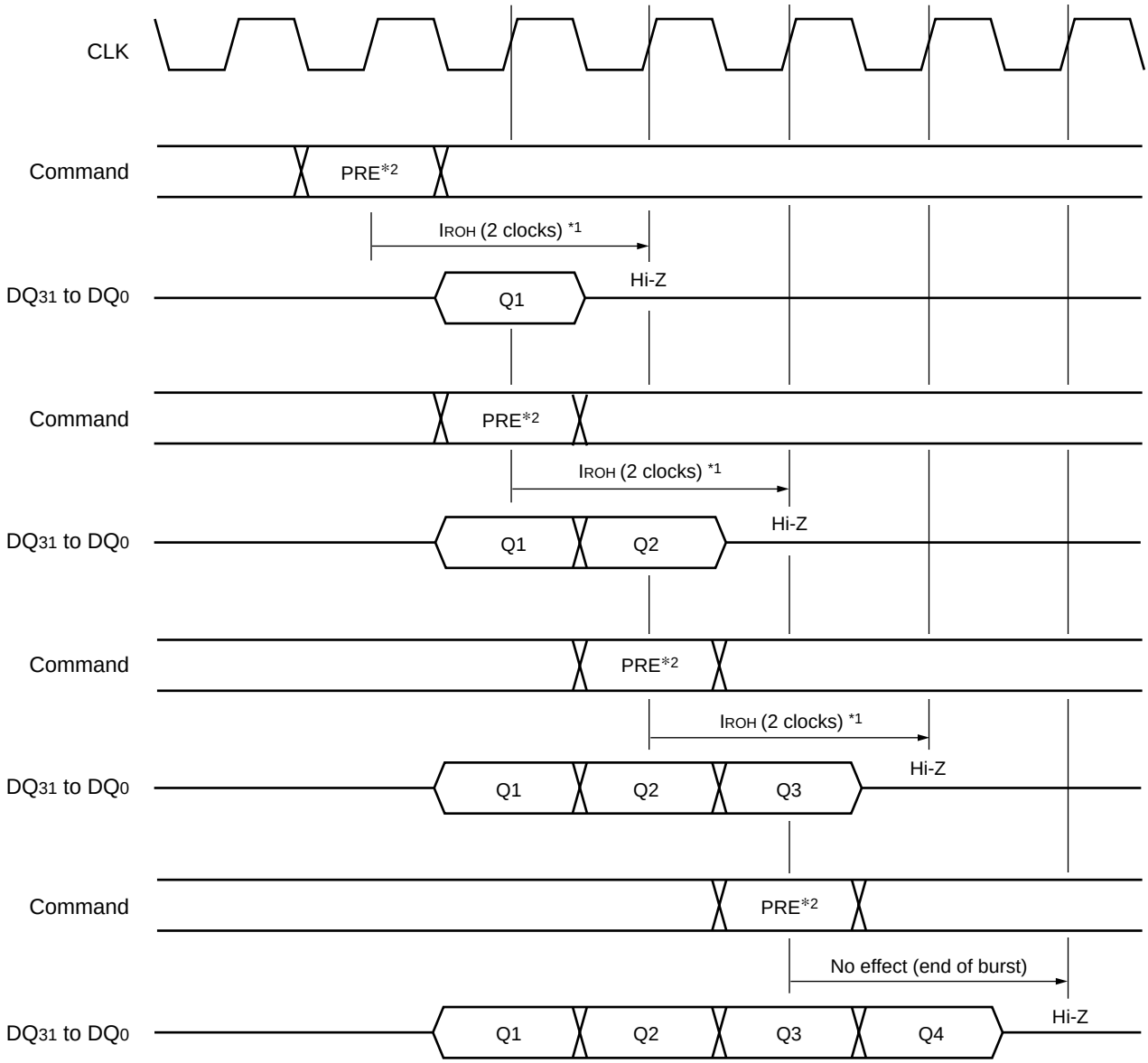


6. PRECHARGE TIMING (APPLIED TO THE SAME BANK)



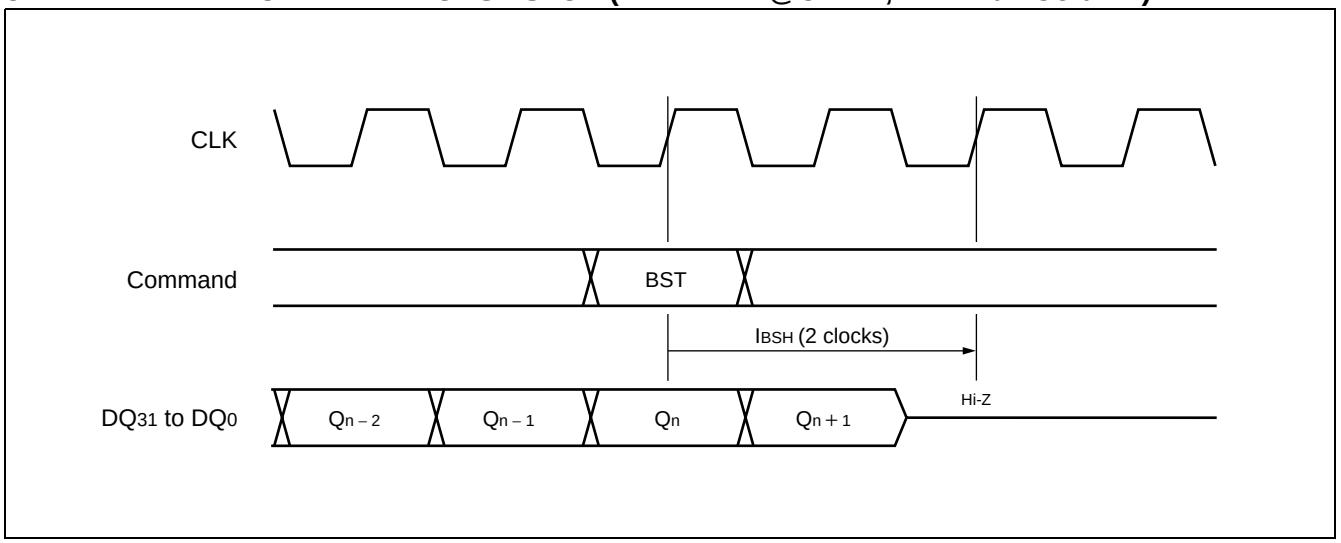
* : PRE means 'PRE' or 'PALL'.

7. READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4)

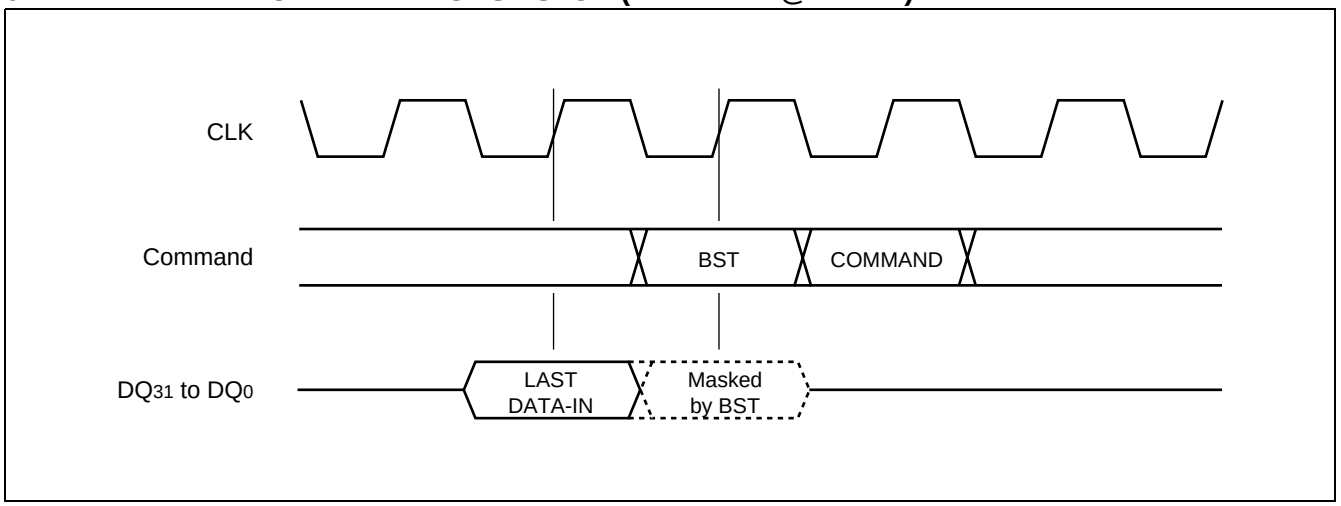


*1 : In case of CL = 2, the I_{ROH2} is 2 clocks.
*2 : PRE means 'PRE' or 'PALL'.

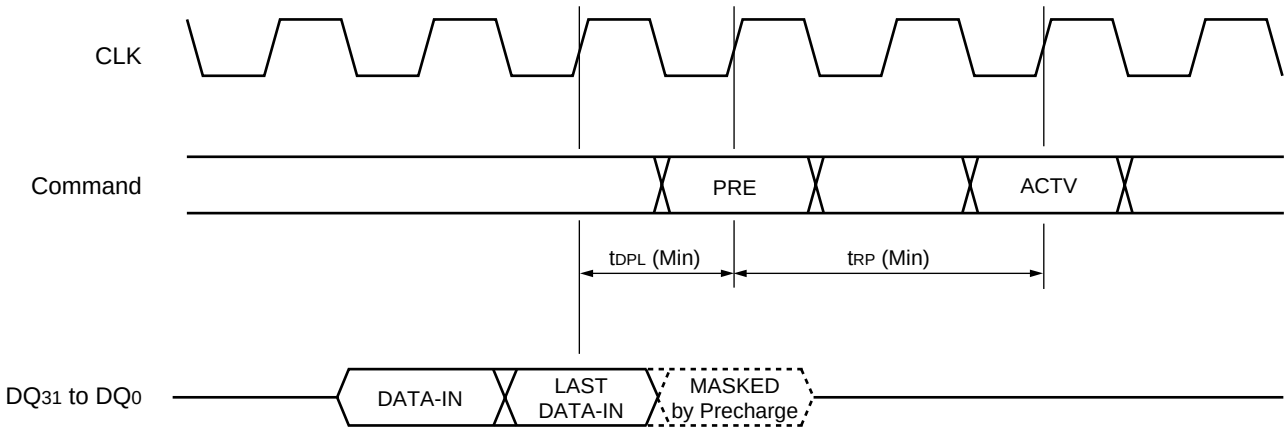
8. READ INTERRUPTED BY BURST STOP (EXAMPLE @CL = 2, BL = Full Column)



9. WRITE INTERRUPTED BY BURST STOP (EXAMPLE @ BL = 2)

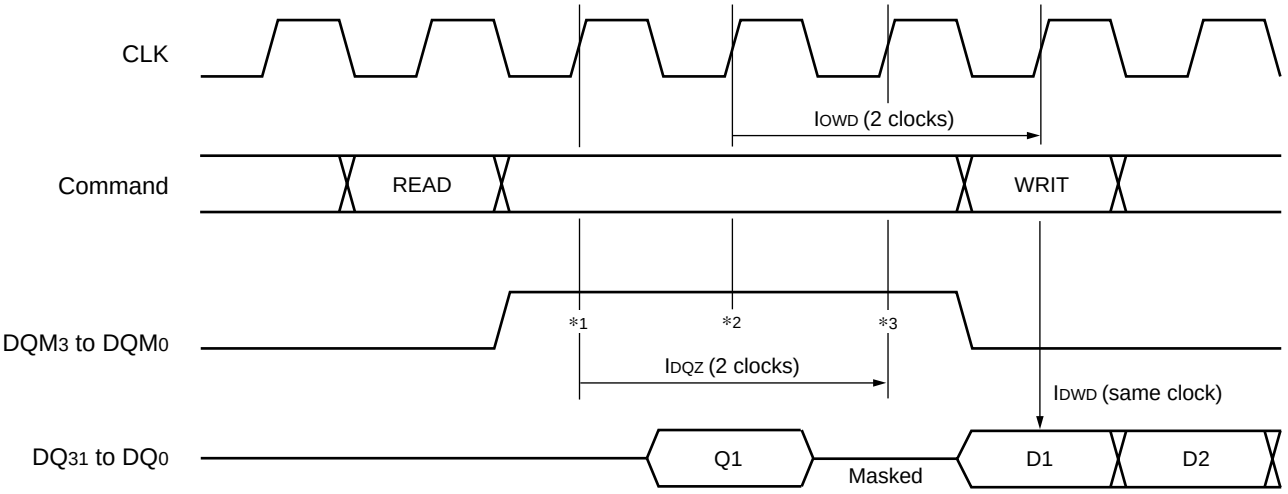


10. WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2)



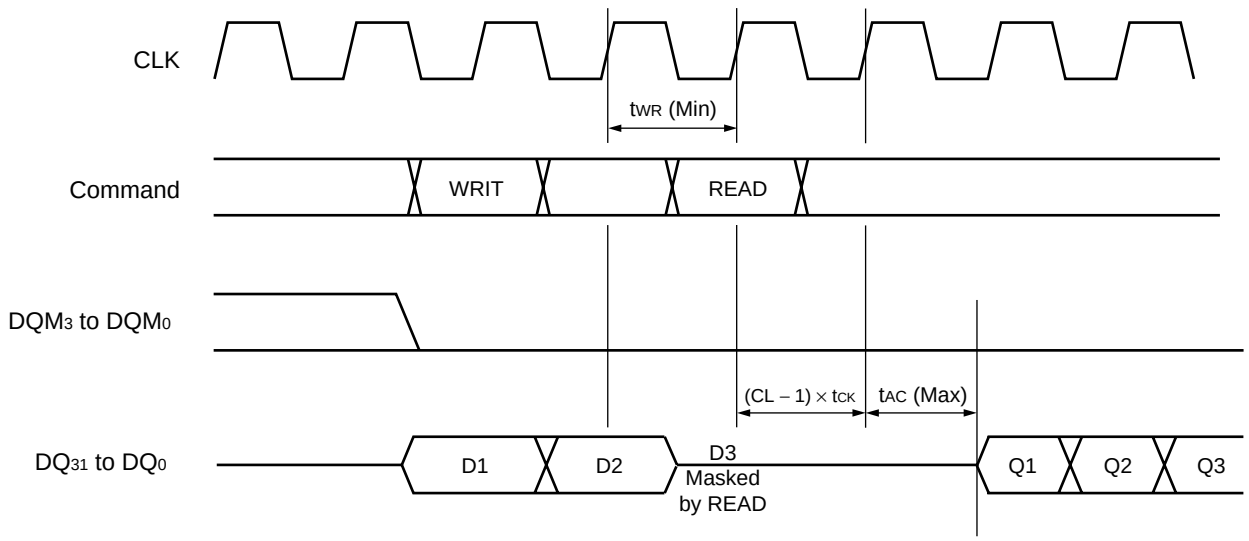
Note : The precharge command (PRE) should only be issued after the t_{DPL} of final data input is satisfied.
PRE means 'PRE' or 'PALL'.

11. READ INTERRUPTED BY WRITE (EXAMPLE @ CL = 2, BL = 4)



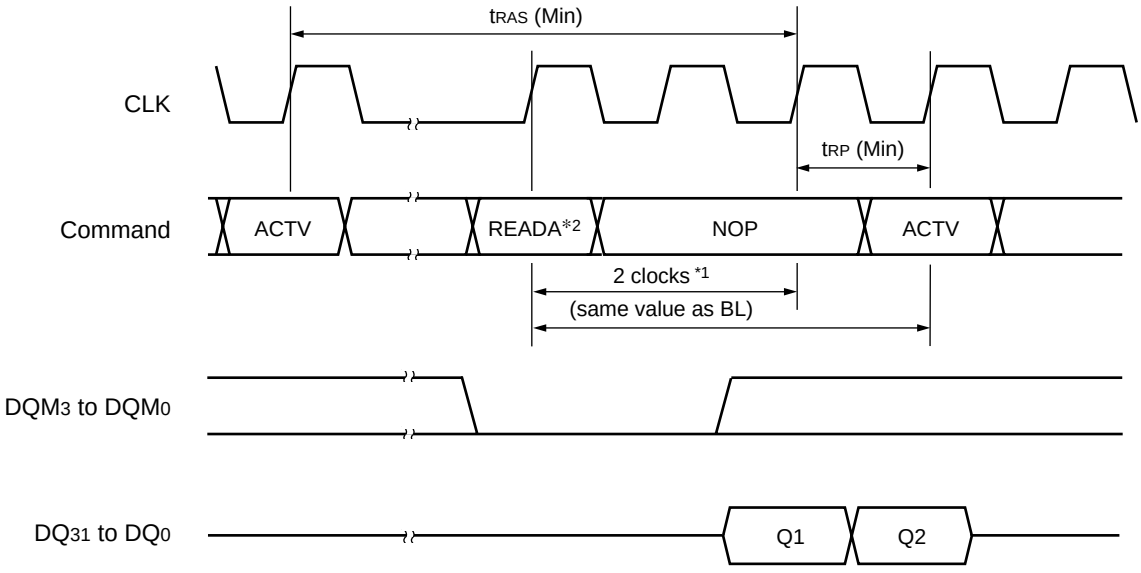
*1 : First DQM makes high-impedance state High-Z between last output and first input data.
*2 : Second DQM makes internal output data mask to avoid bus contention.
*3 : Third DQM also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

12. WRITE TO READ TIMING (EXAMPLE @ CL = 2, BL = 4)



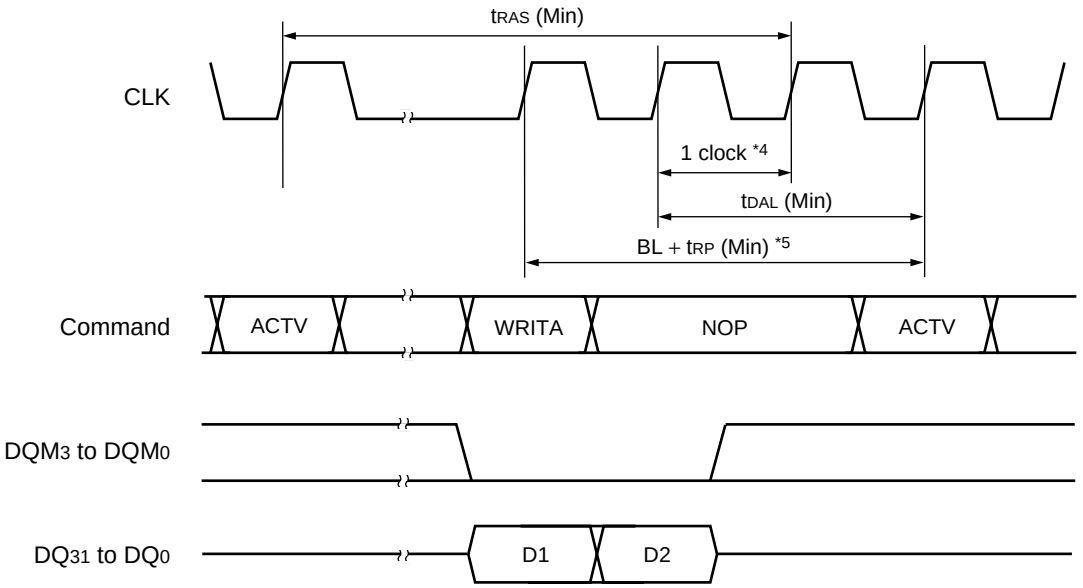
Note : Read command should be issued after t_{WR} of final data input is satisfied.

13. READ WITH AUTO-PRECHARGE (EXAPLE @ CL = 2, BL = 2, Applied to same bank)



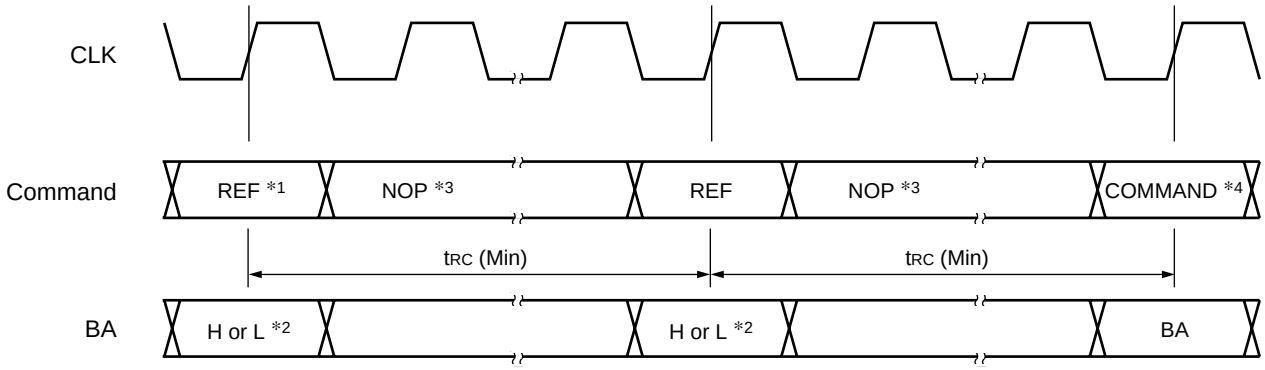
*1 : Precharge at read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after the READA command is asserted.
*2 : Next ACTV command should be issued after BL + t_{RP} (min) from READA command.

14. WRITE WITH AUTO-PRECHARGE (EXAMPLE @ CL = 2, BL = 2, Applied to same bank) *1, *2, *3



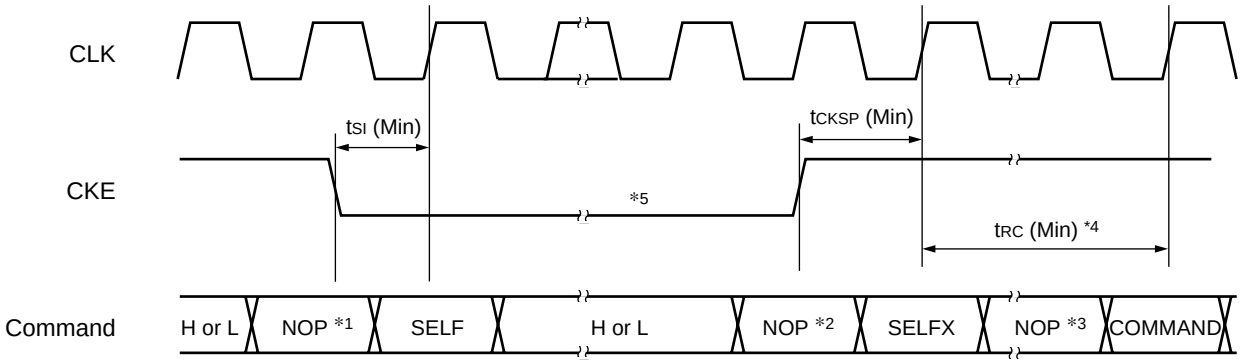
*1 : Even if the final data is masked by DQM, the precharge does not start the clock of final data input.
*2 : Once auto precharge command is asserted, no new command within the same bank can be issued.
*3 : Auto-precharge command doesn't affect at full column burst operation except Burst READ & Single Write.
*4 : Precharge at write with Auto-precharge is started after 1 clock at CL = 2 (-12) , 2 clock at CL = 2 (-12L) and CL = 3 from the end of burst.
*5 : Next command should be issued after BL + t_{RP} (min) at CL = 2 (-12) , BL + 1 + t_{RP} (min) at CL = 2 (-12L) and CL = 3 from WRITA command.

15. AUTO-REFRESH TIMING



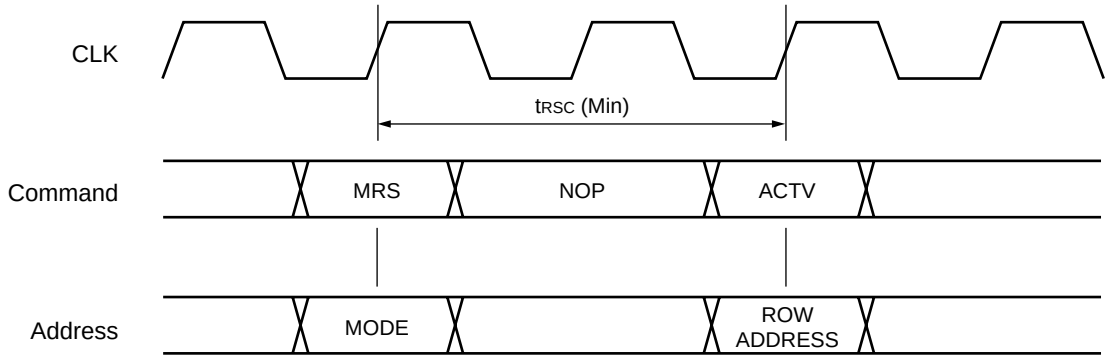
*1 : All banks should be precharged prior to the first Auto-refresh command (REF) .
*2 : Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.
*3 : Either NOP or DESL command should be asserted during t_{RC} period while Auto-refresh mode.
*4 : Any activation command such as ACTV or MRS command other than REF command should be asserted after t_{RC} from the last REF command.

16. SELF-REFRESH ENTRY AND EXIT TIMING



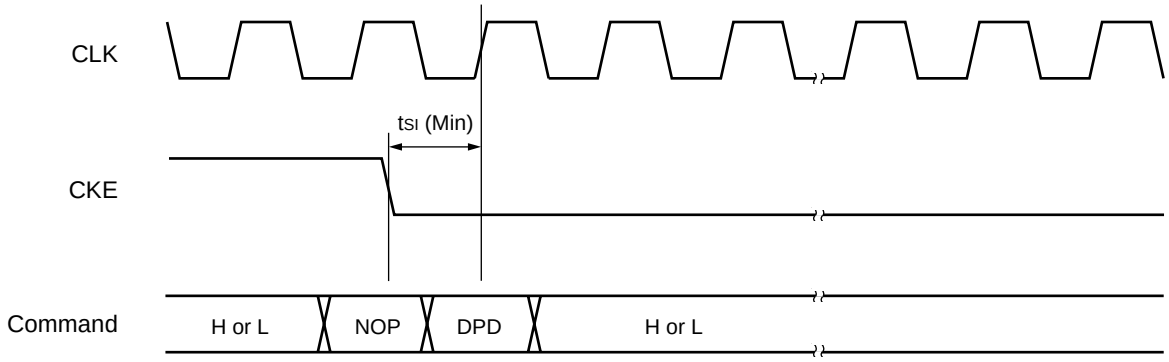
*1 : Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF) .
*2 : The Self-refresh Exit command (SELFX) is latched after t_{CKSP} (Min) . It is recommended to apply NOP command in conjunction with CKE.
*3 : Either NOP or DESL command can be used during t_{RC} period.
*4 : CKE should be held high within one t_{RC} period after t_{CKSP}.
*5 : CKE level should be held less than 0.2 V during self-refresh mode.

17. MODE REGISTER SET TIMING



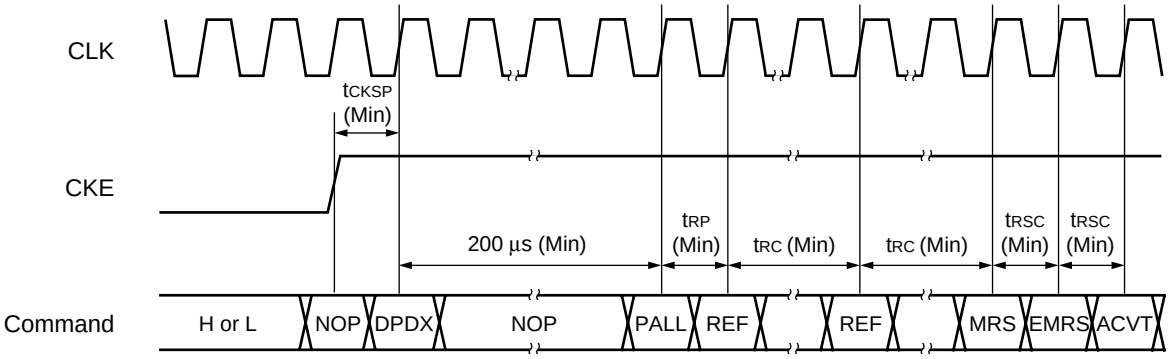
Note : The Mode Register Set command (MRS) should only be asserted after all banks have been precharged.

18. DEEP POWER DOWN ENTRY TIMING



Note : Deep Power Down Command (DPD) should only be asserted if all banks have been precharged and all outputs are in High-Z.

19. DEEP POWER DOWN EXIT TIMING



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