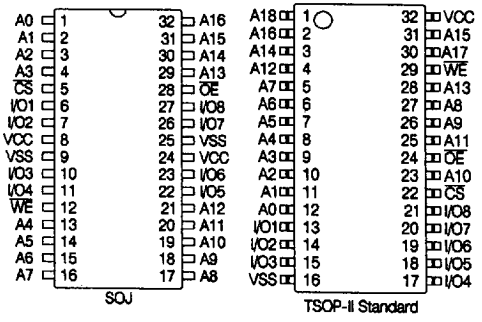
## DESCRIPTION

The HY63V8100 is a 1,048,576 -bits high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The HY63V8100 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using HYUNDAI's advanced CMOS process and designed for high-speed circuit technology. It is particulary well suited for use in high-density high-speed system applications.

## FEATURES

- **High speed - 20/25/30ns**
- **Low power consumption**
  - **-HY63V8100AS**
    - **Active : 100mA (max.)**
    - **Standby (TTL) : 35mA (max.)**
    - **(CMOS) : 1mA (max.)**
  - **-HY63V8100AL**
    - **Active : 100mA (max.)**
    - **Standby (TTL) : 35mA (max.)**
    - **(CMOS) : 50μA (max.)**
- **Single 3.3V±10% power supply**
- **TTL compatible inputs and outputs**
- **32 pin 400 mil SOJ (Revolutionary)**
- **32 pin 400 mil TSOP-II**

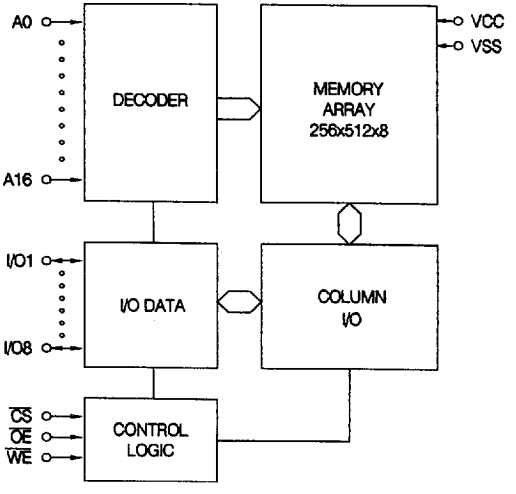
## PIN CONNECTION




## PIN DESCRIPTION

| Pin Name | Pin Function |
|---|---|
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| A0-A15 | Address Inputs |
| I/O1-I/O8 | Data Input/Output |
| Vcc | Power(+3.3V) |
| Vss | Ground |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$, $V_{IN}$, $V_{OUT}$ | Power Supply,Input/Output Voltage | -0.3 to 4.6 | V |
| $T_A$ | Operating Temperature | 0 to 70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -10 to 125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to 150 | °C |
| $P_D$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | Data Output Current | 50 | mA |
| $T_{SOLDER}$ | Lead Soldering Temperature & Time | 260 • 10 | °C • sec |

Note:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliablity.

## RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | - | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3[1] | - | 0.8 | V |

Note:
1. $V_{IL}$ = -3.0V for pulse width less than 10ns

## TRUTH TABLE

| MODE | I/O OPERATION | $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ |
|---|---|---|---|---|
| Standby | High-Z | H | X | X |
| Output Disabled | High-Z | L | H | H |
| Read | Data out | L | H | L |
| Write | Data in | L | L | X |

Note:
1. X= Don't Care

## DC CHARACTERISTICS

($T_A$ = 0°C to 70°C, $V_{CC}$ = 3.3V± 10%, unless otherwise specified.)

| SYMBOL | PARAMETER | TEST CONDITIONS | SPEED | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{SS} \le V_{IN} \le V_{CC}$ | | -1 | - | 1 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \le V_{OUT} \le V_{CC}$<br>$\overline{CS}$ = $V_{IH}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$ = $V_{IL}$ | | -1 | - | 1 | µA |
| $I_{CC1}$ | Average Operating Current | $\overline{CS}$ = $V_{IL}$, $I_{I/O}$ = 0mA<br>Min. Duty Cycle = 100% | 20ns | - | - | 100 | mA |
| | | | 25ns | - | - | 100 | mA |
| | | | 30ns | - | - | 90 | mA |
| $I_{SB}$ | TTL Standby Current (TTL Inputs) | $\overline{CS}$=$V_{IH}$,$V_{IN}$=$V_{IH}$ or $V_{IL}$, Min. Cycle | | - | - | 35 | mA |
| $I_{SB1}$ | CMOS Standby Current(CMOS Inputs) | $\overline{CS}$ ≥ $V_{CC}$ -0.2V,$V_{IN}$ ≥ $V_{CC}$-0.2V<br>or $V_{IN}$ ≤ 0.2V | | - | - | 1 | mA |
| | | | L | - | 20 | 50 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$= 8.0mA | | - | - | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$= - 4.0mA | | 2.4 | - | - | V |

Note:
1. Typical values are at $V_{CC}$=3.3V, T=25°C

## AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=3.3V ±10%, unless otherwise noted.)

| # | SYMBOL | PARAMETER | 20 | | 25 | | 30 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| | **READ CYCLE** | | | | | | | | |
| 1 | tRC | Read Cycle Time | 20 | - | 25 | - | 30 | - | ns |
| 2 | tAA | Address Access Time | - | 20 | - | 25 | - | 30 | ns |
| 3 | tACS | Chip Select Access Time | - | 20 | - | 25 | - | 30 | ns |
| 4 | tOE | Output Enable to Output Valid | - | 10 | - | 13 | - | 15 | ns |
| 5 | tCLZ | Chip Select to Low -Z Output | 5 | - | 5 | - | 5 | - | ns |
| 6 | tOLZ | Output Enable to Low-Z Output | 5 | - | 5 | - | 5 | - | ns |
| 7 | tCHZ | Chip Disable to High -Z Output | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| 8 | tOHZ | Output Disable to High -Z Output | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| 9 | tOH | Output Hold from Address Change | 5 | - | 5 | - | 5 | - | ns |
| | **WRITE CYCLE** | | | | | | | | |
| 10 | tWC | Write Cycle Time | 20 | - | 25 | - | 30 | - | ns |
| 11 | tCW | Chip Select to End of Write | 15 | - | 18 | - | 20 | - | ns |
| 12 | tAW | Address Valid to End of Write | 15 | - | 18 | - | 20 | - | ns |
| 13 | tAS | Address Set-up Time | 0 | - | 0 | - | 0 | - | ns |
| 14 | tWP | Write Pluse Width | 15 | - | 18 | - | 20 | - | ns |
| 15 | tWR | Write Recovery Time | 0 | - | 0 | - | 0 | - | ns |
| 16 | tWHZ | Write to High-Z Output | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| 17 | tDW | Data to Write Time Overlap | 12 | - | 15 | - | 17 | - | ns |
| 18 | tDH | Data Hold from Write Time | 0 | - | 0 | - | 0 | - | ns |
| 19 | tOW | Output Active from End of Write | 5 | - | 5 | - | 5 | - | ns |

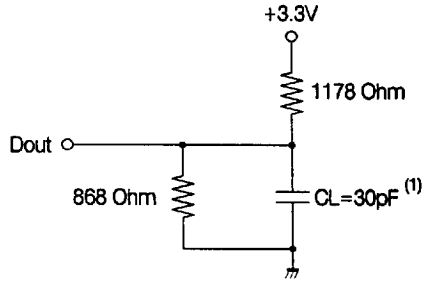
## AC TEST CONDITIONS

($T_A$=0°C to 70°C, $V_{CC}$=3.3V ±10%, unless otherwise specified.)

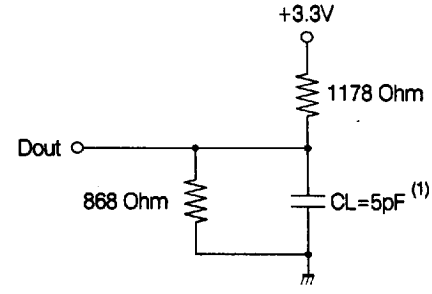
| PARAMETER | VALUE |
|---|---|
| Input Pulse Level | 0V to 2.8V |
| Input Rise and Fall Time | 3ns |
| Input and Output Timing Reference Levels | 1.4V |
| Output Load | See below |

## AC TEST LOADS

Output Load (A)




Output Load (B)
(for $t_{CHZ}$,$t_{CLZ}$,$t_{OLZ}$,$t_{OHZ}$,$t_{WHZ}$ & $t_{OW}$)




Note:
1. Including jig and scope capacitance.

## CAPACITANCE

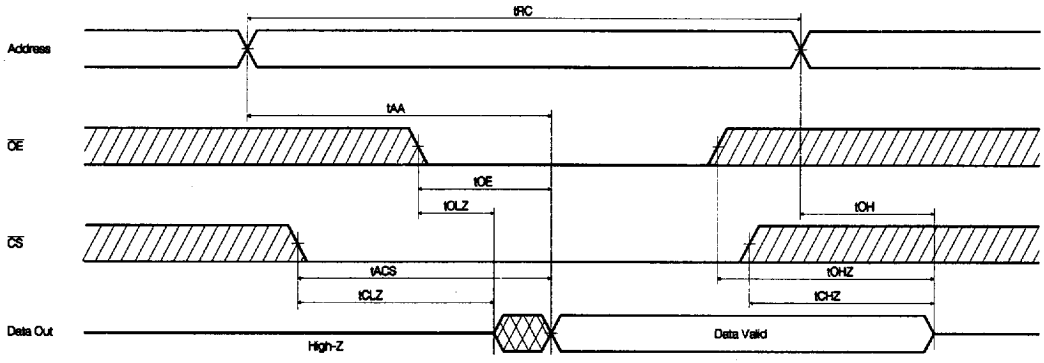
($T_A$=25°C, f= 1MHz)

| SYMBOL | PARAMETER | CONDITION | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$=0V | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{I/O}$=0V | 10 | pF |

Note:
1. This parameter is sampled and not 100% tested.

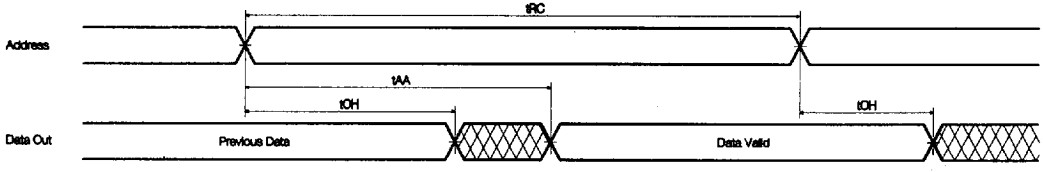
## TIMING DIAGRAM

### READ CYCLE1



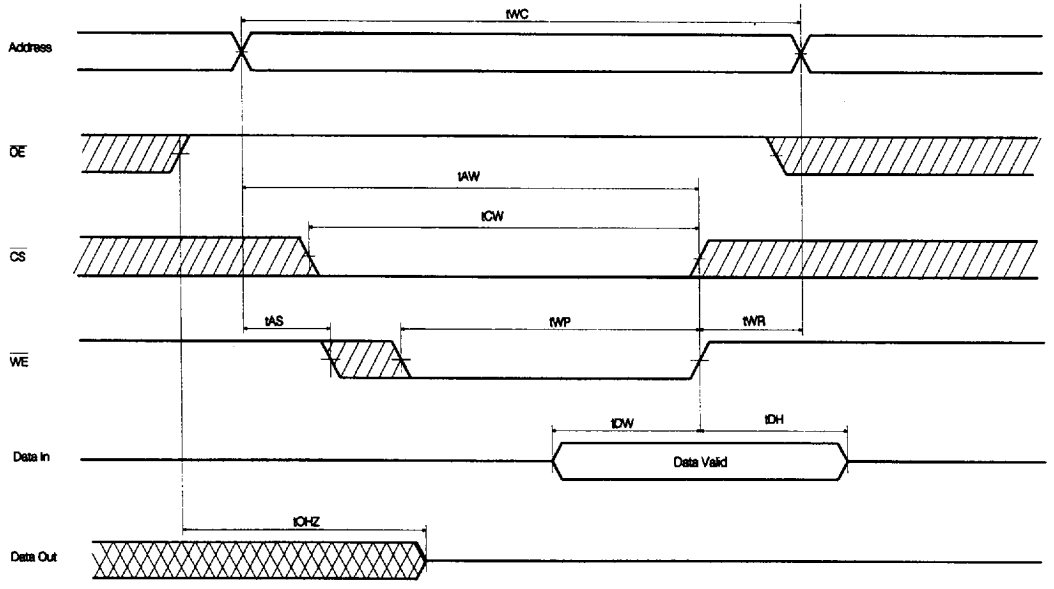

Note (READ CYCLE):
1. $t_{CHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{CHZ}$ max. is less than $t_{CLZ}$ min. both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

### READ CYCLE2

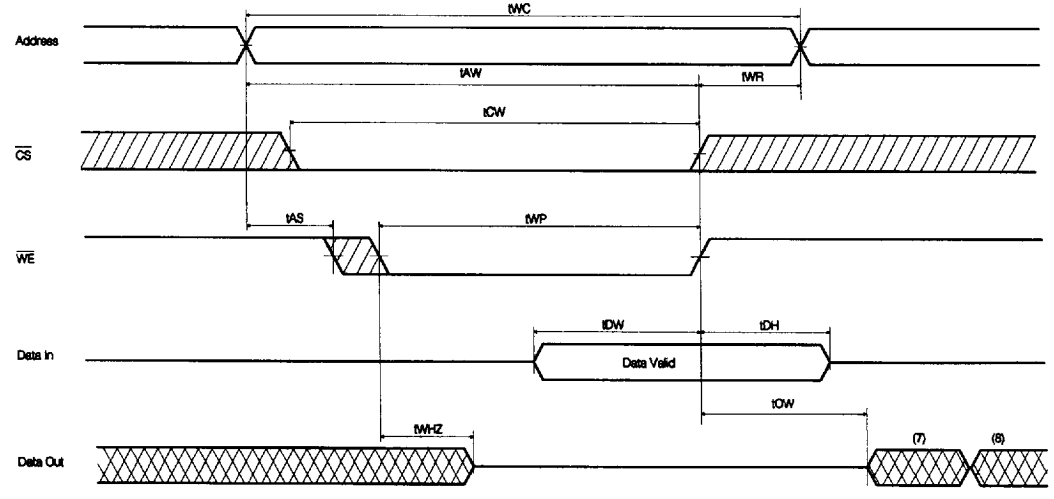



Note(READ CYCLE):
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS}$=$V_{IL}$.
3. $\overline{OE}$=$V_{IL}$.

**WRITE CYCLE 1 ($\overline{OE}$ Low Clocked)**




**WRITE CYCLE 2 ($\overline{OE}$ Low Fixed)**



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low, and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high. $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the later of $\overline{CS}$ going low to end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
5. If $\overline{OE}$ and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. $D_{OUT}$ is the same phase of lastest written data in this write cycle.
8. $D_{OUT}$ is the read data of the new address.

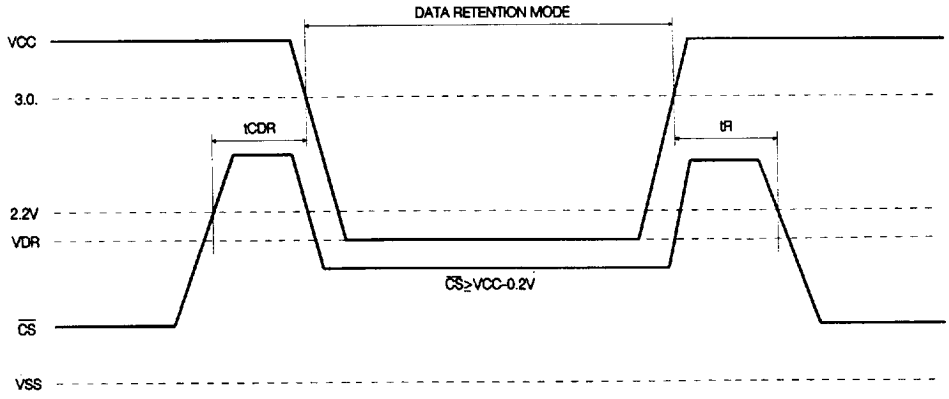
## DATA RETENTION CHARACTERISTICS (L Version)

($T_A$=0°C to 70°C)

| SYMBOL | PARAMETER | TEST CONDITION | POWER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | $\overline{CS} \geq V_{CC}$-0.2V<br>$V_{SS} \leq V_{IN} \leq V_{CC}$ | | 2.0 | - | - | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$=3.0V<br>$\overline{CS} \geq V_{CC}$-0.2V<br>$V_{SS} \leq V_{IN} \leq V_{CC}$ | L | - | 10 | 50 | µA |
| $t_{CDR}$ | Chip Disable to Data Retention Time | See Data Retention Timing Diagram | | 0 | - | - | ns |
| $t_R$ | Operating Recovery Time | | | $t_{RC}$(2) | - | - | ns |

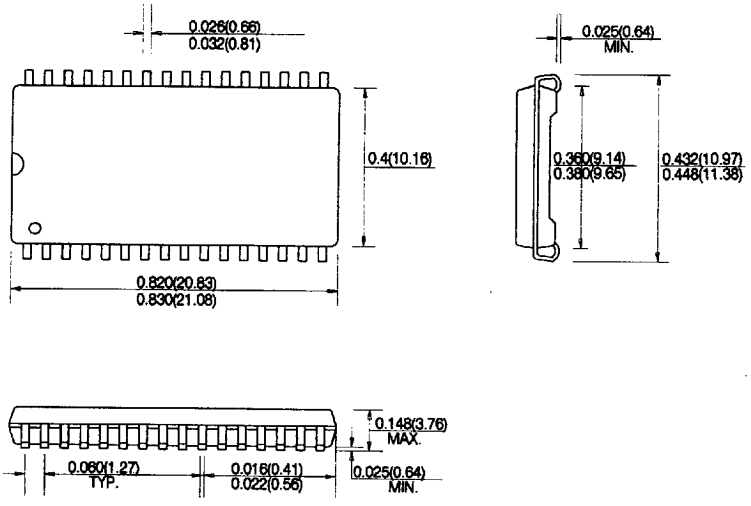
Notes:
1. Typical values are at the condition of $T_A$=25°C.
2. $t_{RC}$ is read cycle time.

## DATA RETENTION TIMING DIAGRAM 1

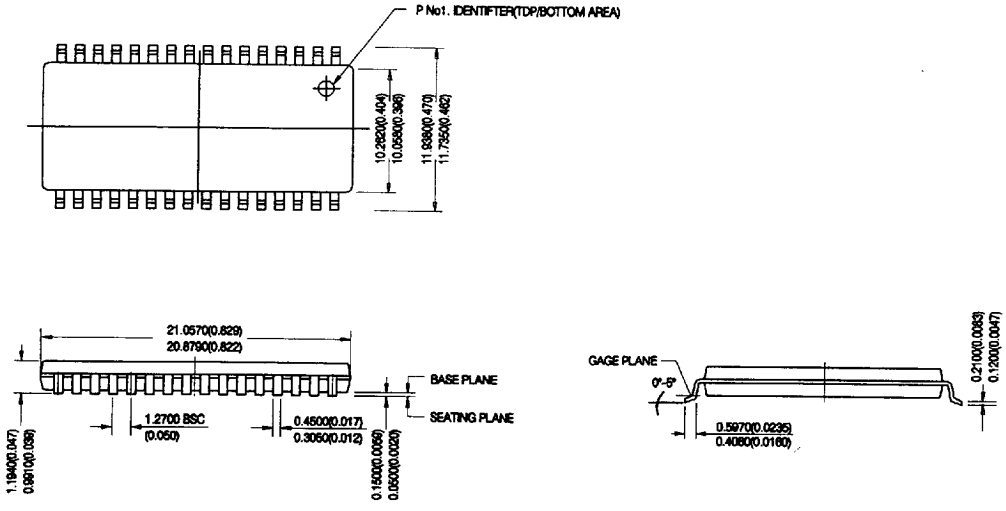


## PACKAGE INFORMATION

### 400 mil 32 pin Small Outline J-Form Package (J)




### 400 mil 32 pin Plastic Thin Small Outline Package (T2)



## ORDERING INFORMATION

| PART NO. | SPEED | POWER | PACKAGE |
|---|---|---|---|
| HY63V8100AJ | 20/25/30 | | SOJ |
| HY63V8100ALJ | 20/25/30 | L-part | SOJ |
| HY63V8100AT2 | 20/25/30 | | TSOP-II |
| HY63V8100ALT2 | 20/25/30 | L-part | TSOP-II |
| HY63V8100AR2 | 20/25/30 | | TSOP-II(R) |
| HY63V8100ALR2 | 20/25/30 | L-part | TSOP-II(R) |