

## DESCRIPTION

The HY514403B is the new generation and fast dynamic RAM organized 1,048,576 x 4-bit. The HY514403B has four CASs(CAS0-3) which control corresponding data I/O port in conjunction with OE(eg. CAS0 controls DQ0, CAS1 controls DQ1, CAS2 controls DQ2 and CAS3 controls DQ3). The HY514403B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY514403B to be packaged in a standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V ±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

- Low power dissipation  
 Max. battery back-up 1.65mW (L-part)  
 Max. CMOS standby 1.1mW (L-part)  
 5.5mW  
 Max. TTL standby 11mW  
 Max. Self Refresh 1.1mW(SL-part)  
 Max. operating

Speed	Power
50	550.0mW
60	495.0mW
70	440.0mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access and cycle time

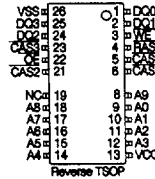
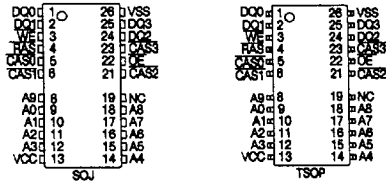
Speed	t <sub>TRAC</sub>	t <sub>CAC</sub>	t <sub>PC</sub>
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Fast page mode operation
- Four independent CAS controls
- Multi-bit test capability
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden & Self Refresh capability
- 1024 refresh cycles / 128ms (L-part)  
 1024 refresh cycles / 16ms

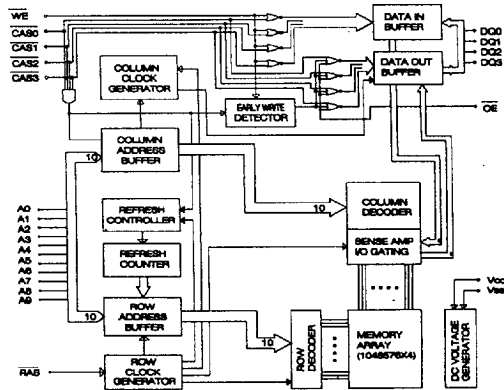
## PIN DESCRIPTION

RAS	Row Address Strobe
CAS 0-3	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A9	Address input
DQ0-DQ3	Data Output/Output
Vcc	Power (+5V)
Vss	Ground

## PIN CONNECTION



## BLOCK DIAGRAM



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**ABSOLUTE MAXIMUM RATING**

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	0.90	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE: All Voltage are referenced to Vss.

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**DC CHARACTERISTICS**

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TES CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	Vss ≤ VIN ≤ 6.5V All other pins not under test = Vss		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	Vss ≤ VOUT ≤ 5.5V RAS & CAS at VIH		-10	10	μA	
ICC1	Vcc Supply Current, Operating	trc = trc (min.)	50	-	100	mA	1,2,3
			60	-	90		
			70	-	80		
ICC2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ Vss		-	2	mA	
ICC3	Vcc Supply Current, RAS-only refresh	trc = trc (min.)	50	-	100	mA	1,3
			60	-	90		
			70	-	80		
ICC4	Vcc Supply Current, Fast Page mode	tPC = tPC (min.)	50	-	70	mA	1,2,3
			60	-	60		
			70	-	50		
ICC5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc-0.2V	L-part	-	1	mA	5
				-	200		
ICC6	Vcc Supply Current, CAS-before- RAS refresh	trc = trc (min.)	50	-	100	mA	1,3
			60	-	90		
			70	-	80		
ICC7	Vcc Supply Current, Battery Back up (L-part only)	trc = 125μs, trAS ≤ 1μs CAS = CBR cycling or 0.2V OE & WE = Vcc-0.2V, A0 - A9 = Vcc-0.2V or 0.2V DQ0-DQ3 = 0.2V, Vcc-0.2V or open		-	300	μA	1,4,5
ICC8	Vcc Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	200	μA	6
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

**NOTE :**

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rates.
2. ICC1, ICC3, ICC4 and ICC6 are dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS =VIL. ICC4, Address can be changed maximum once while CAS=VIH.
4. Only trAS(max.)=1μs is applied to refresh of battery backup but trAS(max.)=10μs is applied to normal functional operation .
5. ICC5(max.)=200 μA and ICC7 are applied to L-parts (HY514403BLJ, HY514403BLT, HY514403BLR, HY514403BSLJ, HY514403BSLT, HY514403BSLR.)
6. ICC8 is applied to SL-parts only (HY514403BSLJ, HY514403BSLT and HY514403BSLR.)

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**AC CHARACTERISTICS**

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.) NOTE1,2,3,13

#	SYMBOL	PARAMETER	HY514403B/J/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE	
			- 50		- 60		- 70				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns		
2	tRWC	Read-Modify-Write Cycle Time	130	-	155	-	185	-	ns		
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns		
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns		
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10	
6	tCAC	Access Time from CAS	-	15	-	15	-	20	ns	4,9	
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10	
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4,15	
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4	
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5	
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3	
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns		
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns		
14	tRASP	RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns		
15	tRSH	RAS Hold Time	15	-	15	-	20	-	ns		
16	tCSH	CAS Hold Time	50	-	60	-	70	-	ns		
17	tCAS	CAS Pulse width	15	10K	20	10K	20	10K	ns		
18	tRCD	RAS to CAS Delay	15	35	20	45	20	50	ns	9	
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10	
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	17	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns		
23	tRAH	Row Address Hold time	8	-	10	-	10	-	ns		
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14	
26	tAR	Column Address Hold Time from RAS	45	-	50	-	55	-	ns		
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns		
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6,14	
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6	
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	14	
32	tWCR	Write Command Hold Time from RAS	40	-	45	-	55	-	ns		
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns		
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	20	-	ns		
35	tCWL	Write Command to CAS Lead Time	15	-	15	-	20	-	ns	16	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7	
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7	
38	tDHR	Data-In Hold Time Referenced to RAS	40	-	45	-	55	-	ns		
39	tREF	Refresh Period (1024 cycles)		-	16	-	16	-	16	ms	12
			L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set up Time	0	-	0	-	0	-	ns	8,14	

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY514403BJ/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to $\overline{WE}$ Delay Time	35	-	40	-	50	-	ns	8
42	tRWD	RAS to $\overline{WE}$ Delay Time	70	-	85	-	100	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	45	-	55	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	CAS Precharge Time (CBR Counter Test)	20	-	20	-	25	-	ns	17
48	tROH	RAS Hold Time Referenced to $\overline{OE}$	-	10	-	10	-	10	ns	
49	tOEA	$\overline{OE}$ Access Time	-	15	-	15	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	20	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	20	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from CAS Precharge	50	-	55	-	65	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	$\overline{WE}$ to RAS Precharge Time(CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to RAS Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time	10	-	10	-	10	-	ns	
59	tRASS	RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	$\mu$ s	
60	tRPS	RAS Precharge Time (Self Refresh)	120	-	130	-	150	-	ns	
61	tCHS	CAS Hold Time from RAS (Self Refresh)	- 50	-	- 50	-	- 50	-	ns	

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**AC CHARACTERISTICS IN TEST MODE**

NOTE 18

#	SYMBOL	PARAMETER	HY514403BJ/BT/BR/BLJ/BLT/BLR/ BSLJ/BSLT/BSLR						UNIT	NOTE
			- 50		- 60		- 70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	135	-	155	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	85	-	100	-	ns	
5	tRAC	Access Time from $\overline{\text{RAS}}$	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from $\overline{\text{CAS}}$	-	20	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{\text{CAS}}$ Precharge	-	35	-	40	-	45	ns	4
13	tRAS	$\overline{\text{RAS}}$ Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	$\overline{\text{RAS}}$ Hold Time	20	-	20	-	25	-	ns	
16	tCSH	$\overline{\text{CAS}}$ Hold Time	55	-	65	-	75	-	ns	
17	tCAS	$\overline{\text{CAS}}$ Pulse Width	20	10K	20	10K	25	10K	ns	
27	tRAL	Column Address to $\overline{\text{RAS}}$ Lead Time	30	-	35	-	40	-	ns	
41	tCWD	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	40	-	40	-	50	-	ns	8
42	tRWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	75	-	85	-	100	-	ns	8
43	tAWD	Column Address to $\overline{\text{WE}}$ Delay Time	50	-	55	-	65	-	ns	8
49	tOEA	$\overline{\text{OE}}$ Access Time	-	20	-	20	-	25	ns	
50	tOED	$\overline{\text{OE}}$ to Data Delay	20	-	20	-	25	-	ns	
52	tOEH	$\overline{\text{OE}}$ Command Hold Time	20	-	20	-	25	-	ns	

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**NOTE:**

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle before proper device operation is achieved.
2. If  $\overline{\text{RAS}}=\text{Vss}$  during power-up, the HY514403B could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $\text{Vcc}$  during power-up or be held at a valid  $\text{VIH}$  in order to minimize the power-up current
3.  $\text{VIH}(\text{min.})$  and  $\text{VIL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $\text{VIH}(\text{min.})$  and  $\text{VIL}(\text{max.})$ , and are assumed to be 5ns for all inputs.
4. Measured at  $\text{VOH}=2.4\text{V}$  and  $\text{VOL}=0.4\text{V}$  with a load equivalent to 2 TTL loads and 100pF.
5.  $\text{tOFF}(\text{max.})$  and  $\text{tOEZ}$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either  $\text{trCH}$  or  $\text{trRH}$  must be satisfied for a read cycle.
7. These parameters are referenced to  $\overline{\text{CAS0}}$ ,  $\overline{\text{CAS1}}$ ,  $\overline{\text{CAS2}}$ , and  $\overline{\text{CAS3}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in Read-Modify-Write cycles.
8.  $\text{twCS}$ ,  $\text{trWD}$ ,  $\text{tcWD}$ ,  $\text{tAWD}$  and  $\text{tcpWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $\text{twCS} \geq \text{twCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If  $\text{trWD} \geq \text{trWD}(\text{min.})$ ,  $\text{tcWD} \geq \text{tcWD}(\text{min.})$ ,  $\text{tAWD} \geq \text{tAWD}(\text{min.})$ , and  $\text{tcpWD} \geq \text{tcpWD}(\text{min.})$ , the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the  $\text{trCD}(\text{max.})$  limit insures that  $\text{trAC}(\text{max.})$  can be met.  $\text{trCD}(\text{max.})$  is specified as a reference point only. If  $\text{trCD}$  is greater than the specified  $\text{trCD}(\text{max.})$  limit, then access time is controlled by  $\text{tcAC}$ .
10. Operation within the  $\text{trAD}(\text{max.})$  limit insures that  $\text{trAC}(\text{max.})$  can be met.  $\text{trAD}(\text{max.})$  is specified as a reference point only. If  $\text{trAD}$  is greater than the specified  $\text{trAD}(\text{max.})$  limit, then access time is controlled by  $\text{tAA}$ .
11.  $\text{tREF}(\text{max.})=128\text{ms}$  is applied to L-Parts(HY514403BLJ/BSLJ, HY514403BLT/BSLT and HY514403BLR/BSLR).
12. A burst of 1024  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles must be executed within 16ms(128ms for L-part) after exiting self refresh.
13. When all of four  $\overline{\text{CAS}}$ s go low at the same time, all 4-bits data are written into the device.  $\overline{\text{CAS}}$ s must be transitioned simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of  $\overline{\text{CAS}}$ .
15. These parameters are determined by the later rising edge of  $\overline{\text{CAS}}$ .
16.  $\text{tcwl}$  must be satisfied by all of four  $\overline{\text{CAS}}$ s for 4-bits access cycles.
17.  $\text{tcp}$  and  $\text{tcPT}$  are measured when all of four  $\overline{\text{CAS}}$ s is high state.
18. These specificaitons are applied to the test Mode.

**CAPACITANCE**

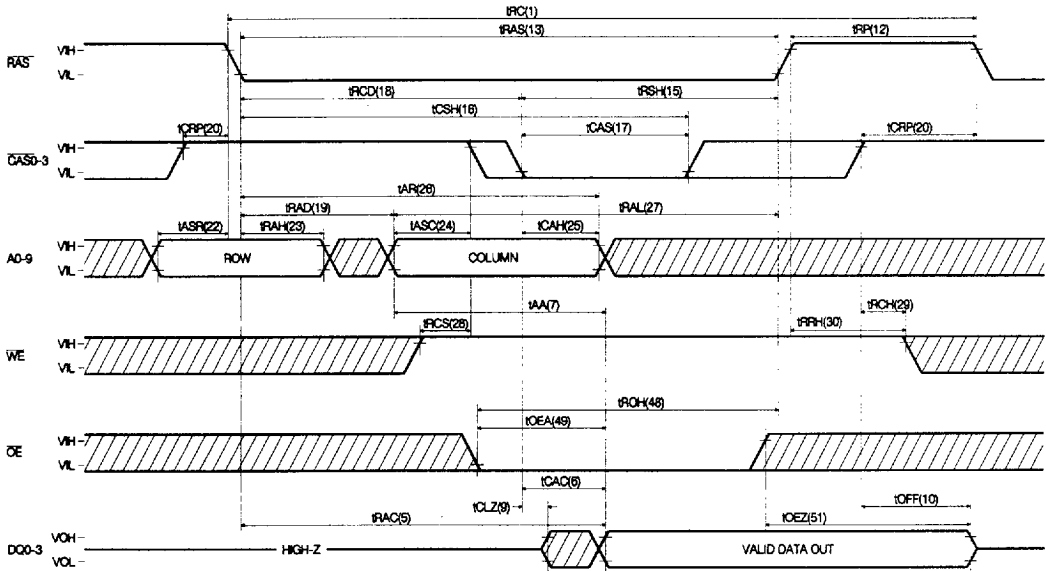
( $\text{TA}=25^\circ\text{C}$ ,  $\text{Vcc}=5\text{V} \pm 10\%$ ,  $\text{Vss}=0\text{V}$ ,  $f=1\text{MHz}$ , unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	-	7	pF
CDQ	Data Input/output Capacitance (DQ0-DQ3)	-	7	pF

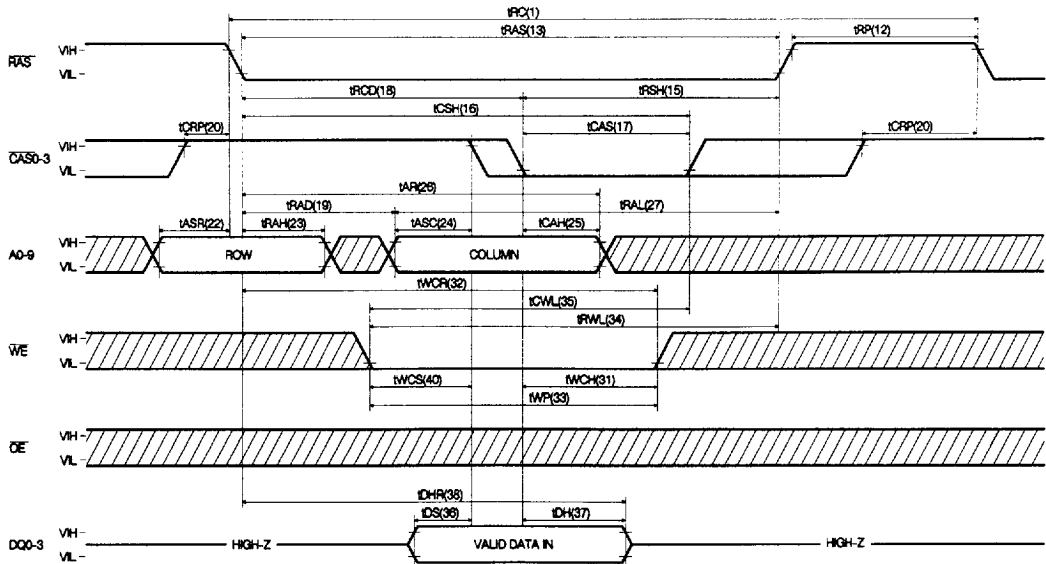
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**TIMING DIAGRAM**

**READ CYCLE**



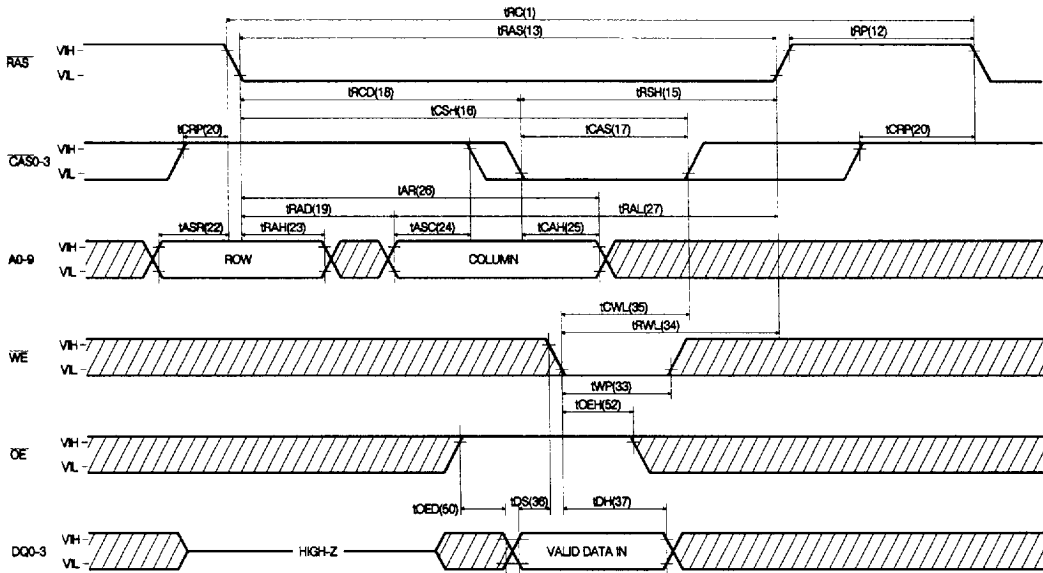
**EARLY WRITE CYCLE**



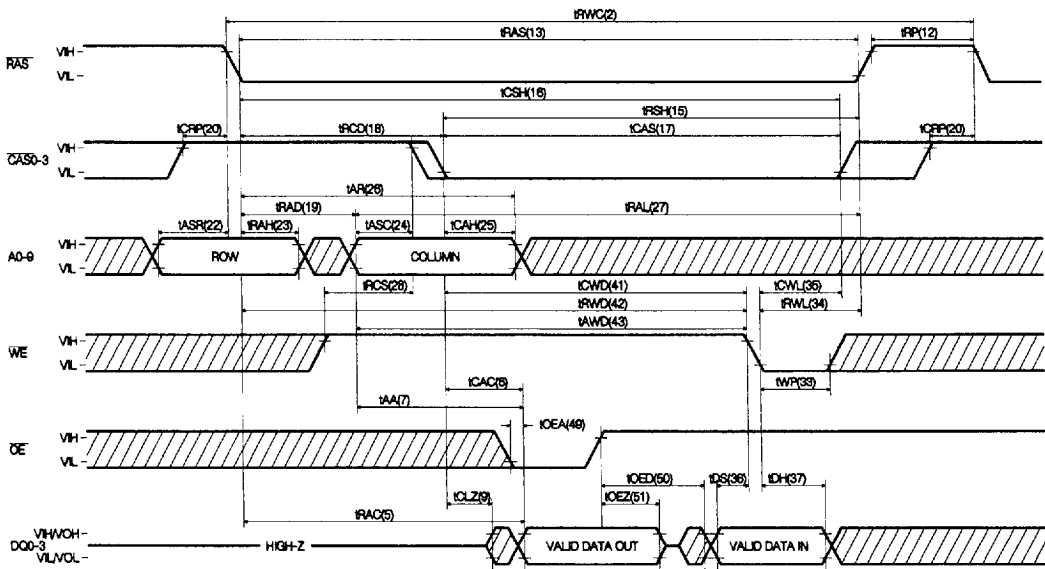
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**WRITE CYCLE ( $\overline{OE}$  CONTROLLED WRITE)**



**READ-MODIFY-WRITE CYCLE**

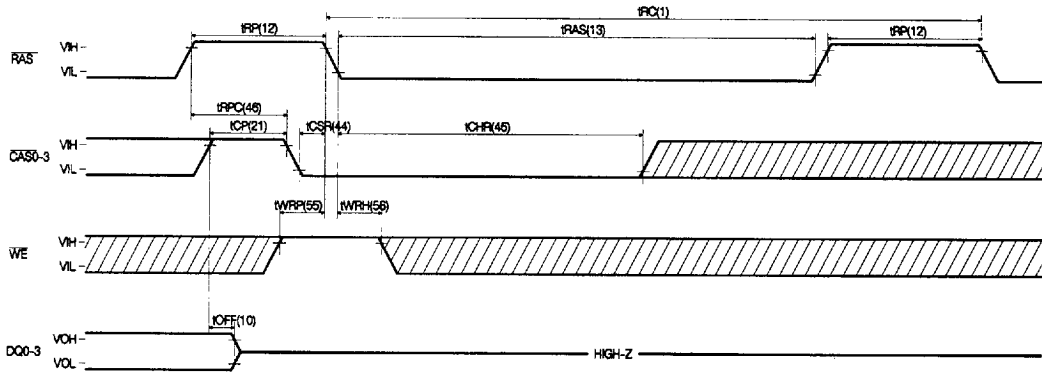


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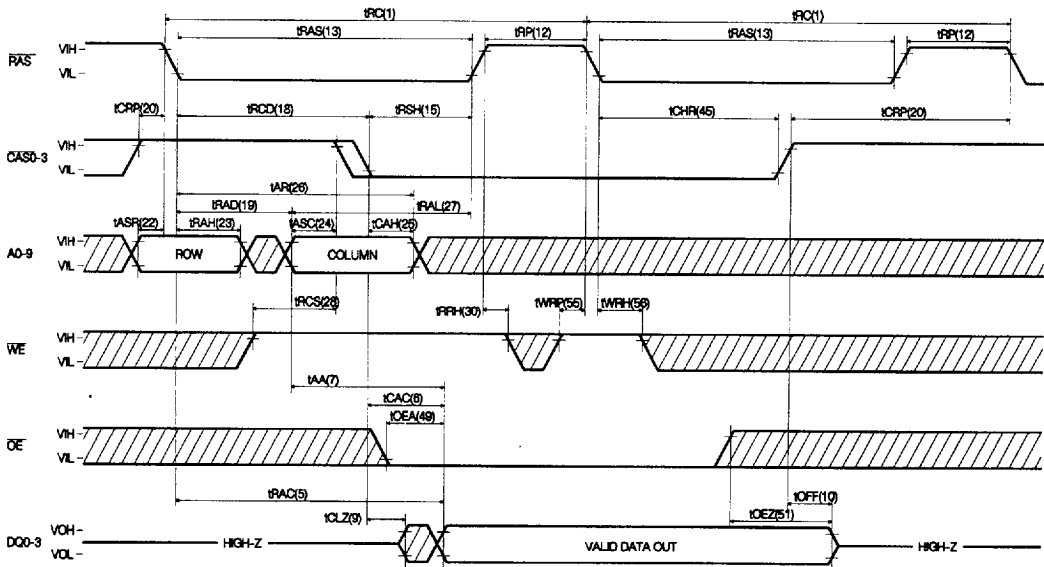


CAS-BEFORE-RAS REFRESH CYCLE



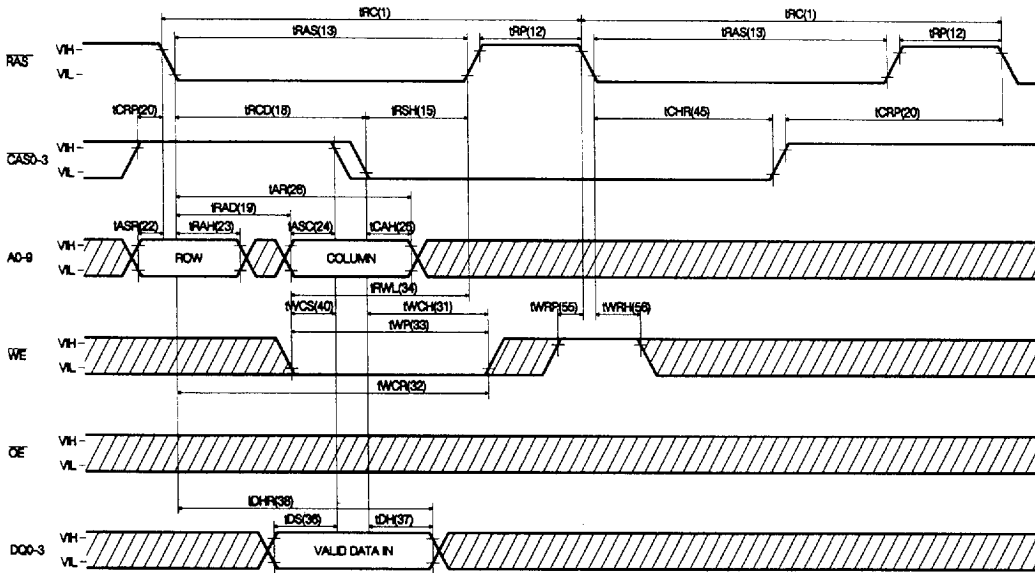
NOTE : A0-A9 and OE = "H" OR "L"

HIDDEN REFRESH CYCLE (READ)

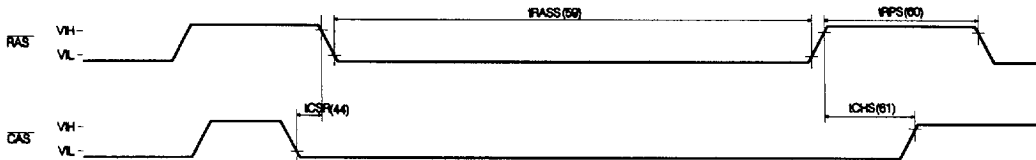


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HIDDEN REFRESH CYCLE (WRITE)



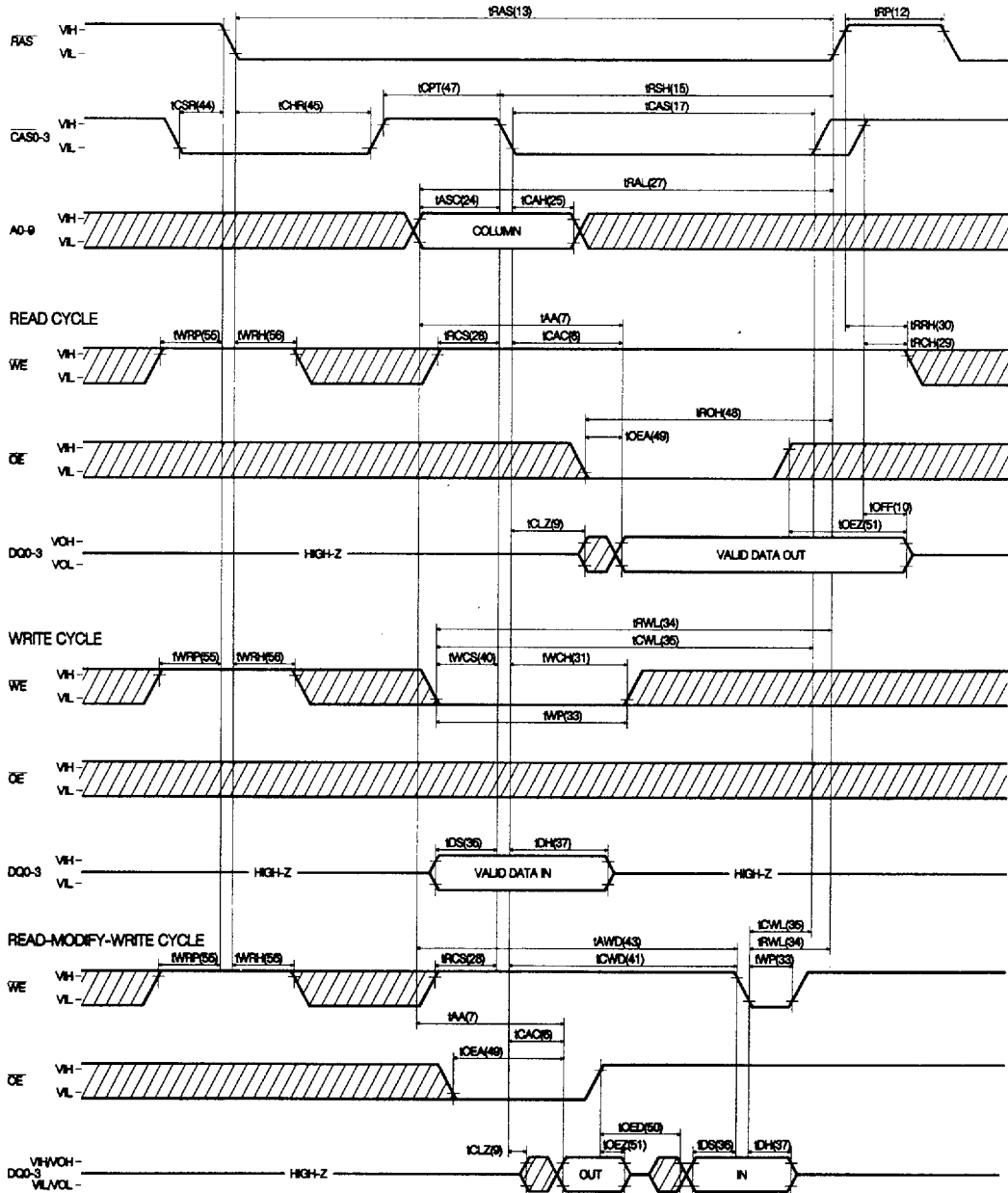
CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE:A0-9, WE and OE = 'H' or 'L'

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**CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE**

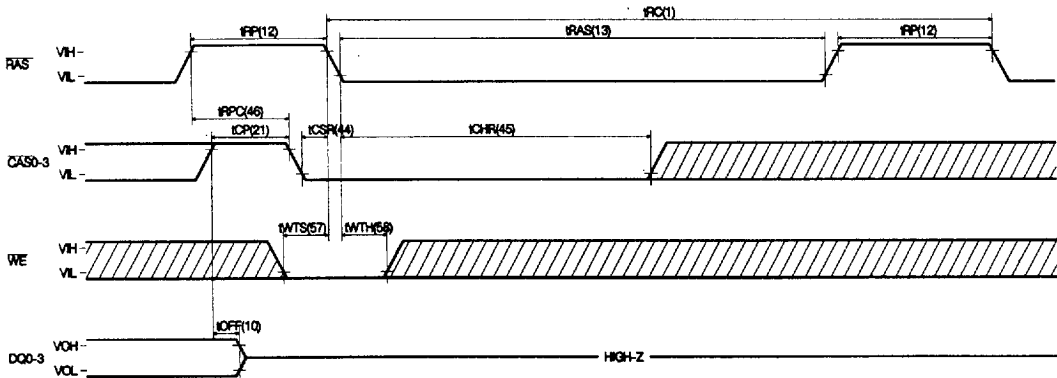


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TEST MODE

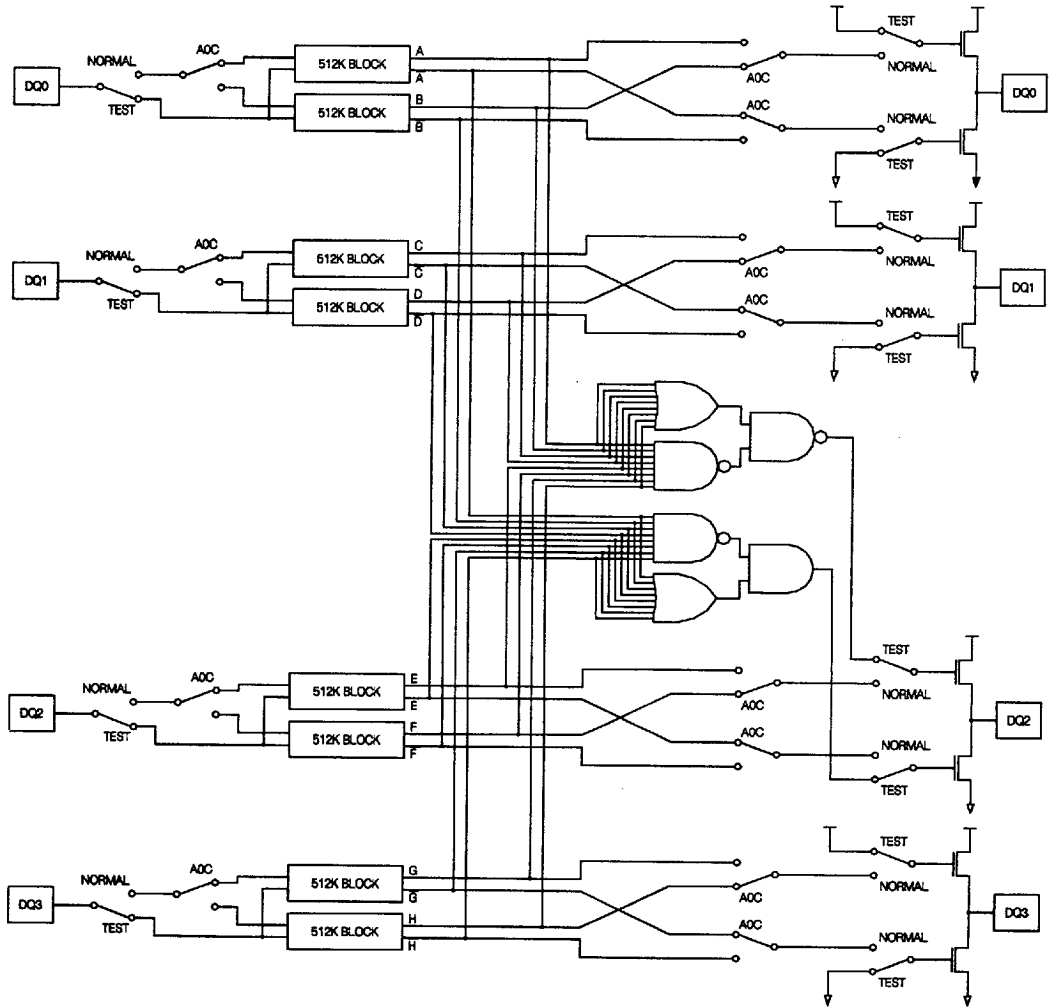
The HY514403B is a DRAM organized 1,048,576 x 1-bit. It is internally organized 524,288 x 8-bit. In Test Mode, data are written into 8 sectors (Each is composed of 512K bits) in parallel and retrieved the same way. Column address A0 is not used. If, upon reading, all 8-bit data from 8 sectors are equal (all "1"s or "0"s), the DQ2 pin indicates a "1". If they are not equal, the DQ2 pin indicates a "0". The DQ0, DQ1 and DQ3 pins always indicate a "1" in Test Mode Read cycles. The diagram below shows the timing of the HY514403B to enter Test Mode. In Test Mode, the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. WE, CAS-before-RAS cycle (Test Mode in Cycle) puts the HY514403B into Test Mode and CAS-before-RAS or RAS-only refresh cycle puts it back into Normal Mode. In Test Mode, WE, CAS-before-RAS cycle shall be used for the refresh operation. The Test Mode function reduces test time. (1/2 in case of N test pattern)

TEST MODE IN CYCLE



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BLOCK DIAGRAM IN TEST MODE

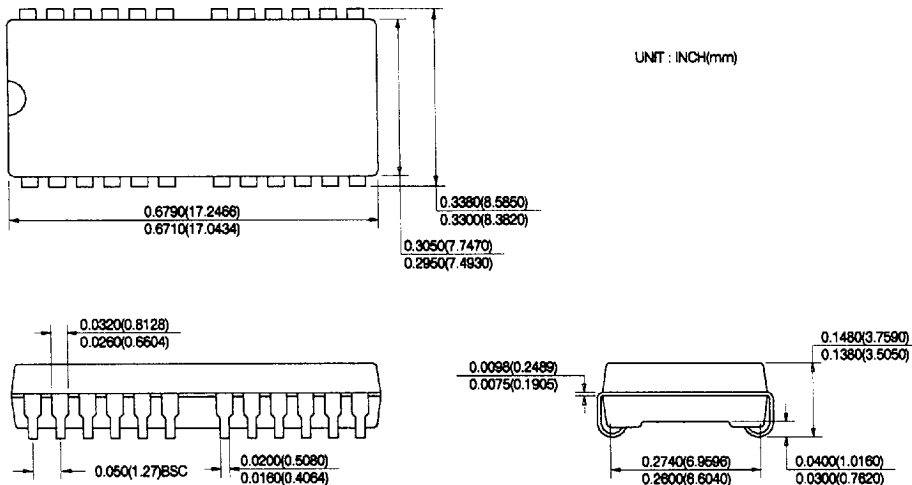


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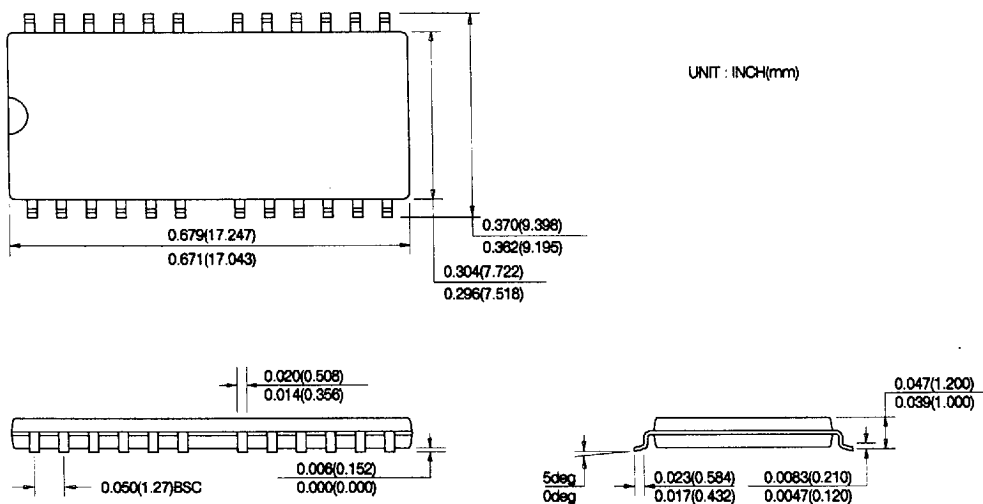


**PACKAGE INFORMATION**

**300 mil 24/26 pin Small Outline J-form Package (J)**



**300 mil 24/26 pin Thin Small Outline Package (T) (R)**



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**ORDERING INFORMATION**

<b>PART NUMBER</b>	<b>SPEED</b>	<b>POWER</b>	<b>PACKAGE</b>
HY514403BJ	50/60/70		SOJ
HY514403BLJ	50/60/70	L-part	SOJ
HY514403BSLJ	50/60/70	SL-part	SOJ
HY514403BT	50/60/70		TSOP-II
HY514403BLT	50/60/70	L-part	TSOP-II
HY514403BSLT	50/60/70	SL-part	TSOP-II
HY514403BR	50/60/70		TSOP-II(R)
HY514403BLR	50/60/70	L-part	TSOP-II(R)
HY514403BSLR	50/60/70	SL-part	TSOP-II(R)

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