RICMOS™ GATE ARRAYS

HR2000
FAMILY

FEATURES

- Fabricated on Honeywell's Radiation Hardened 0.65 μm_{Leff} RICMOS™ IV Bulk Process

- Array Sizes from 10K to 336K Available Gates (Raw)

- TTL or CMOS Compatible I/O

- Full Complement of Screening Flows

- Configurable Multi-Port Gate Array SRAM

- Modular Custom Drop-In SRAM Capability

- Supports System Speeds Beyond 75 MHz

- Total Dose Hardness $\geq 1 \times 10^6$ rad(SiO_2)

- Dose Rate Upset Hardness $\geq 1 \times 10^9$ rad(Si)/sec

- Dose Rate Survivability $\geq 1 \times 10^{12}$ rad (Si)/sec

- Soft Error Rate $\leq 1 \times 10^{-10}$ Errors/Bit/Day

- Neutron Fluence Hardness to 1×10^{14}/cm^2

- No Latchup

- Supports 5V Operation

GENERAL DESCRIPTION

The HR2000 gate arrays are performance oriented sea-of-transistor arrays, fabricated on Honeywell's 0.65 μm RICMOS™ IV bulk CMOS process. The high density and performance characteristics of the RICMOS (Radiation Insensitive CMOS) process make possible device operation beyond 75 MHz over the full military temperature range, even after exposure to ionizing radiation exceeding 1×10^6 rad(SiO_2). Flip-Flops have been designed for a Soft Error Rate (SER) of less than 1×10^{-10} errors/bit/day in the Adams 90% worst case environment.

Each HR2000 design is founded on our proven RICMOS ASIC library of SSI and MSI logic elements, configurable RAM cells and selectable I/O pads. The gate arrays feature a global clock network capable of handling multiple clock signals with low clock skew between registers. This family is fully compatible with Honeywell's high reliability screening procedures and consistent with QML Class Q and V requirements.

Designers can choose from a wide variety of I/O types. Output buffer options include 5 drive strengths, CMOS/TTL levels, IEEE 1149.1 boundary scan, pull-up/pull-down resistors, and three-state capability. Input buffers can be selected with CMOS/TTL/Schmitt trigger levels,

IEEE 1149.1 boundary scan and pull-up/pull-down resistors. Bi-directional buffers are also available.

The HR2000 family provides options for configurable multi-port SRAMs. Word widths can be selected in single bit increments. A variety of SRAM read and write port options are available to serve most applications. Custom drop-in macrocells can also be implemented to further increase chip density.

Logic designers need not have prior experience in radiation hardening. Honeywell's VDS™ Toolkit and RICMOS IV libraries provide the necessary guidance to achieve first pass design success. The VDS Toolkit supports industry standard platforms including those offered by Mentor Graphics and Synopsys.

Honeywell can perform design translations to the HR2000 arrays from other CAD platforms. Our synthesis capabilities allow customers to use familiar CAD tools and libraries to map the design to Honeywell library components.

The HR2000 family of gate arrays is the right choice for your high reliability applications demanding high density and radiation performance. To learn more about Honeywell's variety of space components, call us at 612-954-2888.

HR2000

HR2000 Characteristics	HR2010	HR2065	HR2090	HR2125	HR2210	HR2340
Total Core Gate Count	10K	68K	92K	126K	207K	336K
Usable Gate Count	7K	40K	52K	67K	103K	158K
Maximum Die I/O	72	176	220	252	314	372
Maximum Package I/O (1)	60	172	220	216	256	320
Typical Delay—2 Input NAND	350 ps at 5.0V					
Selectable I/O	Driver, Receiver, Bi-Directional, Three-State					
I/O Interface Levels	CMOS, TTL, Schmitt Trigger					
Typical Power Dissipation	0.65 µW/Gate/MHz, @ 5.0V					
Operating Voltage	5V ± 10%					
Operating Temperature	-55° C to 125° C					
Process Technology	RICMOS™ IV					
Minimum Geometry	0.65 µm Leff / 0.8 µm Drawn					

(1) Design and package dependent

**To learn more about Honeywell Solid State Electronics Center, visit our web site at
http://www.ssec.honeywell.com**

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