

DESCRIPTION:

The DPS256S8P/PL/PLL is a 256K x 8 high-density, low-power static RAM module comprised of two 128K x 8 monolithic SRAM's, an advanced high-speed CMOS decoder and decoupling capacitors surface mounted on a co-fired ceramic substrate having side-brazed leads.

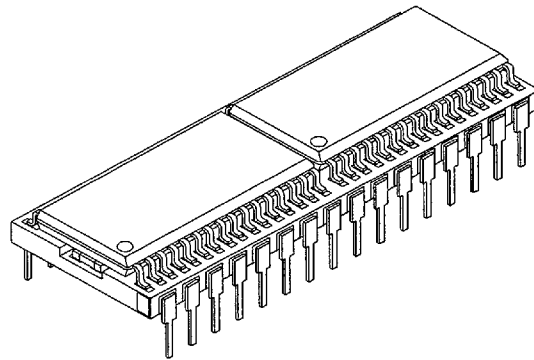
The DPS256S8P/PL/PLL is available in a 600-mil-wide, 32-pin dual-in-line package that conforms to the same JEDEC standard pin configuration as the future four megabit monolithics.

The DPS256S8P/PL/PLL operates from a single +5V supply and all input and output pins are completely TTL-compatible. The low standby power of the DPS256S8P/PL/PLL makes it ideal for battery-backed applications.

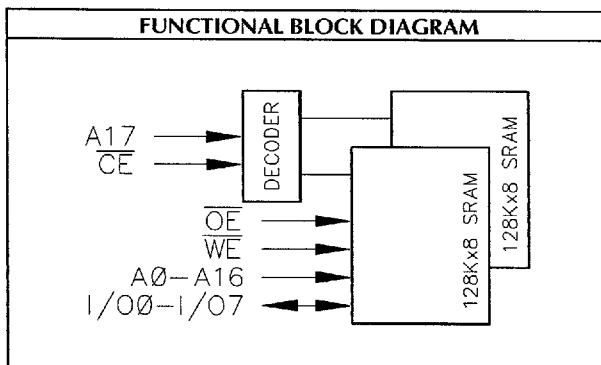
FEATURES:

- 262,144 by 8 Bit Configuration
- Access Times: 70*, 85, 100, 120, 150ns
- Low Power Dissipation:
 - 15 μ W (typ.) Standby (DPS256S8PL/DPS256S8PLL)
 - 20 μ W (typ.) Standby (DPS256S8P)
 - 275 mW (typ.) Operating
- 2-Volt Data Retention
- Fully Static Operation - No Clock or Refresh Required
- All inputs and Outputs are TTL-Compatible
- 600 mil, 32-pin JEDEC Standard DIP Pinout

* Available in Commercial only.



PIN NAMES	
A0 - A17	Address Inputs
I/O0 - I/O7	Data In/Out
\overline{CE}	Chip Enable
\overline{WE}	Write Enable
\overline{OE}	Output Enable
V _{DD}	Power (+5V)
V _{SS}	Ground
N.C.	No Connect



PIN-OUT DIAGRAM			
N.C.	1	32	VDD
A16	2	31	A15
A14	3	30	A17
A12	4	29	\overline{WE}
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	\overline{OE}
A2	10	23	A10
A1	11	22	\overline{CE}
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
VSS	16	17	I/O3

RECOMMENDED OPERATING RANGE ¹						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V _{DD}	Supply Voltage	4.5	5.0	5.5	V	
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V	
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V	
T _A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	

TRUTH TABLE					
Mode	CE	WE	OE	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	DOUT	Active
Write	L	L	X	DIN	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -1.0mA	2.4	-	V
V _{OL}	LOW Voltage	I _{OL} = 2.1mA		0.4	V

ABSOLUTE MAXIMUM RATINGS ³				
Symbol	Parameter	Max.	Unit	
T _{STC}	Storage Temperature	-55 to +125	°C	
T _{BIAS}	Temperature Under Bias	-10 to +85	°C	
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	V	
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V	

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	25	pF	V _{IN} = 0V
C _{CE}	Chip Enable	20		
C _{WE}	Write Enable	25		
C _{OE}	Output Enable	25		
C _{VO}	Data Input/Output	35		

DC OPERATING CHARACTERISTICS: Over operating ranges								
Symbol	Characteristics	Test Conditions	TYP.	COMMERCIAL		INDUSTRIAL †		Unit
				Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-	-5	+5	-5	+5	µA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-	-5	+5	-5	+5	µA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	P	25	45	50	50	mA
			PL	25	45	50	50	
			PLL	25	35	40	40	
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100%, I _{OUT} = 0mA	P	70	100	100	100	mA
			PL	55	95	95	95	
			PLL	35	75	75	75	
I _{SB1}	Full Standby Supply Current	V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V, CE ≥ V _{DD} -0.2V	P	4	200	300	300	µA
			PL	3	100	150	150	
			PLL	3	50	100	100	
I _{SB2}	Standby Current	CE = V _{IH} , V _{IN} = V _{IH} or V _{IN}	P	2	6	6	6	mA
			PL	2	4	5	5	
			PLL	2	3	4	4	
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA	-	0.4		0.4	0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	-	2.4		2.4	2.4	V

† Not available in 70ns.

DATA RETENTION CHARACTERISTICS									
Symbol	Parameter	Test Conditions	Typ.	COMMERCIAL		INDUSTRIAL †		Unit	
				Min.	Max.	Min.	Max.		
V _{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DR} - 0.2V$	-	2.0	5.5	2.0	5.5	V	
ICCDR2	Data Retention Supply Current	V _{DR} = 2.0V	P	2		90		135	μA
			PL	2		40		60	
			PLL	1		20		30	
ICCDR3	Data Retention Supply Current	V _{DR} = 3.0V	P	2		100		150	μA
			PL	2		50		75	
			PLL	1		25		40	
t _{CDR}	Chip Disable to Data Retention Time		-	0		0		ns	
t _R	Recovery Time	t _{RC} = Read Cycle Timing		5		5		ms	

† Not Available in 70ns.

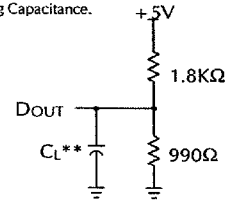
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input and Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

Output Load		
Load	C _L	Parameters Measured
1	100pF	except t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WHZ} , and t _{WLZ}
2	5pF	t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WHZ} , and t _{WLZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



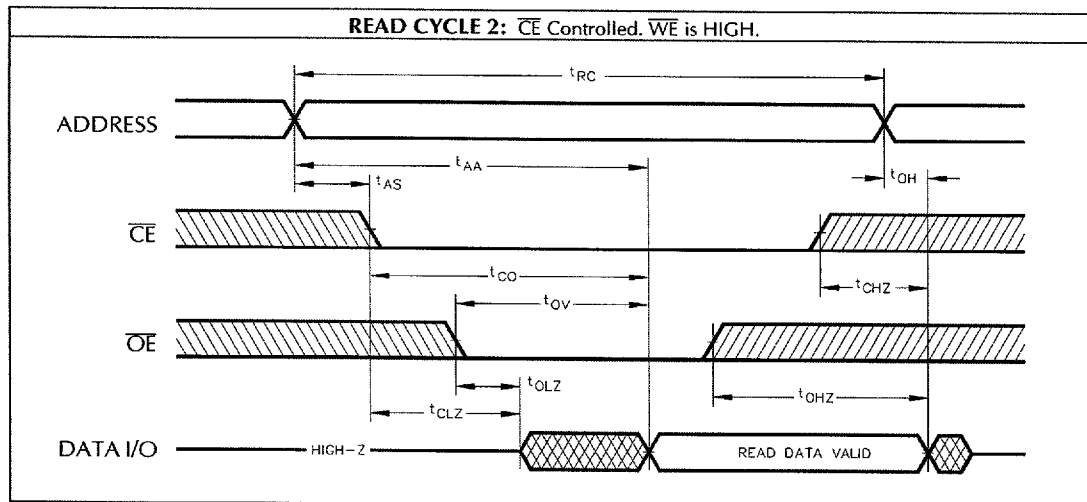
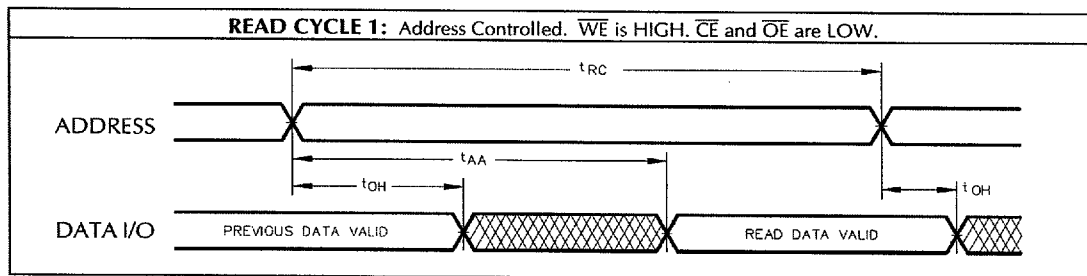
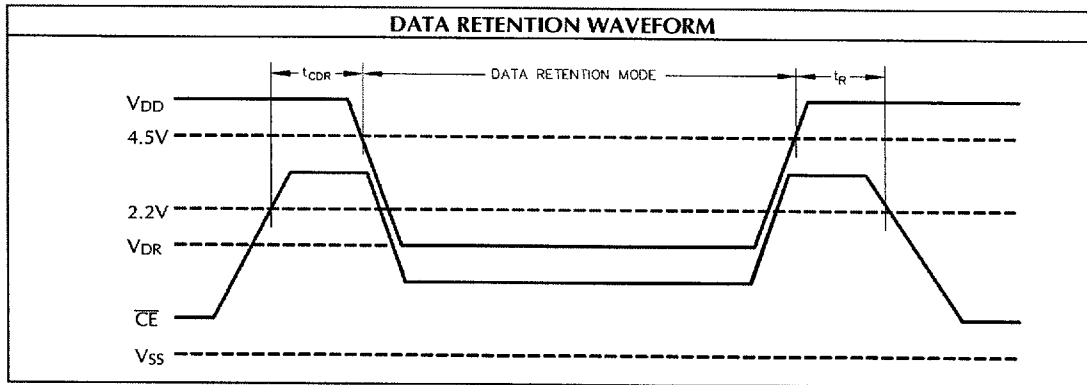
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	70ns ††		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	70		85		100		120		150		ns
2	t _{AA}	Address Access Time		70		85		100		120		150	ns
3	t _{CO}	Chip Enable to Output Valid		70		85		100		120		150	ns
4	t _{OV}	Output Enable to Output Valid		45		45		45		50		60	ns
5	t _{OH}	Output Hold from Address Change	10		10		10		10		10		ns
6	t _{CLZ}	Chip Enable to Output in LOW-Z ^{4,6}	5		5		5		5		5		ns
7	t _{OLZ}	Output Enable to Output in LOW-Z ^{4,6}	0		0		0		0		0		ns
8	t _{CHZ}	Chip Enable to Output in HIGH-Z ^{4,6}		35		45		45		50		60	ns
9	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4,6}		30		30		30		35		45	ns

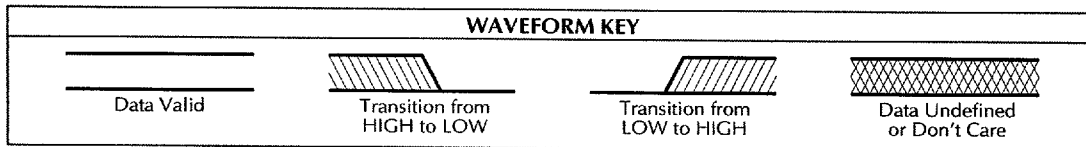
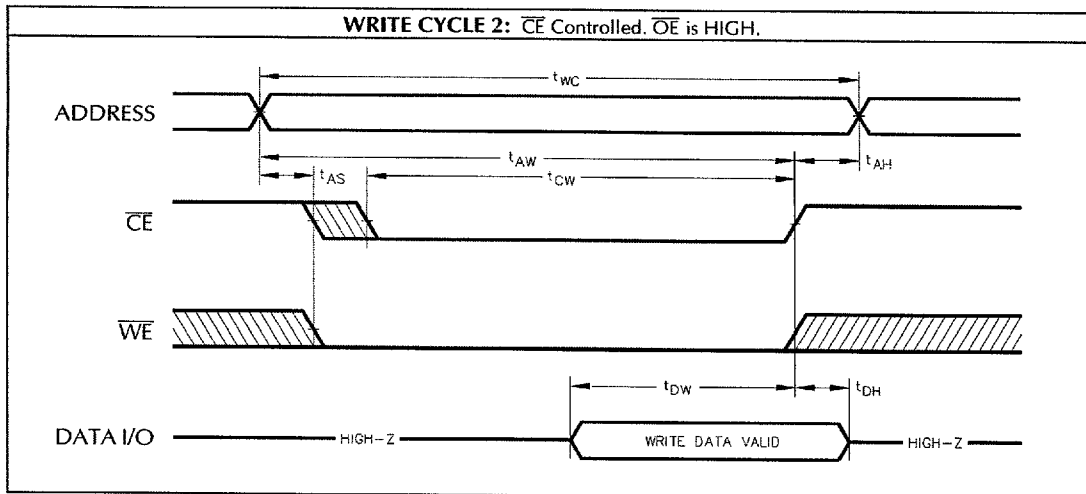
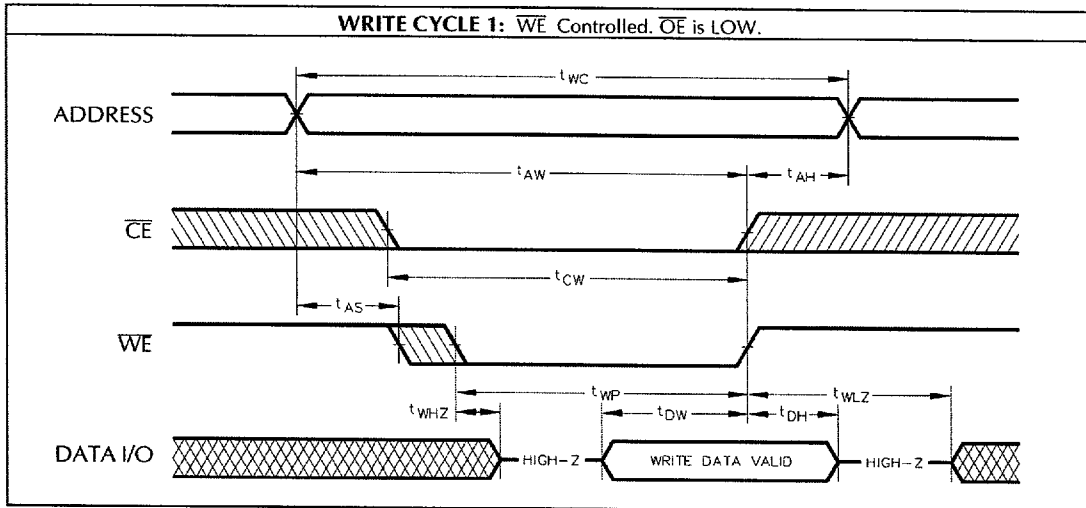
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷													
No.	Symbol	Parameter	70ns ††		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	70		85		100		120		150		ns
11	t _{AV}	Address Valid to End of Write	65		80		90		105		115		ns
12	t _{CV}	Chip Enable to End of Write	65		80		90		105		115		ns
13	t _{DW}	Data to Write Time Overlap	35		35		35		40		50		ns
14	t _{DH}	Data Hold Time from Write Time	0		0		0		0		0		ns
15	t _{WP}	Write Pulse Width	55		55		65		75		85		ns
16	t _{AS}	Address Set-up Time ^{***}	0		0		0		0		0		ns
17	t _{AH}	Address Hold Time	5		5		5		5		5		ns
18	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4,6}		30		30		30		35		40	ns
19	t _{WLZ}	Write Enable to Output in LOW-Z ^{4,6}	5		5		5		5		5		ns

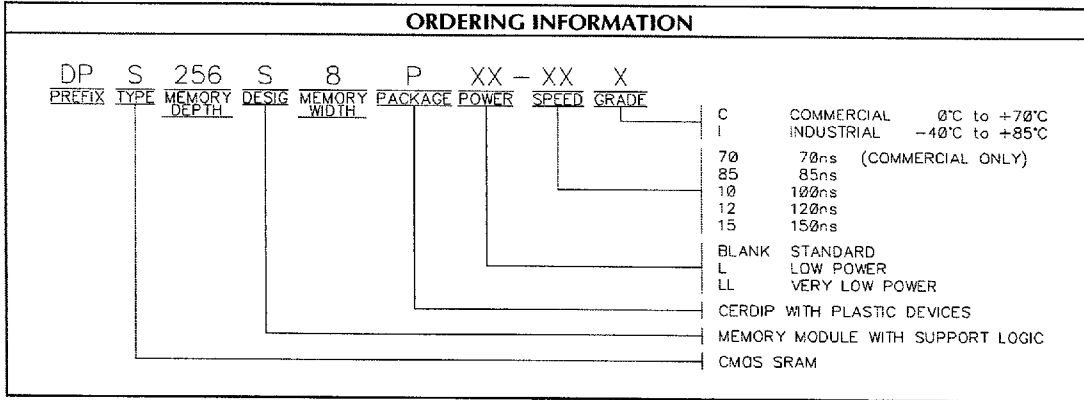
*** Valid for both Read and Write Cycles.

†† Available in commercial only.



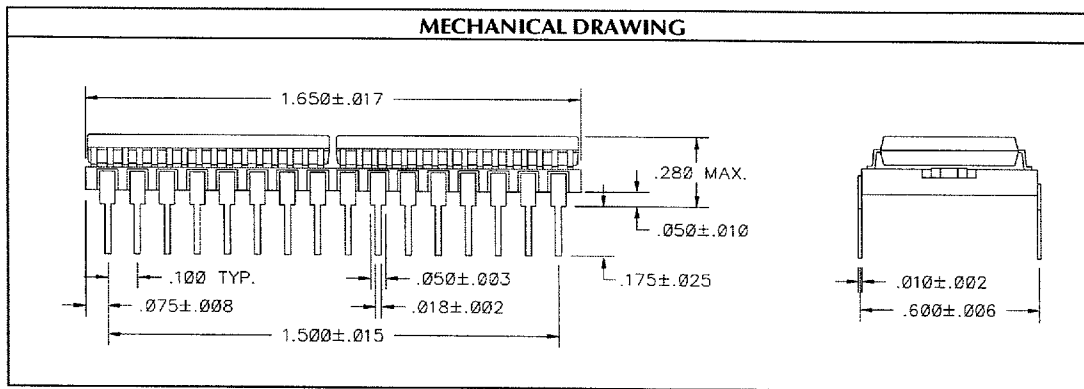






NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.



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