Am29C52A

CMOS Eight-Bit Bidirectional I/O Port

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- **Low Power**
  - The CMOS Am29C52A is a plug-in replacement for the Am2952A. The Am29C52A dissipates less than 20% of the power of its equivalent bipolar part.
- **Am29C52A-1 faster speed-select version**
- **Eight-Bit, Bidirectional I/O Port**
  - Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional buses.
- **Separate Clock, Clock Enable and Three-State Output Enable for Each Register**
- **24 mA Output Current Sink Capability**
- **24-pin Slim Package; 28-pin PLCC**

GENERAL DESCRIPTION

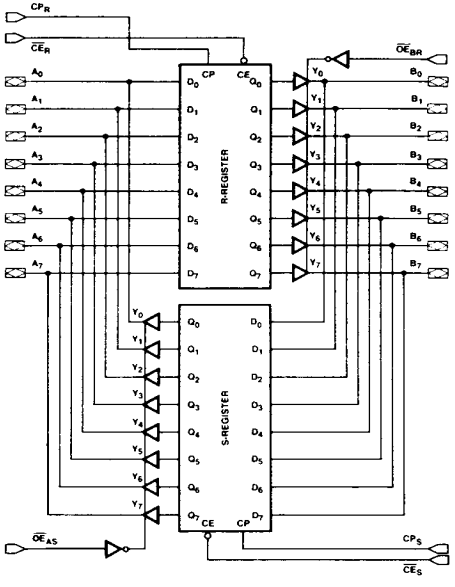
The Am29C52A, a member of Advanced Micro Devices' Am2900 Family, is designed for use as a parallel data I/O port. Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional, three-state buses.

Considerable flexibility is designed into the Am29C52A. Separate Clock, Clock Enable and Three-State Output Enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports.

Twenty-four mA output current sink capability, sufficient for most three-state buses, is provided by the Am29C52A.

The Am29C52A features AMD's advanced CMOS processing. It is a plug-in replacement for the Am2952A.

BLOCK DIAGRAM



BD002371

Publication # 10830 | Rev. A | Amendment /0
Issue Date: May 1989

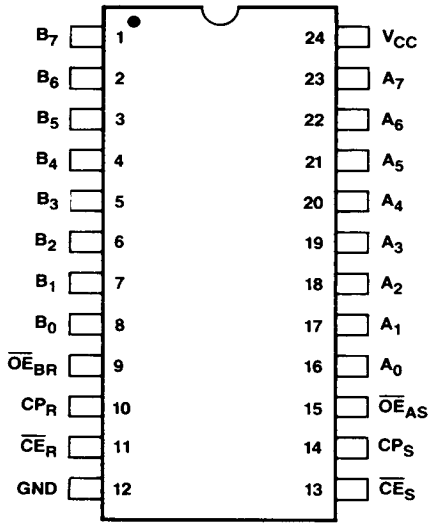
RELATED AMD PRODUCTS

Part No.	Description
Am27S35A	1024 X 8 Registered PROM
Am2904	Status and Shift Controller
Am29C10A	CMOS Microprogram Controller
Am29C101	CMOS 16-Bit Microprocessor Slice
Am29C111	CMOS 16-Bit Microsequencer
Am29C116	CMOS 16-Bit Microsequencer
Am2914	Vectored Interrupt Controller
Am2918	Pipeline Register
Am2922	Condition Code Mux
Am2925	Clock Generator
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am2940	DMA Address Generator
Am29C50A	CMOS 8-Bit Bidirectional I/O Port with Handshake
Am29800A	High-Performance Bus Interface Family
Am29C800	High-Performance CMOS Bus Interface Family
Am29818A	SSR™ Diagnostics/Pipeline Register

SSR is a trademark of Advanced Micro Devices, Inc.

CONNECTION DIAGRAMS
Top View

DIP



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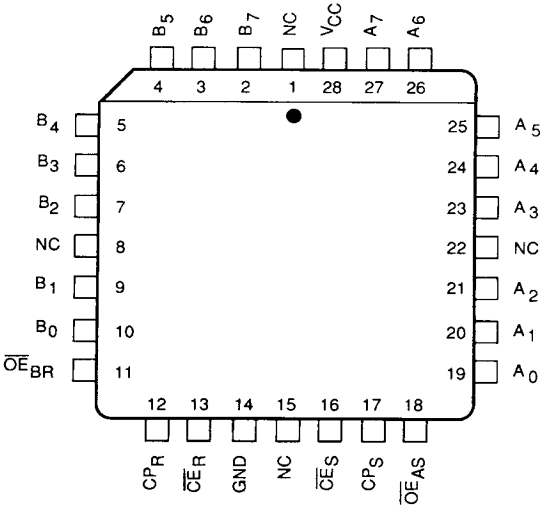
PLCC



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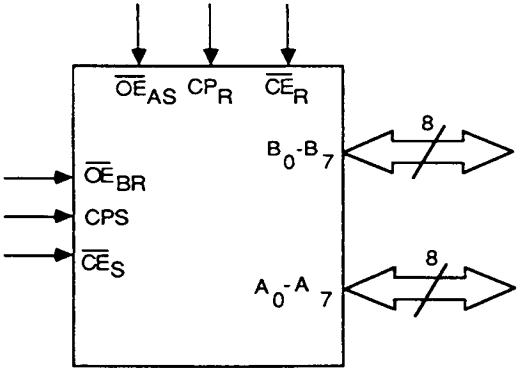
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



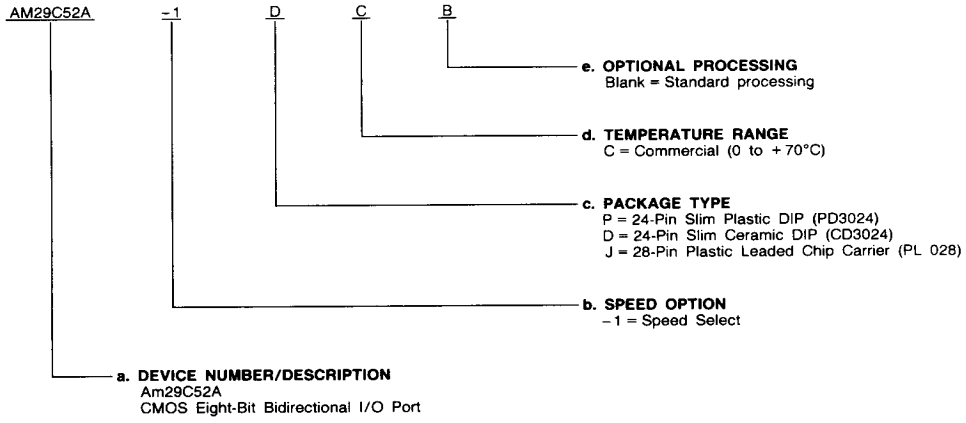
LS003030

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C52A	PC, DC, JC
AM29C52A-1	

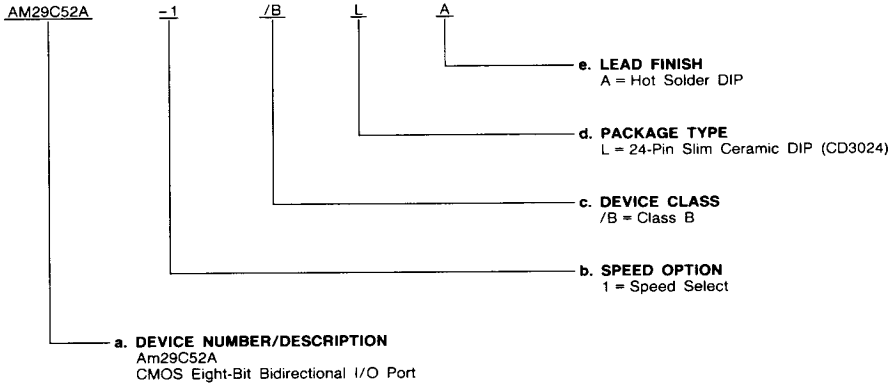
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C52A	/BLA
AM29C52A-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests include Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_7$ Address I/O Lines (Input/Output)
Eight bidirectional lines carrying the R Register inputs or S Register outputs.

$B_0 - B_7$ Address I/O Lines (Input/Output)
Eight bidirectional lines carrying the S Register inputs or R Register outputs.

$\overline{CE}_R$ Clock Enable – R Register (Input)
The clock enable for the R Register. When $\overline{CE}_R$ is LOW, data is entered into the R Register on the LOW-to-HIGH transition of the CP_R signal. When $\overline{CE}_R$ is HIGH, the R Register holds its contents, regardless of CP_R signal transitions.

$\overline{CE}_S$ Clock Enable – S Register (Input)
The clock enable for the S Register. When $\overline{CE}_S$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CP_S signal. When $\overline{CE}_S$ is HIGH, the S Register holds its contents, regardless of CP_S signal transitions.

CP_R Clock – R Register (Input)
The clock for the R Register. When $\overline{CE}_R$ is LOW, data is entered into the R Register on the LOW-to-HIGH transition of the CP_R signal.

CP_S Clock – S Register (Input)
The clock for the S Register. When $\overline{CE}_S$ is LOW, data is entered into the S Register on the LOW-to-HIGH transition of the CP_S signal.

$\overline{OE}_{AS}$ Output Enable – S Register (Input)
The output enable for the S Register. When $\overline{OE}_{AS}$ is LOW, the S Register three-state outputs are enabled onto the $A_0 - A_7$ lines. When $\overline{OE}_{AS}$ is HIGH, the S Register outputs are in the high-impedance state.

$\overline{OE}_{BR}$ Output Enable – R Register (Input)
The output enable for the R Register. When $\overline{OE}_{BR}$ is LOW, the R Register three-state outputs are enabled onto the $B_0 - B_7$ lines. When $\overline{OE}_{BR}$ is HIGH, the R Register outputs are in the high-impedance state.

REGISTER FUNCTION TABLE (Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

H = HIGH
L = LOW
X = Don't care
Z = High Impedance
NC = No Change
↑ = LOW-to-HIGH transition

OUTPUT CONTROL

$\overline{OE}$	Internal Q	Y-Outputs Am29C52A	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.3 V to +7.0 V
DC Voltage Applied to Outputs For
High Output State ..... −0.3 V to +V_{CC} +0.3 V
DC Input Voltage ..... −0.3 V to +5.5 V +0.3 V
DC Output Current, Into Outputs ..... 30 mA
DC Input Current ..... −10 mA to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0°C to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Military* (M) Devices
Ambient Temperature (T_A) ..... −55°C to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Package Thermal Resistance (Typical)

Symbol	CD3024	PD3024	PL 028	Units
θ_{JA}	58	57	76	°C/W
θ_{JC}	10	NA	NA	°C/W

*Military Product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OH} = −2 mA	2.4		V
				COM'L, I_{OL} = −6.5 mA	2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	A_{0-7} B_{0-7}	MIL, I_{OL} = 16 mA		0.5	V
				COM'L, I_{OL} = 24 mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V				−10	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				10	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V				10	μA
I_O	Output Off-State Leakage Current	V_{CC} = Max.	A_{0-7}, B_{0-7}	V_O = 2.4 V		10	μA
				V_O = 0.4 V		−10	
I_{CC}	Static Power Supply Current (Notes 2 & 3)	V_{CC} = Max. I_O = 0 μA	COM'L T_A = 0 to +70°C	(Note 4) TTL V_{IN} = 0.5 V or 2.4 V		30	mA
			MIL T_A = −55 to +125°C	(Note 4) TTL V_{IN} = 0.5 V or 2.4 V		35	
C_{PD}	Power Dissipation Capacitance (Note 4)						

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. I_{CC} is measured with all inputs at 4.5 V and all outputs open.
3. Worst case I_{CC} is at minimum temperature.
4. C_{PD} determines the dynamic current consumption:

I_{CC} (Total) = I_{CC} (Static) + $(C_{PD} + nCL)\frac{f}{2}$ where f is the clock frequency, C_L is the output load capacitance, and n is the number of loads.

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_I	Input Capacitance	f = 1 MHZ, T_A = 25°C V_{CC} = 4.5 V to 5.5 V		.0	pF
C_O	Output Capacitance			.0	

* These capacitances are tested on a sample basis.

SWITCHING CHARACTERISTICS over **Commercial** operating range

Am29C52A

The tables below define the Am29C52A switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5 V output level. All values are in ns with R_L on A_i and B_i = 220 Ω and R_L on FS and FR = 300 Ω. C_L = 50 pF except output disable times which are specified at C_L = 5 pF, measured to 0.5 V change of output voltage level.

A. Setup and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7}	CPR ↓	11(4)	3(5)
B_{0-7}	CPS ↓	11	3
$\overline{CE}S$	CPS ↓	9	2
$\overline{CE}R$	CPR ↓	9(2)	2(3)

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	20	–
CPR ↓	–	20(8)

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	10	10
CPR	10	10(1)

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}	20	20
$\overline{OE}BR$	B_{0-7}	20(7)	20(6)

Note: Waveform reference numbers in parentheses.

Am29C52A-1

A. Setup and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7}	CPR ↓	10(4)	3(5)
B_{0-7}	CPS ↓	10	3
$\overline{CE}S$	CPS ↓	8	2
$\overline{CE}R$	CPR ↓	8(2)	2(3)

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	16	–
CPR ↓	–	16(8)

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	10	10
CPR	10	10(1)

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}	18	18
$\overline{OE}BR$	B_{0-7}	18(7)	18(6)

Note: Waveform reference numbers in parentheses.

SWITCHING CHARACTERISTICS over **Military** operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Am29C52A

A. Setup and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7}	CPR ↓	11(4)	3(5)
B_{0-7}	CPS ↓	11	3
$\overline{CES}$	CPS ↓	9	2
$\overline{CER}$	CPR ↓	9(2)	2(3)

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	20	–
CPR ↓	–	20(8)

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	10	10
CPR	10	10(1)

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}	20	20
$\overline{OE}BR$	B_{0-7}	20(7)	20(6)

Note: Waveform reference numbers in parentheses.

Am29C52A-1

A. Setup and Hold Times

Input	With Respect To	t_s	t_h
A_{0-7}	CPR ↓	10(4)	3(5)
B_{0-7}	CPS ↓	10	3
$\overline{CES}$	CPS ↓	8	2
$\overline{CER}$	CPR ↓	8(2)	2(3)

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	16	–
CPR ↓	–	16(8)

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS	10	10
CPR	10	10(1)

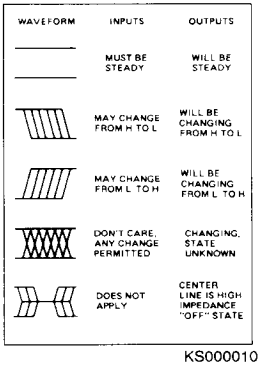
D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}AS$	A_{0-7}	18	18
$\overline{OE}BR$	B_{0-7}	18(7)	18(6)

Note: Waveform reference numbers in parentheses.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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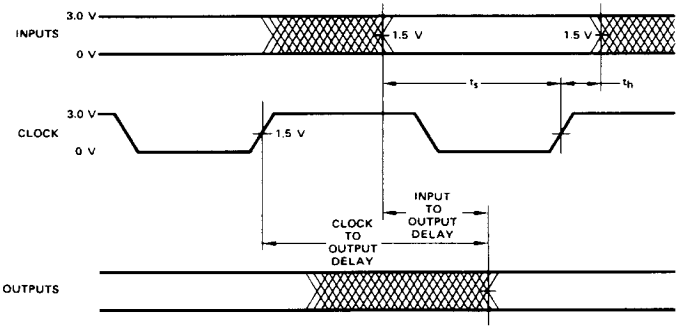

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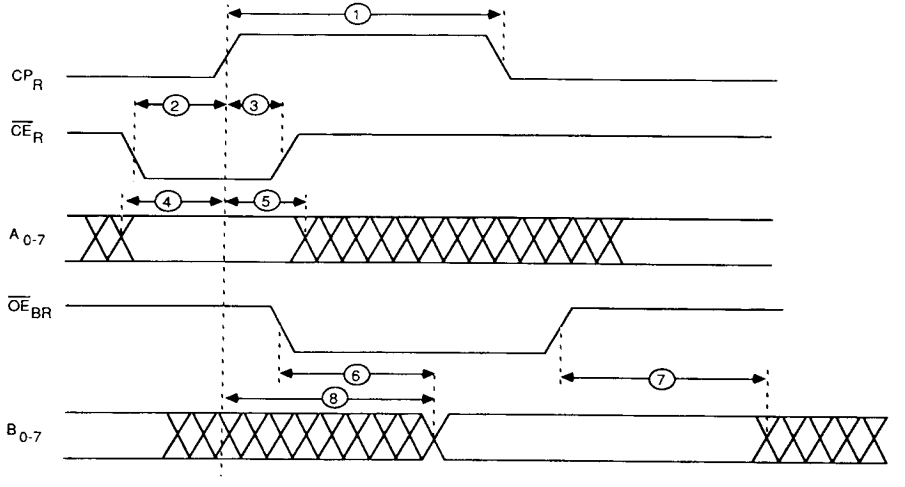
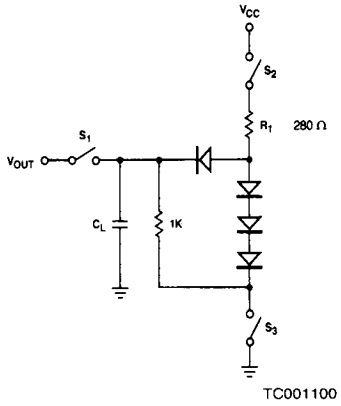


Note: Waveforms apply to both S and R registers.

WF024460

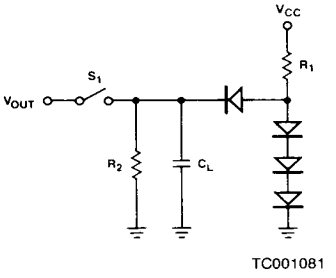
Write and Read

SWITCHING TEST CIRCUITS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}}$$

A. Three-State Outputs



$$R_2 = \frac{2.4\ V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}}$$

B. Normal Outputs

Notes: 1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.

TEST OUTPUT LOADS FOR Am29C52A

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
16–23	A_{0-7}	A	220	1K
1–8	B_{0-7}	A	220	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

TEST PHILOSOPHY AND METHODS

The following eight points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.

2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.

3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.

4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.

5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.

6. Capacitive Loading for AC Testing.

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the progagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH}, I_{OL} for example) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.

7. Threshold Testing

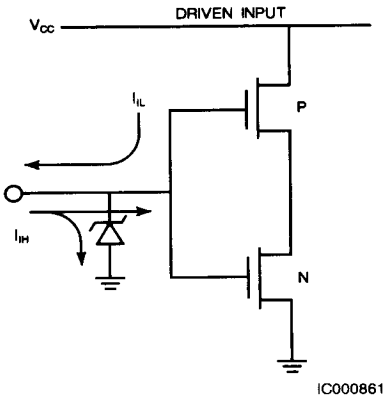
The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high speed circuits. These oscillations are not indicative of a reject device, but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" put levels rather than at V_{IL} Max. and V_{IH} Min.

8. AC Testing

Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

INPUT/OUTPUT CIRCUIT DIAGRAMS



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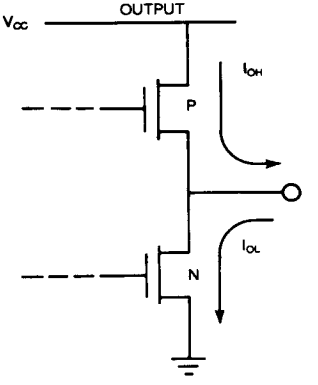

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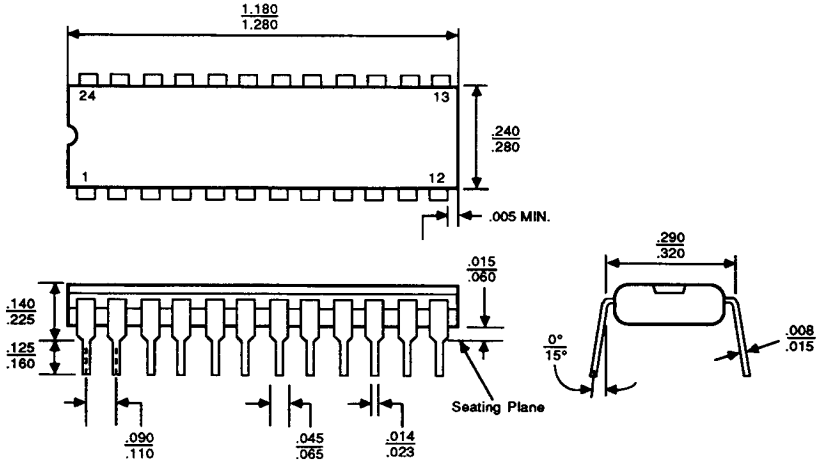
PHYSICAL DIMENSIONS*

PD3024



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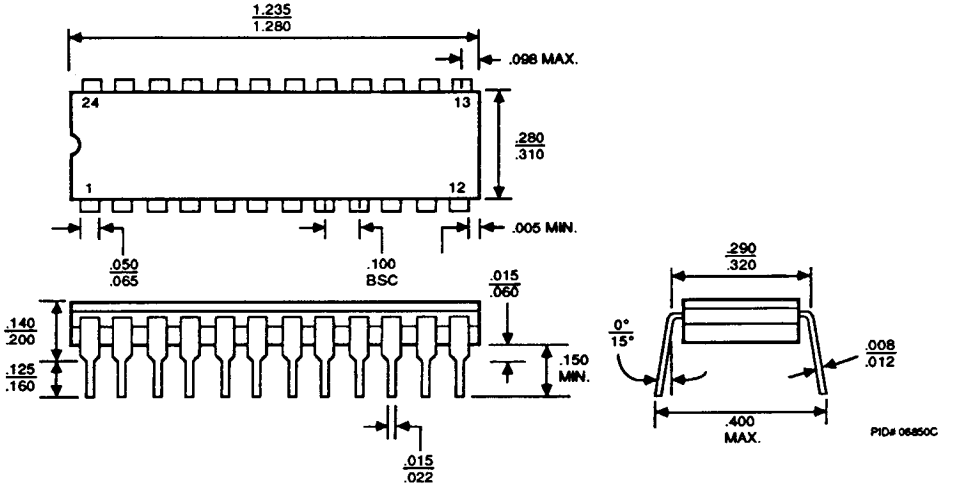
CD3024

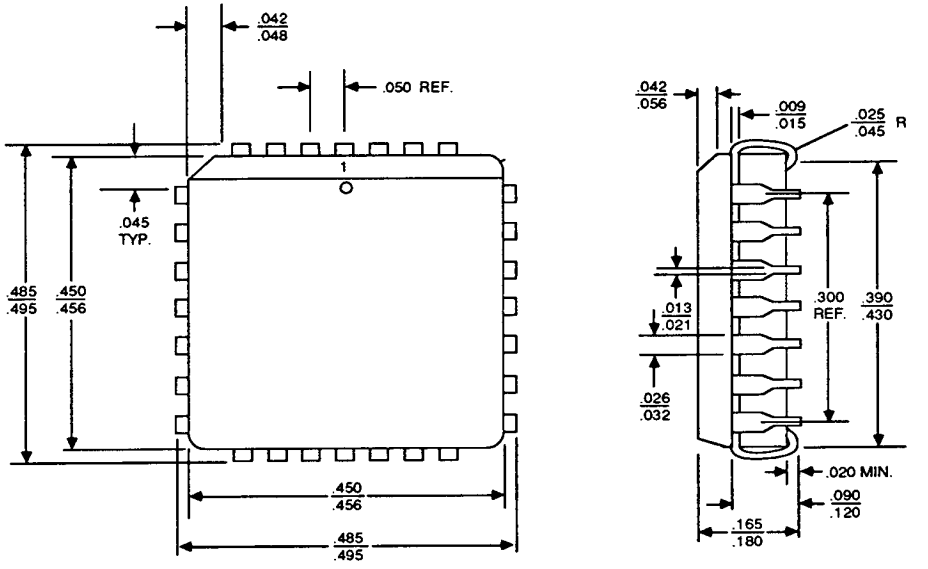


PID # 06850C

*For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS (Cont'd.)

PL 028



PID# 06751E

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