

## HMOS HIGH DENSITY N-CHANNEL SILICON-GATE DEPLETION LOAD 16/32 BIT MICROPROCESSOR

**DESCRIPTION**

The TS 68000 is the first implementation of the 68000 16/32 microprocessor architecture. The TS 68000 has a 16-bit data bus and 24-bit address and data-buses. It is completely code-compatible with the TS 68008 8-bit data bus implementation of the 68000 and is downward code-compatible with the TS 68020 32-bit implementation of the architecture. Any user-mode programs written using the TS 68000 instruction set will run unchanged on the TS 68008 and TS 68020. This is possible because the user programming model is identical for all three processors and the instruction sets are proper sub-sets of the complete architecture.

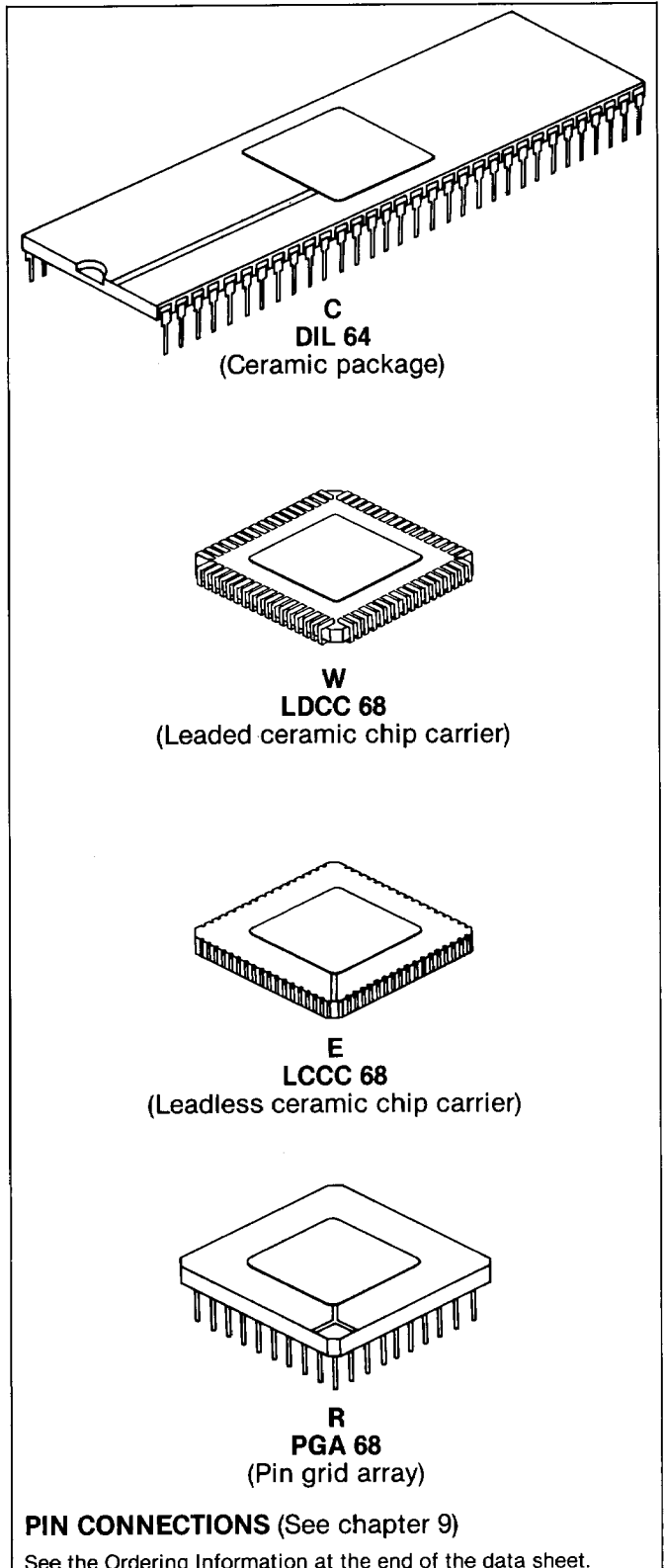
**MAIN FEATURES**

- 16/32-bit data and address register
- 16 megabytes direct addressing range
- 56 powerful instruction types
- Operations on five main data types
- Memory mapped I/O
- 14 addressing modes
- 3 available versions : 8 MHz / 10 and 12.5 MHz
- Military temperature range :
  - 55 / + 125°C (8 / 10 MHz),
  - 55 / + 110°C (12.5 MHz)
- Power supply : 5.0 VDC  $\pm$  5 %

**SCREENING / QUALITY**

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y)
- MIL-STD-883 (class B, rev C)
- DESC 82021
- TMS STANDARD.



## **SUMMARY**

- 1 - SCOPE
- 2 - APPLICABLE DOCUMENTS
- 3 - REQUIREMENTS
- 4 - QUALITY ASSURANCE PROVISION
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- 6 - PREPARATION FOR DELIVERY
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- 9 - TERMINAL CONNECTIONS
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## 1 - SCOPE

This drawing describes the specific requirements for the microprocessor 68000, 8, 10 and 12.5 MHz in compliance either with MIL-STD-883 class B rev C, CECC 90000 class B or TMS STANDARD.

## 2 - APPLICABLE DOCUMENTS

### 2.1 - MIL-STD-883

- 1) MIL-STD-883 : test methods and procedures for electronics
- 2) MIL-M-38510 : general specifications for microcircuits
- 3) Desc Drawing 8202102 (8 MHz) - 8202103 (10 MHz) - 8202104 (12.5 MHz)

### 2.2 - CECC 90000

- 1) CECC 90000
- 2) Specification CECC 90110-001      8 / 10 MHz  
CECC 90110-006      12.5 MHz

## 3 - REQUIREMENTS

### 3.1 - GENERAL

The microcircuits are in accordance with the applicable document and as specified herein.

### 3.2 - DESIGN AND CONSTRUCTION

#### 3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be as shown in § 9.

#### 3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 (except finish C (as described in 3.5.6.1 of MIL-M-38510)).

#### 3.2.3 - Package

The microcircuits are packaged in a hermetically sealed ceramic package which is conformed to case outlines of MIL-M-38510 appendix C (when defined).

- 64 lead DIP      case outline : D-13
- SQ.LCC 68 pins      case outline : C-7
- 68 Terminal JCC      case outline : C-J5
- 68 PIN SQ.PGA up case outline : similar to P-AB.

The precise case outlines are described in MIL-M-38510 and into § 8 of this document.

### 3.3 - ELECTRICAL REQUIREMENTS

#### 3.3.1 - Absolute maximum ratings

Characteristics	Symbol	Conditions	Min	Max	Unit
Supply voltage	V <sub>CC</sub>	—	-0.3	+0.7	V
Input voltage	V <sub>I</sub>	—	-0.3	+0.7	V
Storage temperature	T <sub>stg</sub>	—	-65	+150	°C
Power dissipation	P <sub>D</sub>	T <sub>case</sub> = -55°C for 8 - 10 - 12.5 MHz		1.75	W
		T <sub>case</sub> = +125°C • 8 - 10 MHz • 12.5 MHz		1.5 1.7	W W
Junction temperature	T <sub>j</sub>	—	—	170	°C
Lead temperature		max soldering 5 seconds	—	270	°C
Thermal resistance	R <sub>th</sub>	estimated for any ceramic package		10	°C/W
Operating temperature (*)		T <sub>case</sub> • 8 - 10 MHz • 12.5 MHz	-55 -55	+125 +110	°C °C

#### 3.3.2 - Recommended operating conditions

Characteristics and conditions	Symbol	Operating ranges		
		Min	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.25	V
High level input voltage	V <sub>IH</sub>	2	—	V
Low level input voltage	V <sub>IL</sub>	—	0.8	V
Frequency of operation • 8 MHz part • 10 MHz part • 12.5 MHz part	F	4 4 4	8 10 12.5	MHz MHz MHz
Case operating temperature range • 8 - 10 MHz part (*) • 12.5 MHz part	T <sub>case</sub>	-55 -55	+125 +110	°C °C
Clock rise time	t <sub>r</sub>		10	ns
Clock fall time	t <sub>f</sub>		10	ns

(\*) T<sub>case</sub> could be -40 / +85°C or 0 / 70°C as specified in ordering information chapter 10.4.



### 3.3.3 - Electrical performance conditions

The electrical performance characteristics are specified in table 1 and are applied over full operating temperature range unless otherwise specified (see 10.4).

## 3.4 - MECHANICAL AND ENVIRONMENT

The microcircuit shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

## 3.5 - MARKING

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following informations as minimum :

3.5.1 - Thomson logo

3.5.2 - Manufacturer's part number

3.5.3 - Class B identification

3.5.4 - Date-code of inspection lot

3.5.5 - ESD identifier if available

3.5.6 - Country of manufacturing

## 4 - QUALITY CONFORMANCE INSPECTION

### 4.1 - DESC/MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each inspection lot. Group C and D inspection are performed on a periodic basis in accordance with method 5005 of MIL-STD-883.

### 4.2 - CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each inspection lot as specified in CECC 90110-001. Group C inspection is performed on a periodic basis in accordance with CECC 90110-001.

## 5 - ELECTRICAL CHARACTERISTICS

### 5.1 - GENERAL REQUIREMENTS

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 1A : Static electrical characteristics for all electrical variants.
- Table 1B : Dynamic electrical characteristics for 68000-8 (8 MHz).
- Table 1C : Dynamic electrical characteristics for 68000-10 (10 MHz).
- Table 1D : Dynamic electrical characteristics for 68000-12 (12.5 MHz).

For static characteristics (Table 1A), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics, test methods refer to § 5.2 of this specification (Tables 1B, 1C and 1D).

Indication of «min.» or «max.» in the column «Test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.3 here above.

### 5.2 - TEST CONDITIONS SPECIFIC TO THE DEVICE

#### 5.2.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of tables 1B, 1C and 1D referring to the loading network number as shown in figures 1A and 1B below.

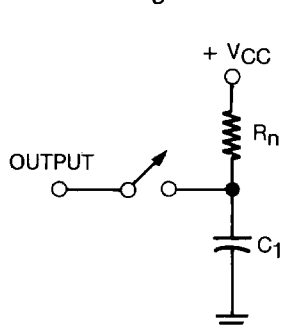


FIGURE 1A - PASSIVE LOADS.

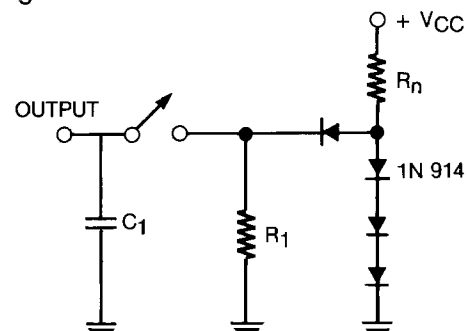


FIGURE 1B - ACTIVE LOADS.

Load NBR	Figure	R <sub>1</sub>	R <sub>n</sub>	C <sub>1</sub> *	Output application
1	1A	—	910 Ω	130 pF	$\overline{\text{RESET}}$
2	1A	—	2.9 kΩ	70 pF	$\overline{\text{HALT}}$
3	1B	6.0 k	1.22 kΩ	130 pF	A1 to A23 $\overline{\text{BG}}$ and FC0 to FC2
4	1B	6.0 k	740 Ω	130 pF	All other outputs

\* C<sub>1</sub> includes all parasitic capacitances of test machines.

5.2.2 - Time definitions

The times specified in tables 1B and 1C as dynamic characteristics are defined in figures 2 to 5 below by a reference number given in the column «Method» of the tables together with the relevant figure number.

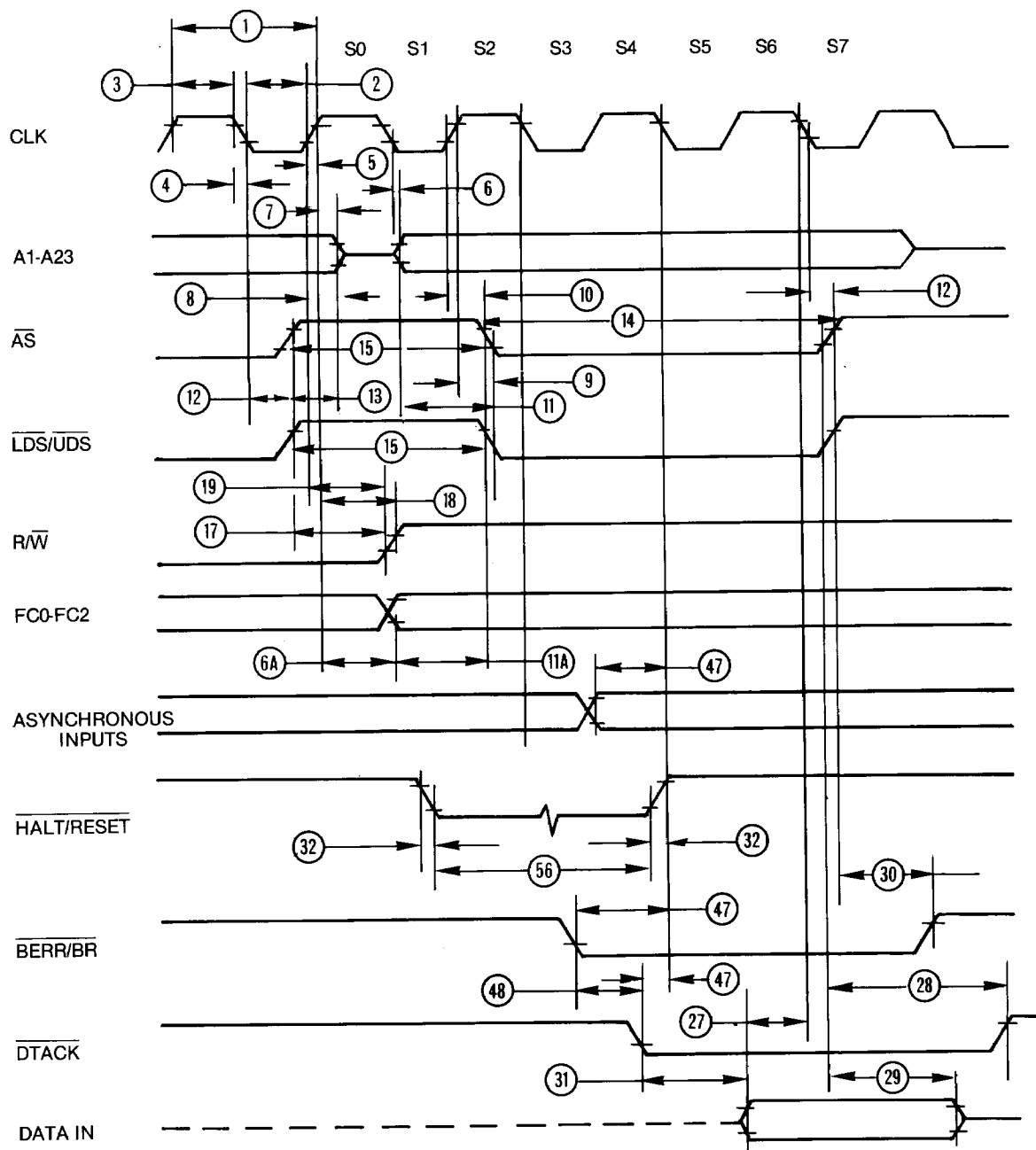


FIGURE 2 - READ CYCLE TIMING.

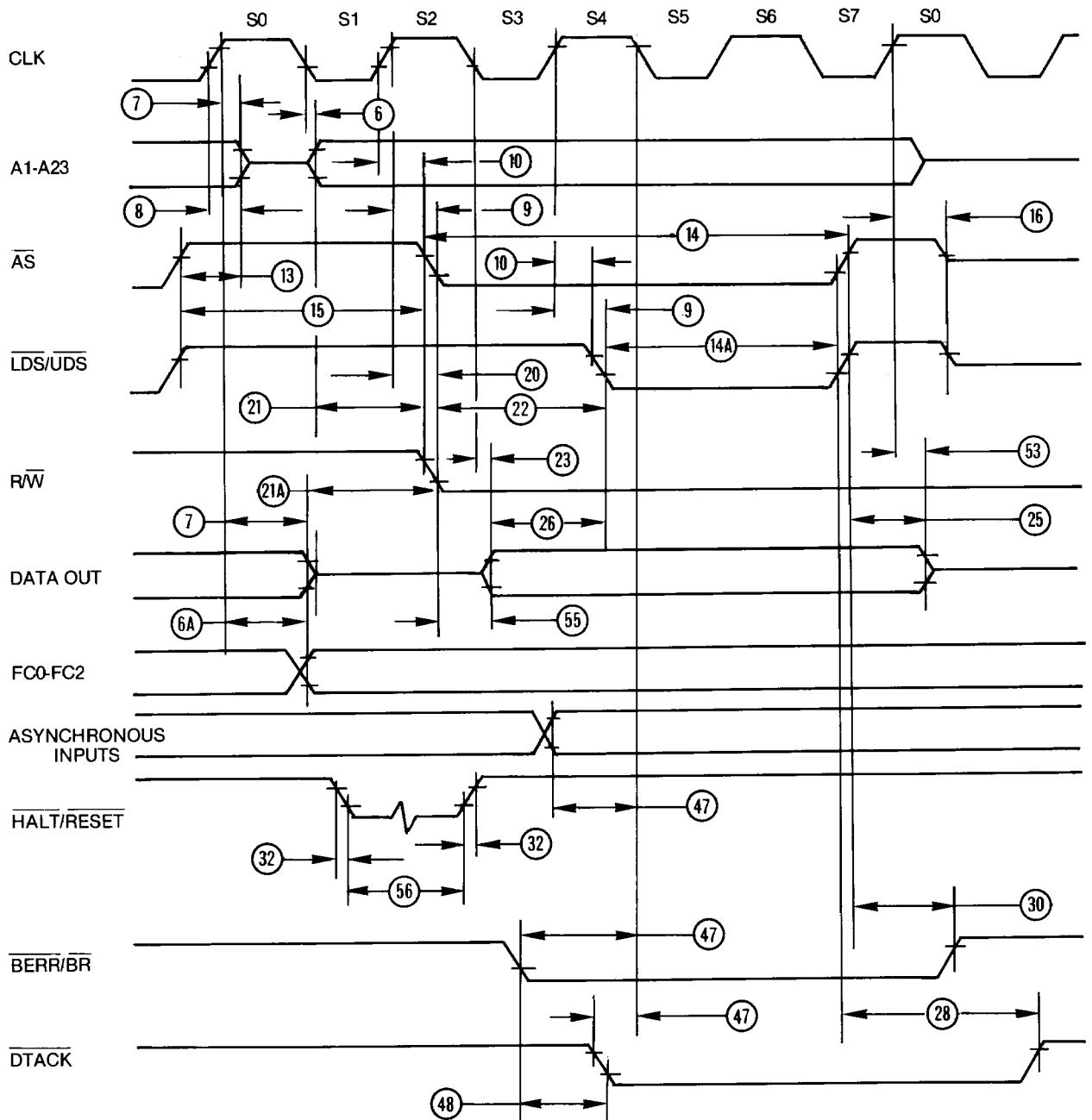


FIGURE 3 - WRITE CYCLE TIMING.

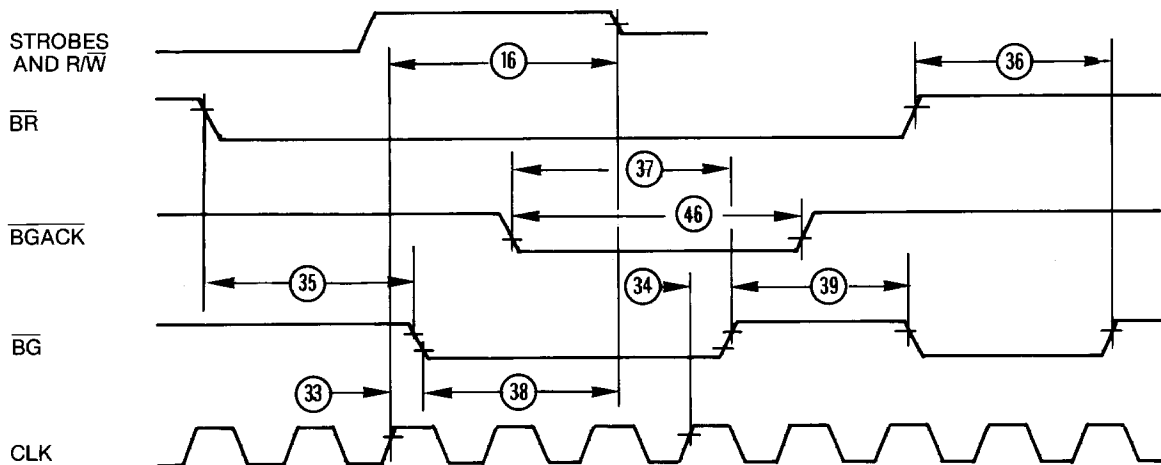


FIGURE 4 - AC ELECTRICAL WAVEFORMS - BUS ARBITRATION.

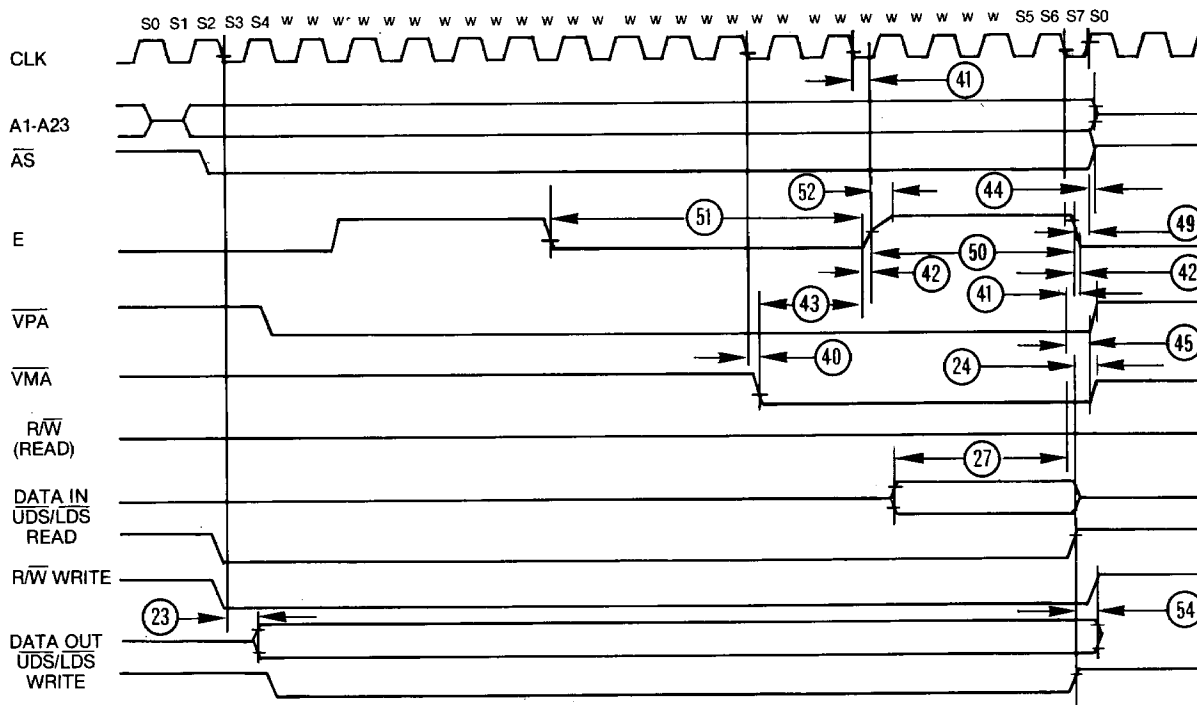


FIGURE 5 - ENABLE / INTERFACE TIMING.

5.2.3 - Input and output signals for dynamic measurements

a) Input pulse characteristics

Where input pulse generator is loaded by only a 50 Ω resistor, the input pulse characteristics shall be as shown in figure 6.

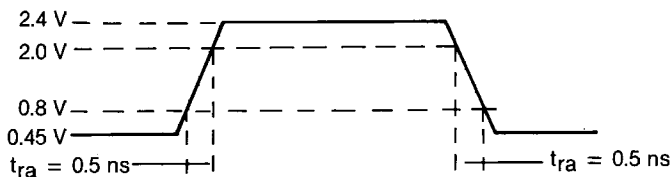


FIGURE 6 - INPUT PULSE CHARACTERISTICS.

b) Time measurement input voltage references

Input voltages which are taken as reference for time measurement shall be :

$V_{IL} = 0.8 \text{ V}$

$V_{IH} = 2.0 \text{ V}$

c) Time measurement output voltage reference for valid state output

Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements, shall be as shown in figure 7.

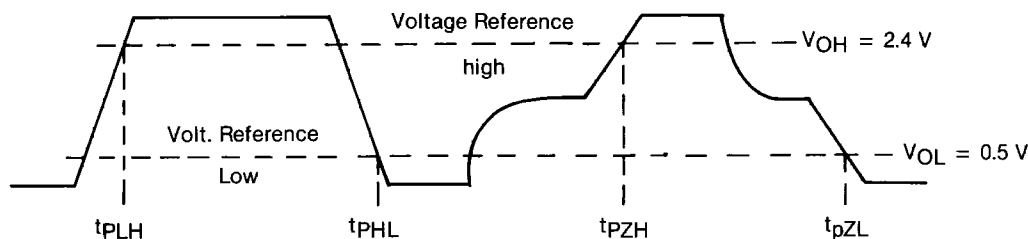


FIGURE 7 - OUTPUT VOLTAGE REFERENCES.

5.2.4 - Referred notes to the tables 1x

The following notes shall apply where referred into the tables 1B, 1C and 1D.

**Note 1 :** If the asynchronous setup time (47) requirements are satisfied, the  $\overline{DTACK}$  low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (27) for the following cycle.

**Note 2 :** Where «CLKS» is stated as unit time limit, the relevant time in nanoseconds shall be calculated as the actual cycle time of clock signal input multiply by the given number of CLKS limits.

**Note 3 :** For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum columns.

**Note 4 :** Actual value depends on actual period.

**Note 5 :** If 47 is satisfied for both  $\overline{DTACK}$  and  $\overline{BERR}$ , 48 may be 0 nanoseconds.

**Note 6 :** The processor will negate  $\overline{BG}$  and begin driving the bus again if external arbitration logic negates  $\overline{BR}$  before asserting  $\overline{BGACK}$ .

**Note 7 :** The falling edge of 56 triggers both the negation of the strobes ( $\overline{AS}$ , and  $\overline{XDS}$ ) and the falling edge of  $\overline{E}$ . either of these events can occur first depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the  $\overline{E}$  clock.

**Note 8 :** When  $\overline{AS}$  and  $\overline{R\overline{W}}$  are equally loaded ( $\pm 20\%$ ), subtract 10 nanoseconds from the values in these columns.

TABLE 1A - STATIC CHARACTERISTICS

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
1	ICC	Supply current	41	VCC = 5.25 V	25°C	—	335	mA
					max			
					min			
2	VOL (1)	Low level output voltage for : A1 to A23 FC0 to FC2 ; $\overline{BG}$	37	VCC = 4.75 V  IOL = 3.2 mA	25°C	—	0.5	V
					max			
					min			
3	VOL (2)	Low level output voltage for : $\overline{HALT}$	37	VCC = 4.75 V  IOL = 1.6 mA	25°C	—	0.5	V
					max			
					min			
4	VOL (3)	Low level output voltage for : AS ; R/W : D0 to D15 $\overline{UDS}$ ; $\overline{LDS}$ ; $\overline{VMA}$ and $\overline{E}$	37	VCC = 4.75 V  IOL = 5.3 mA	25°C	—	0.5	V
					max			
					min			
5	VOL (4)	Low level output voltage for : $\overline{RESET}$	37	VCC = 4.75 V  IOL = 5.0 mA	25°C	—	0.5	V
					max			
					min			
6	VOH	High level output voltage for all outputs	37	VCC = 4.75 V  IOH = -400 $\mu$ A	25°C	2.4	—	V
					max			
					min			
7	IIH (1)	High level input current for all inputs excepted $\overline{HALT}$ and $\overline{RESET}$	38	VCC = 5.25 V  IIH = 2.4 V	25°C	—	2.5	$\mu$ A
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.1.





TABLE 1A - STATIC CHARACTERISTICS (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
8	I <sub>IL</sub> (1)	Low level input current for all inputs excepted <u>HALT</u> and <u>RESET</u>	38	V <sub>CC</sub> = 5.25 V  I <sub>IL</sub> = 0.4 V	25°C	- 2.5	—	μA
					max			
					min			
9	I <sub>IH</sub> (2)	High level input current for : <u>HALT</u> and <u>RESET</u>	38	V <sub>CC</sub> = 5.25 V  I <sub>IH</sub> = 2.4 V	25°C	—	20	μA
					max			
					min			
10	I <sub>IL</sub> (2)	Low level input current for : <u>HALT</u> and <u>RESET</u>	38	V <sub>CC</sub> = 5.25 V  I <sub>IL</sub> = 0.4 V	25°C	- 20	—	μA
					max			
					min			
11	I <sub>OHZ</sub>	High level output three-state leakage current for all outputs	—	V <sub>CC</sub> = 5.25 V  V <sub>OH</sub> = 2.4 V	25°C	—	20	μA
					max			
					min			
12	I <sub>OLZ</sub>	Low level output three-state leakage current for all outputs	—	V <sub>CC</sub> = 5.25 V  V <sub>OL</sub> = 0.4 V	25°C	—	20	μA
					max			
					min			
13	V <sub>IH</sub>	High level input voltage for all inputs	—	V <sub>CC</sub> = 4.75 V	25°C	2.0	—	V
					max			
					min			
14	V <sub>IL</sub>	Low level input voltage for all inputs	—	V <sub>CC</sub> = 4.75 V	25°C	—	0.8	V
					max			
					min			
14A	C <sub>in</sub>	Input capacitance (all inputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C	—	25	pF
					max	—	NA	—
					min	—	NA	—
14B	C <sub>out</sub>	Output capacitance (all outputs)	11	Reverse voltage = 0 V f = 1.0 MHz	25°C	—	20	pF
					max	—	NA	—
					min	—	NA	—
14C	V <sub>test</sub>	Internal protection Transient energy rating	See DS 5.2	See 5.2 of this DS 5 cycles	25°C	- 500	+ 500	V

(\*) Algebraic values.

(\*\*) Measurement method : see 5.1.

TABLE 1B - DYNAMIC CHARACTERISTICS - TS 68000-8

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
15	t <sub>su</sub> (D <sub>I</sub> CL)	Set-up time Data-in to clock low (Note 1)	Fig. 2 Ref. 27	See 5.2.3 (a) to (c) f <sub>C</sub> = 8 MHz	25°C	25	—	ns
					max			
					min			
16	t <sub>su</sub> (SDTCL)	Set-up time DTACK low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1B - DYNAMIC CHARACTERISTICS - TS 68000-8 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
17	$t_{su}$ (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
18	$t_{su}$ (SBGCL)	Set-up time $\overline{BGACK}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
19	$t_{su}$ (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
20	$t_{su}$ (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
21	$t_w$ (CL)	Clock width low	Fig. 2 Ref. 2	See test 15	25°C	55	125	ns
					max			
					min			
22	$t_w$ (CH)	Clock width high	Fig. 2 Ref. 3	See test 15	25°C	55	125	ns
					max			
					min			
23	$t_{PLH}$ $t_{PHL}$ (CHFCV)	Propagation time clock high to FC valid	Fig. 2 Ref. 6	See test 15 Load : 3	25°C	—	70	ns
					max			
					min			
24	$t_{PHL}$ (CHSLX)	Propagation time clock high to $\overline{AS}$ low	Fig. 2 Ref. 9	See test 15 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
26	$t_{PHL}$ (CHSL)	Propagation time CLK high to $\overline{LDS}$ , $\overline{UDS}$ low	Fig. 2 Ref. 9	See test 15 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
27	$t_{PLH}$ (CLSH)	Propagation time CLK low to $\overline{AS}$ high	Fig. 2 Ref. 12	See test 15 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
28	$t_{PLH}$ (CLSH)	Propagation time CLK low to $\overline{LDS}$ , $\overline{UDS}$ high	Fig. 2 Ref. 12	See test 15 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
29	$t_{PLH}$ (CHRHX)	Propagation time CLK high to R/W high	Fig. 2 Ref. 18	See test 15 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
30	$t_{PHL}$ (CHRL)	Propagation time CLK high to $\overline{R/W}$ low	Fig. 3 Ref. 20	See test 15 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
31	$t_{PZL}$ $t_{PZH}$ (CLDO)	Propagation time CLK low to Data-out valid	Fig. 3 Ref. 23	See test 15 Load : 4	25°C	—	70 Note 3	ns
					max			
					min			
32	$t_{PZL}$ $t_{PZH}$ (CLAV)	Propagation time CLK low to Address valid	Fig. 2 Ref. 6	See test 15 Load : 3	25°C	—	70	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).



TABLE 1B - DYNAMIC CHARACTERISTICS - TS 68000-8 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
33	t <sub>PHL</sub> (CHGL)	Propagation time CLK high to $\overline{BG}$ low	Fig. 4 Ref. 33	See test 15 Load : 3	25°C	—	70	ns
					max			
					min			
34	t <sub>PLH</sub> (CHGH)	Propagation time CLK high to $\overline{BG}$ high	Fig. 4 Ref. 34	See test 15 Load : 3	25°C	—	70	ns
					max			
					min			
35	t <sub>PHL</sub> (CLVM)	Propagation time CLK low to $\overline{VMA}$ low	Fig. 5 Ref. 40	See test 15 Load : 4	25°C	—	70	ns
					max			
					min			
36	t <sub>PHL</sub> (CLE)	Propagation time CLK low to E low	Fig. 5 Ref. 41	See test 15 Load : 4	25°C	—	70	ns
					max			
					min			
38	t <sub>h</sub> (SHAZ)	Hold time CLK high to Address	Fig. 2 Ref. 8	See test 15 Load : 3	25°C	0	—	ns
					max			
					min			
42	t <sub>su</sub> (AVSL)	Set-up time Address valid to $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ low	Fig. 2 Ref. 11	See test 15 Load : 4	25°C	30 Note 4	—	ns
					max			
					min			
51	t <sub>PHL</sub> (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	Fig. 4 Ref. 35	See test 15 Load : 3	25°C	1.5	3.5	CLKS Note 2
					max			
					min			
53	t <sub>PLH</sub> (GALEH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	Fig. 4 Ref. 37	See test 15 Load : 3	25°C	1.5	3.5	CLKS Note 2
					max			
					min			
60	t <sub>su</sub> (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	Fig. 3 Ref. 48	See test 15	25°C	20 Note 5	—	ns
					max			
					min			
68	t <sub>su</sub> (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	Fig. 2 Ref. 48	See test 15	25°C	20 Note 5	—	ns
					max			
					min			
72	t <sub>h</sub> (DOSL)	Hold time Data-out valid to $\overline{LDS}$ , $\overline{UDS}$ low	Fig. 3 Ref. 26	See test 15 Load : 4	25°C	30 Note 4	—	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1C - DYNAMIC CHARACTERISTICS - TS 68000-10

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
15	t <sub>su</sub> (DACL)	Set-up time Data-in to clock low (Note 1)	Fig. 2 Ref. 27	See 5.2.3 (a) to (c) f <sub>c</sub> = 10 MHz	25°C	20	—	ns
					max			
					min			
16	t <sub>su</sub> (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1C - DYNAMIC CHARACTERISTICS - TS 68000-10 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
17	t <sub>SU</sub> (SBRCL)	Set-up time B̄R low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
18	t <sub>SU</sub> (SBGCL)	Set-up time BGACK low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
19	t <sub>SU</sub> (SVPACL)	Set-up time V̄PA low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
20	t <sub>SU</sub> (SBERCL)	Set-up time B̄ERR low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
21	t <sub>w</sub> (CL)	Clock width low	Fig. 2 Ref. 2	See test 15	25°C	45	125	ns
					max			
					min			
22	t <sub>w</sub> (CH)	Clock width high	Fig. 2 Ref. 3	See test 15	25°C	45	125	ns
					max			
					min			
23	t <sub>PLH</sub> t <sub>PHL</sub> (CHFCV)	Propagation time clock high to FC valid	Fig. 2 Ref. 6A	See test 15 Load : 3	25°C	—	60	ns
					max			
					min			
24	t <sub>PHL</sub> (CHSLX)	Propagation time clock high to ĀS low	Fig. 2 Ref. 9	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
26	t <sub>PHL</sub> (CHSL)	Propagation time CLK high to LDS, UDS low	Fig. 2 Ref. 9	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
27	t <sub>PLH</sub> (CLSH)	Propagation time CLK low to ĀS high	Fig. 2 Ref. 12	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
28	t <sub>PLH</sub> (CLSH)	Propagation time CLK low to LDS, UDS high	Fig. 2 Ref. 12	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
29	t <sub>PLH</sub> (CHRHX)	Propagation time CLK high to R/W high	Fig. 2 Ref. 18	See test 15 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
30	t <sub>PHL</sub> (CHRL)	Propagation time CLK high to R/W low	Fig. 3 Ref. 20	See test 15 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
31	t <sub>PZL</sub> t <sub>PZH</sub> (CLDO)	Propagation time CLK low to Data-out valid	Fig. 3 Ref. 23	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
32	t <sub>PZL</sub> t <sub>PZH</sub> (CLAV)	Propagation time CLK low to Address valid	Fig. 2 Ref. 6	See test 15 Load : 4	25°C	—	60	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1C - DYNAMIC CHARACTERISTICS - TS 68000-10 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
33	t <sub>PHL</sub> (CHGL)	Propagation time CLK high to $\overline{BG}$ low	Fig. 4 Ref. 33	See test 15 Load : 3	25°C	—	60	ns
					max			
					min			
34	t <sub>PLH</sub> (CHGH)	Propagation time CLK high to $\overline{BG}$ high	Fig. 4 Ref. 34	See test 15 Load : 3	25°C	—	60	ns
					max			
					min			
35	t <sub>PHL</sub> (CLVM)	Propagation time CLK low to VMA low	Fig. 5 Ref. 40	See test 15 Load : 4	25°C	—	70	ns
					max			
					min			
36	t <sub>PHL</sub> (CLE)	Propagation time CLK low to E low	Fig. 5 Ref. 41	See test 15 Load : 4	25°C	—	55	ns
					max			
					min			
38	t <sub>h</sub> (SHAZ)	Hold time CLK high to Address	Fig. 2 Ref. 8	See test 15 Load : 3	25°C	0	—	ns
					max			
					min			
42	t <sub>su</sub> (AVSL)	Set-up time Address valid to $\overline{AS}$ , $\overline{LDS}$ , $\overline{UDS}$ low	Fig. 2 Ref. 11	See test 15 Load : 4	25°C	20 Note 4	—	ns
					max			
					min			
51	t <sub>PHL</sub> (BRLGL)	Propagation time $\overline{BR}$ low to $\overline{BG}$ low	Fig. 4 Ref. 35	See test 15 Load : 3	25°C	1.5 —	3.5 + 80	CLKS Note 2 ns
					max			
					min			
53	t <sub>PLH</sub> (GALGH)	Propagation time $\overline{BGACK}$ low to $\overline{BG}$ high	Fig. 4 Ref. 37	See test 15 Load : 3	25°C	1.5 —	3.5 + 80	CLKS Note 2 ns
					max			
					min			
60	t <sub>su</sub> (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	Fig. 3 Ref. 48	See test 15	25°C	20 Note 5	—	ns
					max			
					min			
68	t <sub>su</sub> (BELDAL)	Set-up time $\overline{BERR}$ low to $\overline{DTACK}$ low	Fig. 2 Ref. 48	See test 15	25°C	20 Note 5	—	ns
					max			
					min			
72	t <sub>h</sub> (DOSL)	Hold time Data-out valid to $\overline{LDS}$ , $\overline{UDS}$ low	Fig. 3 Ref. 26	See test 15 Load : 4	25°C	20 Note 4	—	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1D - DYNAMIC CHARACTERISTICS - TS 68000-12

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
15	t <sub>su</sub> (DICL)	Set-up time Data-in to clock low (Note 1)	Fig. 2 Ref. 27	See 5.2.3 (a) to (c) f <sub>c</sub> = 12 MHz	25°C	20	—	ns
					max			
					min			
16	t <sub>su</sub> (SDTCL)	Set-up time $\overline{DTACK}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1D - DYNAMIC CHARACTERISTICS - TS 68000-12 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
17	$t_{su}$ (SBRCL)	Set-up time $\overline{BR}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
18	$t_{su}$ (SBGCL)	Set-up time BGACK low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
19	$t_{su}$ (SVPACL)	Set-up time $\overline{VPA}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
20	$t_{su}$ (SBERCL)	Set-up time $\overline{BERR}$ low to clock low (Note 1)	Fig. 2 Ref. 47	See test 15	25°C	20	—	ns
					max			
					min			
21	$t_w$ (CL)	Clock width low	Fig. 2 Ref. 2	See test 15	25°C	35	125	ns
					max			
					min			
22	$t_w$ (CH)	Clock width high	Fig. 2 Ref. 3	See test 15	25°C	35	125	ns
					max			
					min			
23	$t_{PLH}$ $t_{PHL}$ (CHFCV)	Propagation time clock high to FC valid	Fig. 2 Ref. 6A	See test 15 Load : 3	25°C	—	55	ns
					max			
					min			
24	$t_{PHL}$ (CHSLX)	Propagation time clock high to $\overline{AS}$ low	Fig. 2 Ref. 9	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
26	$t_{PHL}$ (CHSL)	Propagation time CLK high to LDS, UDS low	Fig. 2 Ref. 9	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
27	$t_{PLH}$ (CLSH)	Propagation time CLK low to $\overline{AS}$ high	Fig. 2 Ref. 12	See test 15 Load : 4	25°C	—	50 Note 3	ns
					max			
					min			
28	$t_{PLH}$ (CLSH)	Propagation time CLK low to $\overline{LDS}$ , $\overline{UDS}$ high	Fig. 2 Ref. 12	See test 15 Load : 4	25°C	—	50 Note 3	ns
					max			
					min			
29	$t_{PLH}$ (CHRHX)	Propagation time CLK high to R/W high	Fig. 2 Ref. 18	See test 15 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
30	$t_{PHL}$ (CHRL)	Propagation time CLK high to R/W low	Fig. 3 Ref. 20	See test 15 Load : 4	25°C	—	60 Note 3	ns
					max			
					min			
31	$t_{PZL}$ $t_{PZH}$ (CLDO)	Propagation time CLK low to Data-out valid	Fig. 3 Ref. 23	See test 15 Load : 4	25°C	—	55 Note 3	ns
					max			
					min			
32	$t_{PZL}$ $t_{PZH}$ (CLAV)	Propagation time CLK low to Address valid	Fig. 2 Ref. 6	See test 15 Load : 4	25°C	—	55	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

TABLE 1D - DYNAMIC CHARACTERISTICS - TS 68000-12 (Continued)

Test Nbr	Symbol	Parameter	Ref Nbr (**)	Test Conditions	Test Temp.	Limits		Unit
						Min (*)	Max (*)	
33	t <sub>PHL</sub> (CHGL)	Propagation time CLK high to $\overline{B\overline{G}}$ low	Fig. 4 Ref. 33	See test 15 Load : 3	25°C	—	50	ns
					max			
					min			
34	t <sub>PLH</sub> (CHGH)	Propagation time CLK high to $\overline{B\overline{G}}$ high	Fig. 4 Ref. 34	See test 15 Load : 3	25°C	—	50	ns
					max			
					min			
35	t <sub>PHL</sub> (CLVM)	Propagation time CLK low to VMA low	Fig. 5 Ref. 40	See test 15 Load : 4	25°C	—	70	ns
					max			
					min			
36	t <sub>PHL</sub> (CLE)	Propagation time CLK low to E low	Fig. 5 Ref. 41	See test 15 Load : 4	25°C	—	45	ns
					max			
					min			
38	t <sub>h</sub> (SHAZ)	Hold time CLK high to Address	Fig. 2 Ref. 8	See test 15 Load : 3	25°C	0	—	ns
					max			
					min			
42	t <sub>su</sub> (AVSL)	Set-up time Address valid to $\overline{A\overline{S}}$ , $\overline{L\overline{D\overline{S}}}$ , $\overline{U\overline{D\overline{S}}}$ low	Fig. 2 Ref. 11	See test 15 Load : 4	25°C	0 Note 4	—	ns
					max			
					min			
51	t <sub>PHL</sub> (BRLGL)	Propagation time $\overline{B\overline{R}}$ low to $\overline{B\overline{G}}$ low	Fig. 4 Ref. 35	See test 15 Load : 3	25°C	1.5 —	3.5 + 70	CLKS Note 2 ns
					max			
					min			
53	t <sub>PLH</sub> (GALGH)	Propagation time $\overline{B\overline{G\overline{A\overline{C\overline{K}}}}$ low to $\overline{B\overline{G}}$ high	Fig. 4 Ref. 37	See test 15 Load : 3	25°C	1.5 —	3.5 + 70	CLKS Note 2 ns
					max			
					min			
60	t <sub>su</sub> (BELDAL)	Set-up time $\overline{B\overline{E\overline{R\overline{R}}}}$ low to $\overline{D\overline{T\overline{A\overline{C\overline{K}}}}$ low	Fig. 3 Ref. 48	See test 15	25°C	20 Note 5	—	ns
					max			
					min			
68	t <sub>su</sub> (BELDAL)	Set-up time $\overline{B\overline{E\overline{R\overline{R}}}}$ low to $\overline{D\overline{T\overline{A\overline{C\overline{K}}}}$ low	Fig. 2 Ref. 48	See test 15	25°C	20 Note 5	—	ns
					max			
					min			
72	t <sub>h</sub> (DOSL)	Hold time Data-out valid to $\overline{L\overline{D\overline{S}}}$ , $\overline{U\overline{D\overline{S}}}$ low	Fig. 3 Ref. 26	See test 15 Load : 4	25°C	15 Note 4	—	ns
					max			
					min			

(\*) Algebraic values.

(\*\*) Measurement method : see 5.2.

Referred notes are given in 5.2.4 (before Table 1A).

AC ELECTRICAL SPECIFICATION - CLOCK TIMING (see Figure 8)

Symbol	Parameter	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
f	Frequency of operation	4.0	8.0	4.0	10.0	4.0	12.5	MHz
t <sub>cyc</sub>	Cycle time	125	250	100	250	80	250	ns
t <sub>CL</sub> t <sub>CH</sub>	Clock pulse width	55 55	125 125	45 45	125 125	35 35	125 125	ns
t <sub>Cr</sub> t <sub>Cf</sub>	Rise and fall time	— —	10 10	— —	10 10	— —	10 10	ns

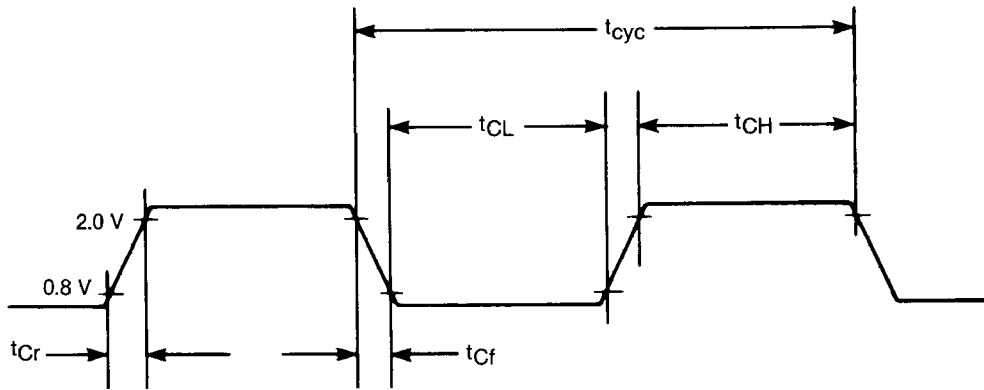
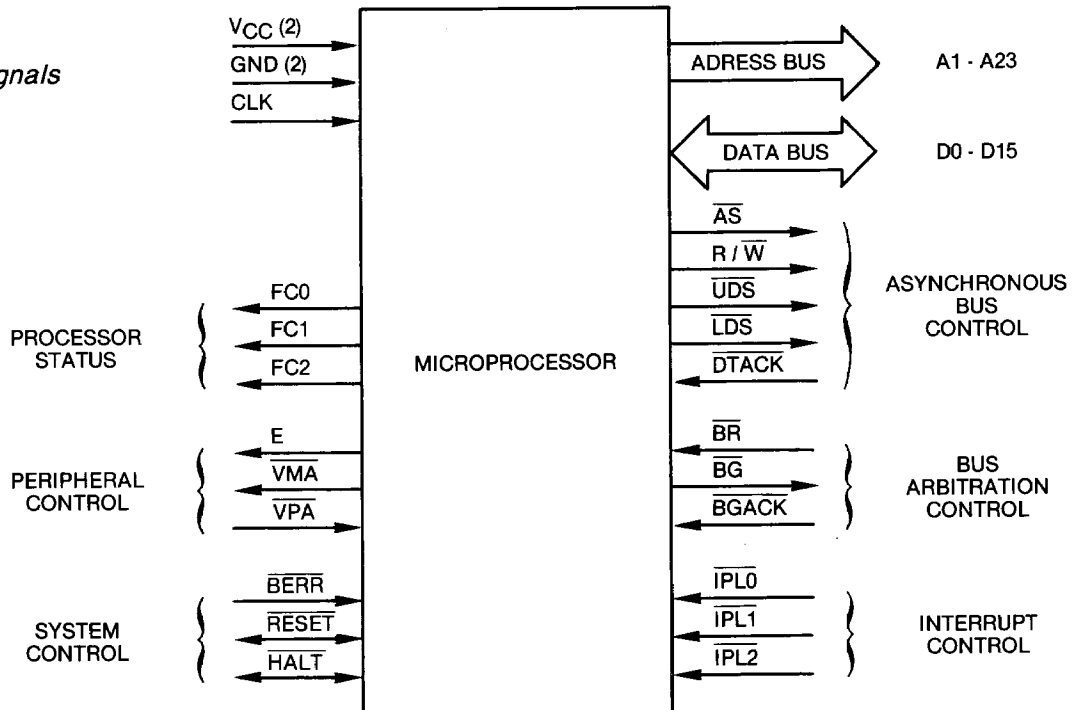


FIGURE 8 - CLOCK INPUT TIMING DIAGRAM.

**Note :** Timing measurements are referenced to and from a low voltage of 0.8 volt and high a voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volt and 2.0 volts.

5.25 - Input & output signals





**6 - PREPARATION FOR DELIVERY**

**6.1 - PACKAGING**

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

**6.2 - CERTIFICATE OF COMPLIANCE**

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperatures for the entire temperature range.

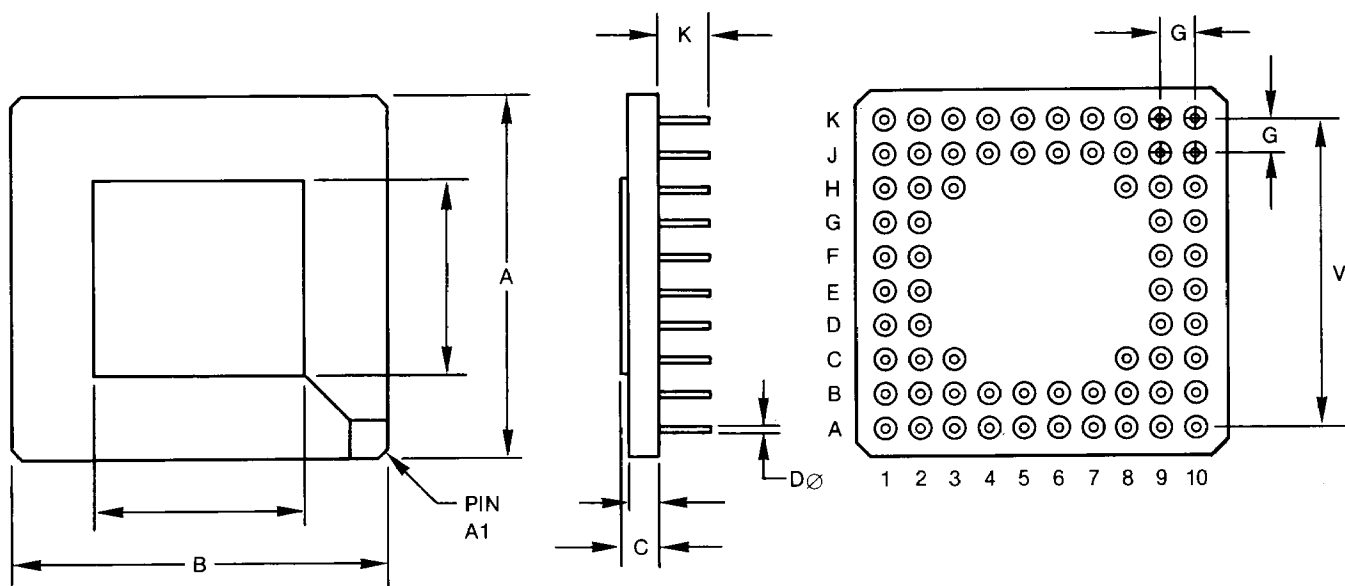
**7 - HANDLING**

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

- a) Device should be handled on benches with conductive and grounded surface.
- b) Ground test equipment, tools and operator.
- c) Do not handle devices by the leads.
- d) Store devices in conductive foam or carriers.
- e) Avoid use of plastic, rubber, or silk in MOS areas.
- f) Maintain relative humidity above 50 %, if practical.

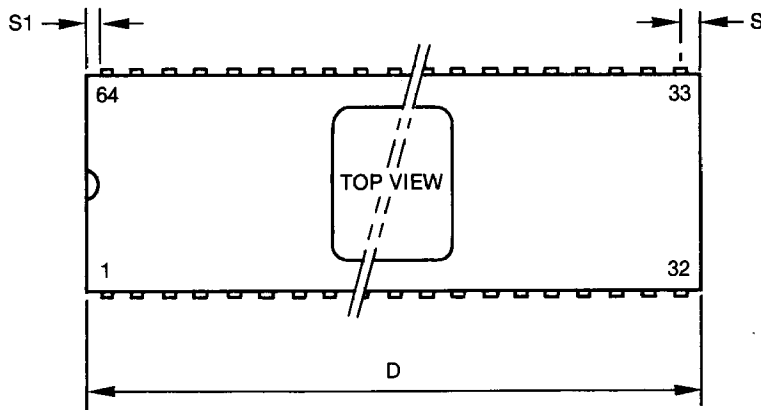
**8 - PACKAGE MECHANICAL DATA**

**8.1 - 68 PINS - PIN GRID ARRAY**

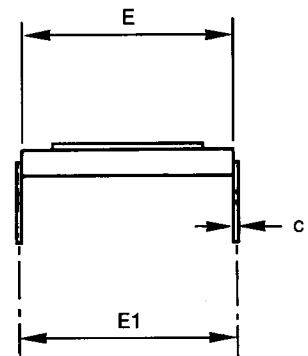
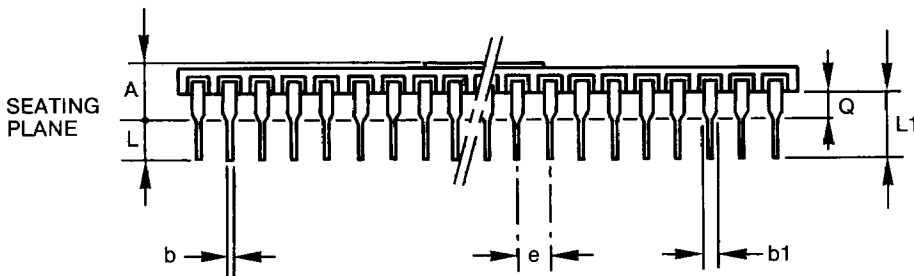


Symbol	Millimeters	
	Min	Max
A	26.41	27.43
B	26.41	27.43
C	1.78	3.68
D $\varnothing$	0.41	0.51
G	2.54 BSC	
K	3.56	4.83
V	22.86 BSC	

8.2 - 64 PINS - CERAMIC DIL



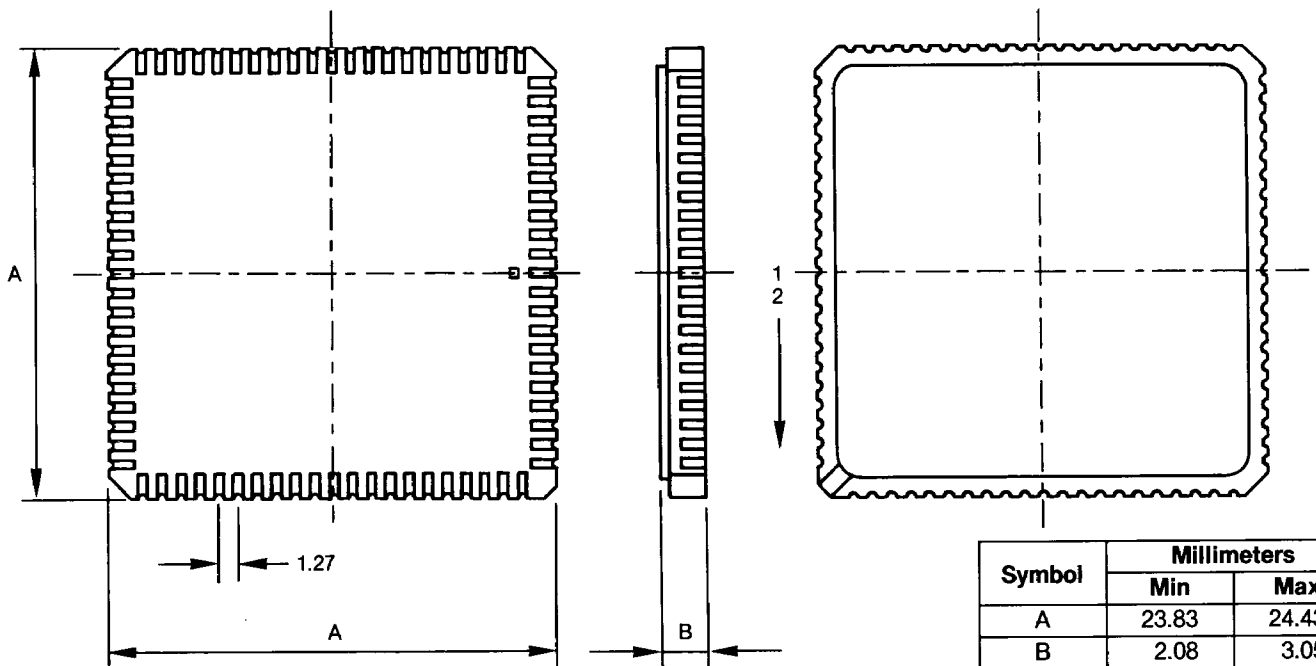
Symbol	Millimeters	
	Min	Max
A	—	5.72
b	0.36	0.58
b <sub>1</sub>	0.96	1.65
c	0.20	0.38
D	—	82.30
E	22.10	23.37
E <sub>1</sub>	22.35	23.88
e	2.54 BSC	
L	3.18	5.08
L <sub>1</sub>	3.81	—
Q	0.38	1.78
S	—	1.78
S <sub>1</sub>	0.13	—



8.3 - 68 PINS - LEADLESS CERAMIC CHIP CARRIER

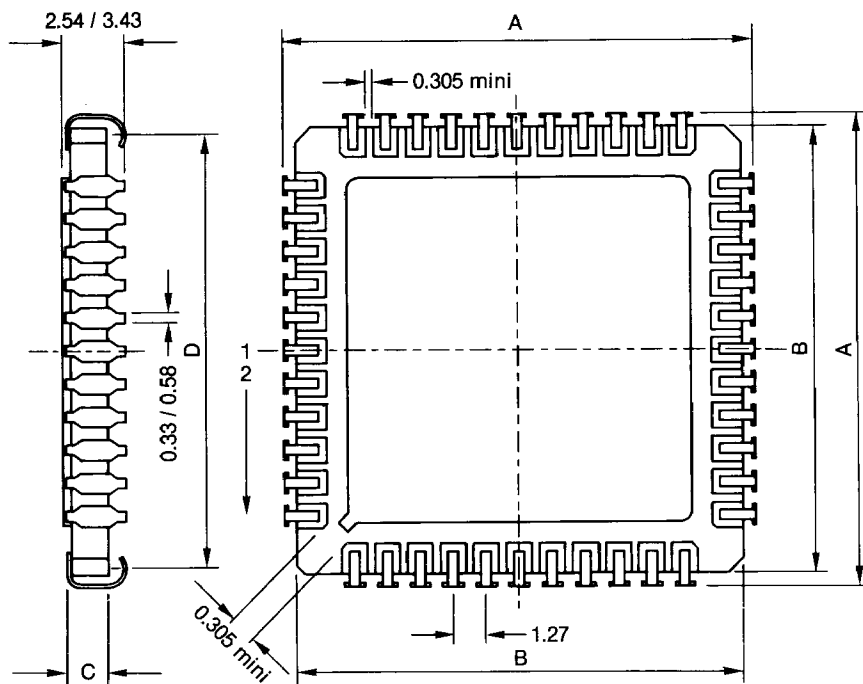
BOTTOM VIEW

TOP VIEW



Symbol	Millimeters	
	Min	Max
A	23.83	24.43
B	2.08	3.05

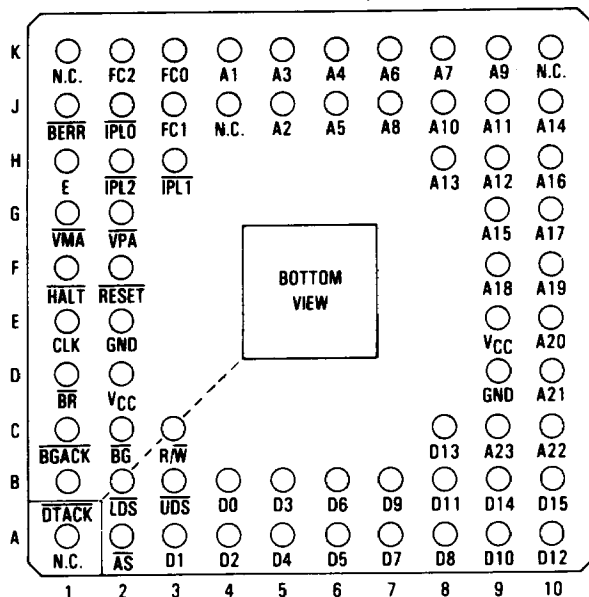
8.4 - 68 PINS - LEADED CERAMIC CHIP CARRIER



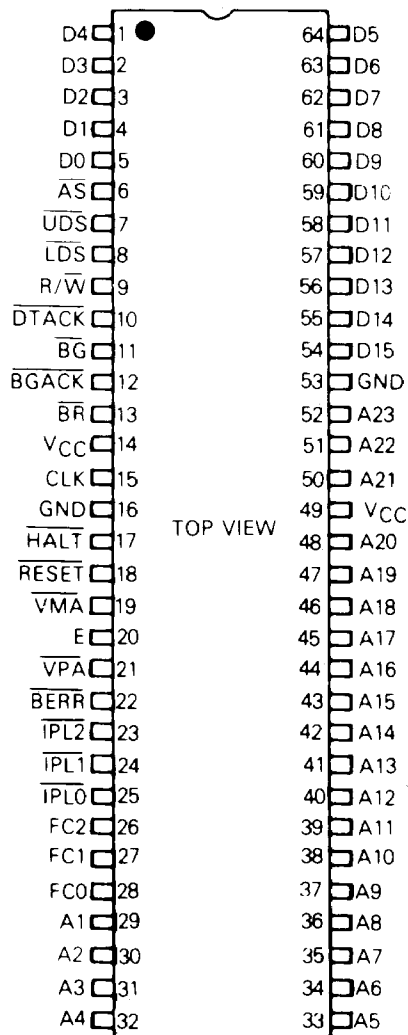
Symbol	Millimeters	
	Min	Max
A	24.89	25.40
B	23.88	24.38
C	2.00	2.51
D	23.11	24.13

9 - TERMINAL CONNECTIONS

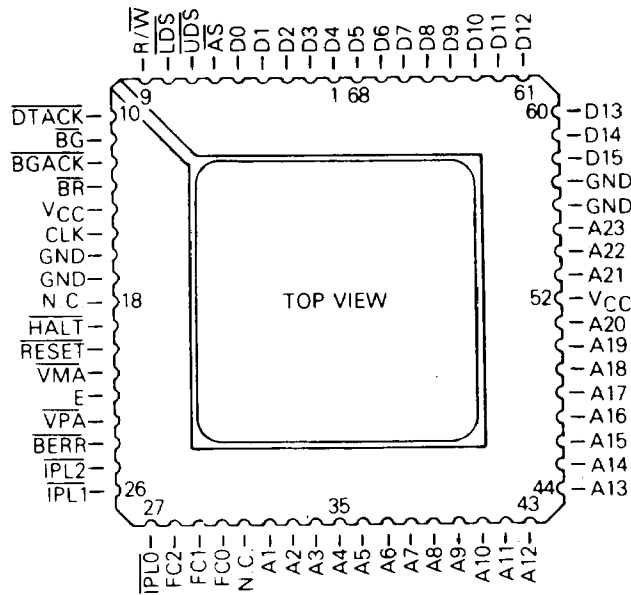
9.1 - 68 PINS - PIN GRID ARRAY



9.2 - 64 PINS - CERAMIC DIL

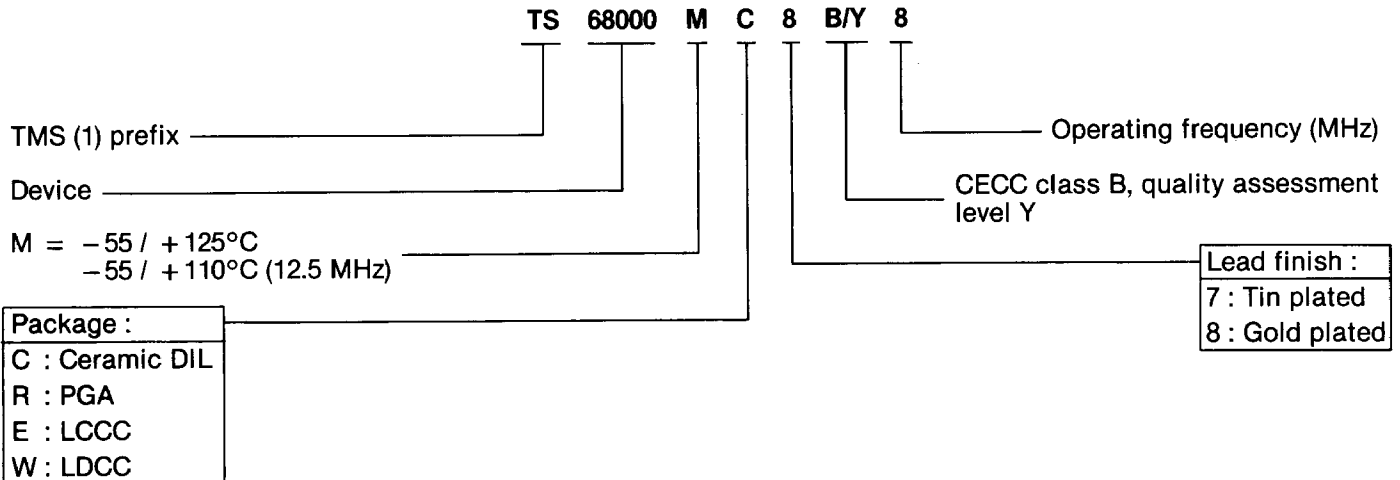


9.3 - 68 PINS - LEADED AND LEADLESS CERAMIC CHIP CARRIER



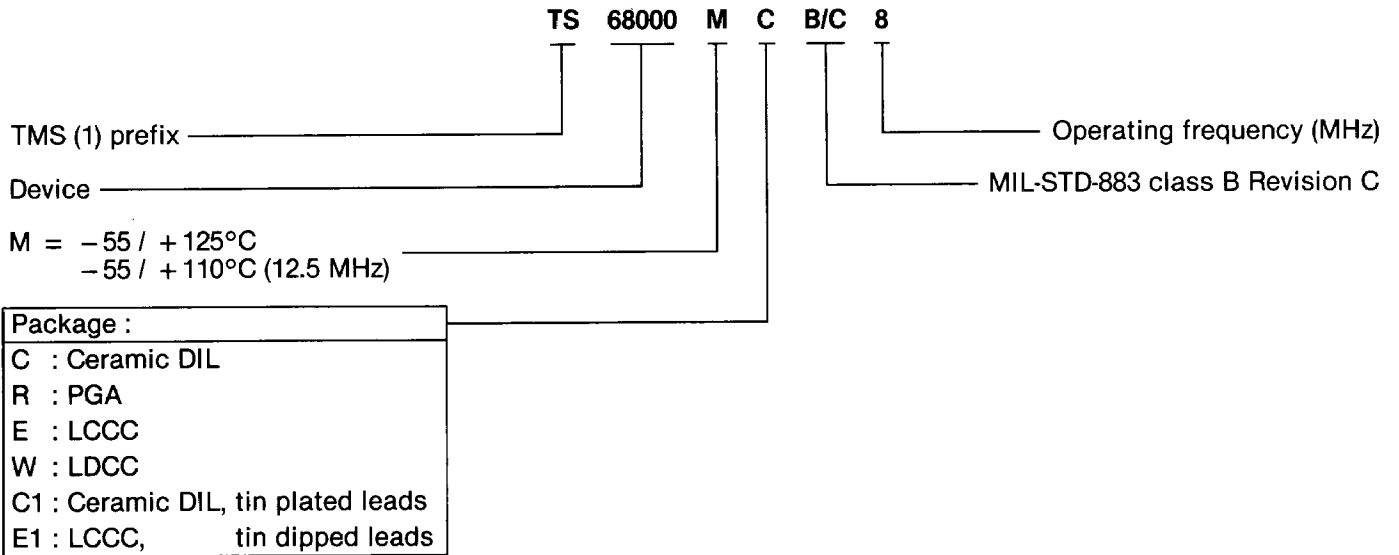
10 - ORDERING INFORMATION

10.1 - CECC (CECC spec number is 90110-001)

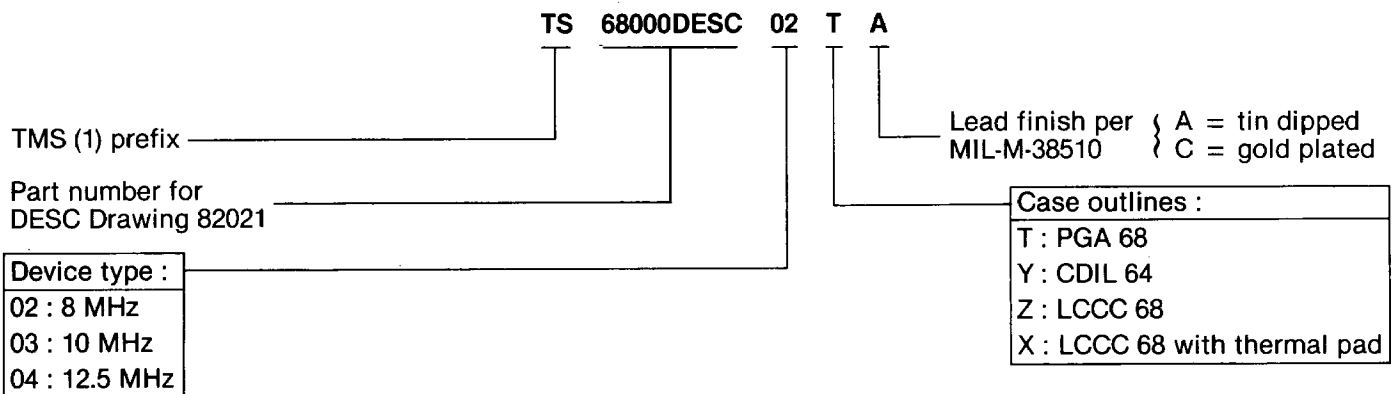


Note : 1 - THOMSON COMPOSANTS MILITAIRES ET SPATIAUX

10.2 - MIL-STD-883



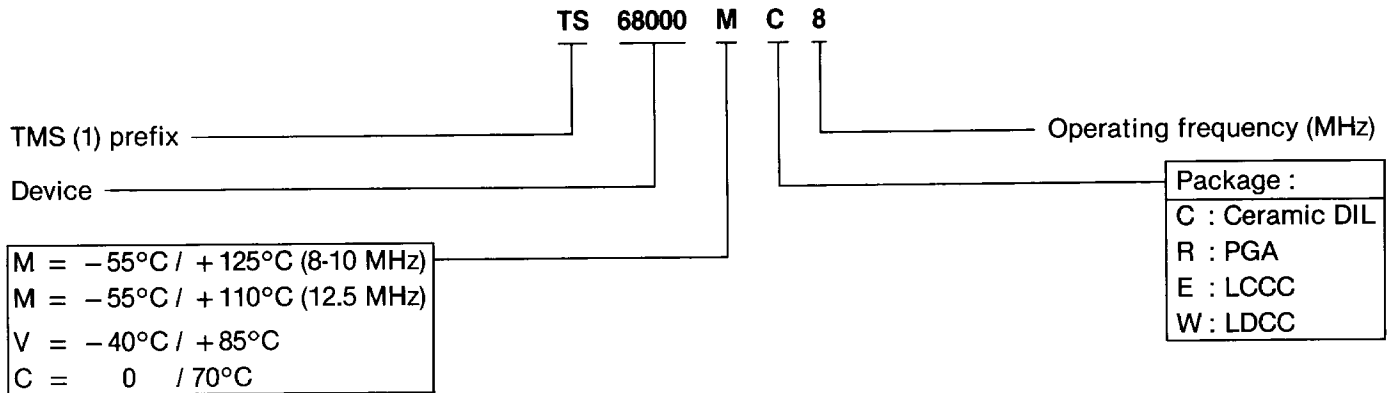
10.3 - DESC



**Attention :** Temperature range is -55 / +110°C for a DESC product.

**Note :** 1 - THOMSON COMPOSANTS MILITAIRES ET SPATIAUX

10.4 - STANDARD PRODUCT



**Note : 1 - THOMSON COMPOSANTS MILITAIRES ET SPATIAUX**

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