SSI 32F8001/8002
Low-Power Programmable Electronic Filter

December 1994

DESCRIPTION

The SSI 32F8001/8002 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation make the SSI 32F8001/8002 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8001/8002 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal. The SSI 32F8001/8002 requires only a +5V supply and are available in 16-lead SON and SOL packages.

FEATURES

- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency (*fc* = 9 to 27 MHz, 32F8001; *fc* = 6 to 18 MHz, 32F8002)**
- **Programmable pulse slimming equalization (0 to 13.5 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **±12% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 *fc* to *fc***
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-Lead SON and SOL package**
- **Pin compatible with SSI 32F8011**

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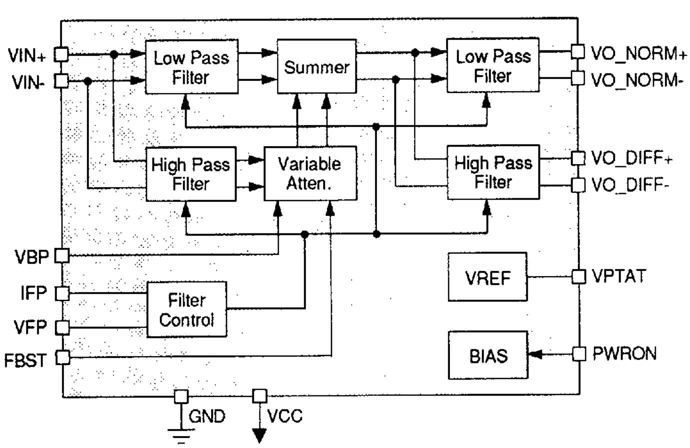
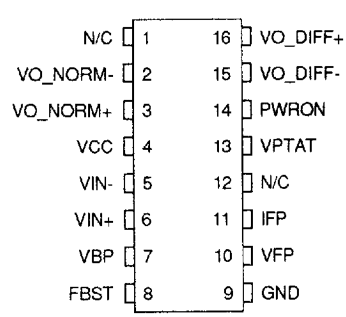
BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8001/8002
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8001/8002 is a high performance programmable electronic filter. It features a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8001 programmable electronic filter can be set to a filter cutoff frequency from 9 to 27 MHz with no boost. The SSI 32F8002 can set the cutoff frequency from 6 to 18 MHz with no boost.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8001/8002 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8001/8002. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the $f c$ and boost circuits.

The cutoff frequency, determined by the -3 dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

$f c$ (ideal, in MHz)

32F8001 = 45.0 • IFP = 45.0 • IVFP • 1.8/VPTAT

32F8002 = 30.0 • IFP = 30.0 • IVFP • 1.8/VPTAT

where IFP and IVFP are in mA, $0.2 < \text{IFP} < 0.6$ mA, VPTAT is in volts, and Ta = 25°C.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8001/8002 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

$f c$ (ideal, in MHz)

32F8001 = 45.0 • IFP = 45.0 • 1.8/(3 • Rx)

32F8002 = 30.0 • IFP = 30.0 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[3.73(\text{VBP}/\text{VPTAT})+1]$, where $0 < \text{VBP} < \text{VPTAT}$.

POWER ON / OFF

The SSI 32F8001/8002 supports a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

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PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency fc, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65°C to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATINGS
Supply voltage	VCC	4.50V < VCC < 5.50V
Ambient Temperature	Ta	0°C < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2V, VCC = 5V		230	300	mW
		PWRON ≥ 2V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW

DC Characteristics

High Level Input Voltage	VIH	TTL input	2			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	µA
Low Level Input Current	IIL	VIL = 0.4V	-1.5			mA

Filter Characteristics

Filter Cutoff Frequency *(*f* -3 dB)	**fc*	32F8001 $fc = \frac{45\ \text{MHz}}{\text{mA}}(\text{IVFP})$ IVFP = 0.2 to 0.6 mA, Ta = 25 °C	9		27	MHz
		32F8002 $fc = \frac{30\ \text{MHz}}{\text{mA}}(\text{IVFP})$ IVFP = 0.2 to 0.6 mA, Ta = 25 °C	6		18	MHz
Filter *fc* Accuracy	FCA	*fc* = max.	-12		+12	%
VO_NORM Diff Gain	AO	F = 0.67 *fc*, FB = 0 dB	0.8		1.2	V/V
VO_DIFF Diff Gain	AD	F = 0.67 *fc*, FB = 0 dB	0.8 AO		1.2 AO	V/V
Frequency Boost at *fc*	FB	VBP = VPTAT *fc* = max.	12	13.5	15	dB
		fc = min.	11.5	13	14.5	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 1.0 *fc* = max.	-1.5		+1.5	dB

FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Group Delay Variation Without Boost TGDO	fc = max., $\frac{VBP}{VPTAT}=0$ 8001	-500		+500	ps
	F = 0.2 fc to fc 8002	-750		+750	ps
	fc = min., $\frac{VBP}{VPTAT}=0$ 8001	-1.5		+1.5	ns
	F = 0.2 fc to fc 8002	-2.25		+2.25	ns
Group Delay Variation Without Boost (continued) TGDO	F = 0.2 fc to fc $\frac{VBP}{VPTAT}=0$	-2		2	%
	F = fc to 1.75 fc $\frac{VBP}{VPTAT}=0$	-4		+4	%
Group Delay Variation with Boost TGDB	fc = max, VBP = VPTAT	-500		+500	ps
	F = 0.2 fc to fc	-750		+750	ps
	fc = min., VBP = VPTAT	-1.5		+1.5	ns
	F = 0.2 to fc	-2.25		+2.25	ns
	F = 0.2 fc TO fc, VBP = VPTAT	-2.5		+2.5	%
	F = fc to 1.75 fc, VBP = VPTAT	-4		+4	%
Filter Input Dynamic Range VIF	THD = 1% max, F = 0.67 fc, VBP = 0V (1000 pF across Rx)	1			Vp-p
	THD = 1.7% max, F = 0.67 fc, VBP = 0V, Normal output (1000 pF across Rx)	1.5			Vp-p
Filter Input Dynamic Range VIF	THD = 3.5% max, F = 0.67 fc, VBP = 0V, Differentiated output (1000 pF across Rx)	1.5			Vp-p
Filter Output Dynamic Range VOF	THD = 1% max, F = 0.67 fc R_{LOAD} ≥ 1kΩ (1000 pF across Rx)	1			Vp-p
Filter Diff Input Resistance RIN		3	4.3		kΩ
Filter Input Capacitance CIN				3	pF
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω 8001		3.5	5.4	mVRms
	fc = max, VBP = 0V 8002		3.3	5.2	mVRms
Output Noise Voltage EOUT Normal Output	BW = 100 MHz, Rs = 50Ω 8001		2.3	3.45	mVRms
	fc = max, VBP = 0V 8002		2.1	3.15	mVRms
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω 8001		7.7	10.75	mVRms
	fc = max, VBP = VPTAT 8002		4.8	7	mVRms
Output Noise Voltage EOUT Normal Output	BW = 100 MHz, Rs = 50Ω 8001		3.8	4.75	mVRms
	fc = max, VBP = VPTAT 8002		2.6	3.3	mVRms

ELECTRICAL SPECIFICATIONS (continued)

FILTER CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Output Sink Current IO –		1			mA
Filter Output Source Current IO +		2			mA
Filter Output Resistance (Single ended) RO	IO+ = 1.0 mA			60	Ω
Reference Voltage VPTAT	Tj = 25°C		1.8		V
PTAT Voltage Input VFP			2/3 VPTAT		V
Programming Current Range IVFP	Ta = 25°C	0.2		0.6	mA
Programming Voltage Range V_{VBP}		0		VPTAT	V
Voltage at pin IFP V_{IFP}	I_{VFP} = 0 mA		2/3 VPTAT		V
Power Up Time	*fc* = 9 MHz			1.5	µs
	fc = 27 MHz			1	µs
Power Down Time				1	µs

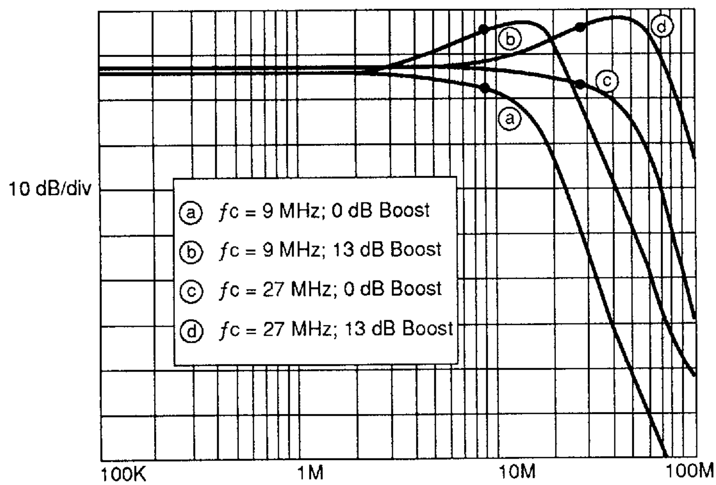

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FIGURE 1: 32F8001 Normal Low Pass Response

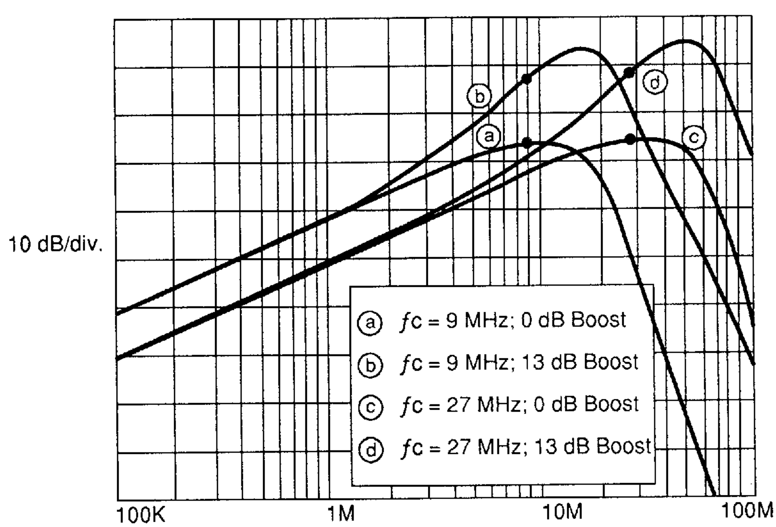


FIGURE 2: 32F8001 Differentiated Low Pass Response

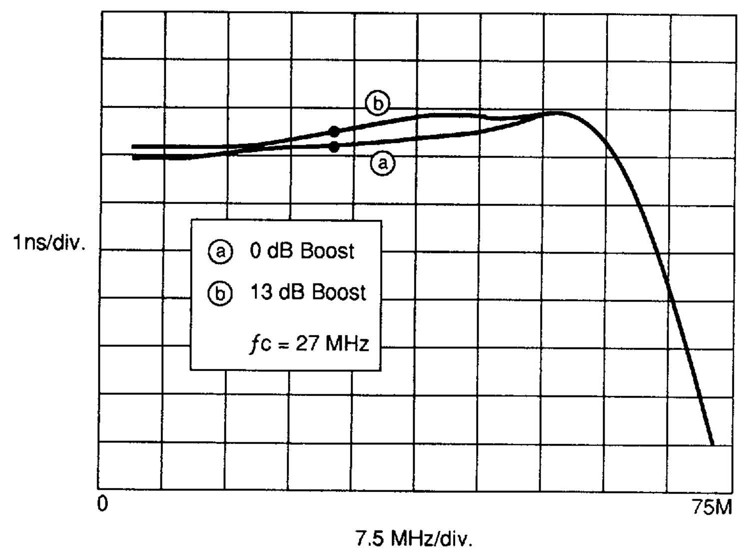
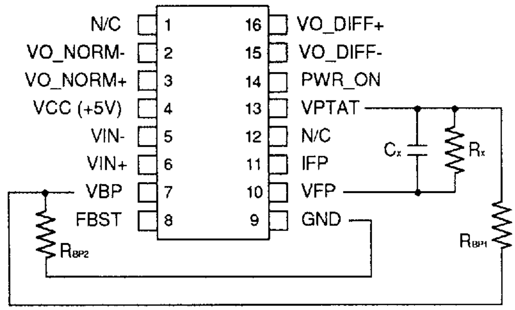


FIGURE 3: 32F8001 Group Delay Response with fc = 27 MHz



VPTAT = 1.8V (25°C)

V_{VFP} = 2/3 (VPTAT)

IVFP range: 0.2 mA to 0.6 mA @25°C

(9 to 27 MHz no boost 32F8001)

(6 to 18 MHz no boost 32F8002)

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \cdot \frac{1}{R_X}$

i.e., fc = 27 MHz then

IVFP = 0.6 mA @25°C Rx = 1 kΩ

Fixed boost programming is also accomplished as shown above. In this case V_{VBP} is set by a voltage divider, where V_{VBP} is a fraction of VPTAT.

i.e., boost = 9 dB then,

VBP/VPTAT = 0.488 9 dB = 20 log [3.73 (0.488) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 0.953$$

Cx = 1000 pF - Cx is needed for lower THD at lower fc.

FIGURE 4: 32F8001/8002 Applications Setup

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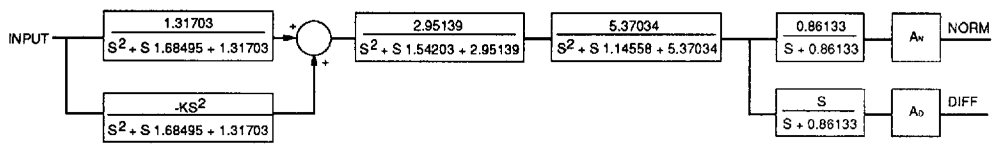

Normalized for $\omega c = (2\pi)\, fc = 1$
AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for fc = 27 MHz, $S = S / [(2\pi)(27 \times 10^6)]$

FIGURE 5: 32F8001/8002 Normalized Block Diagram

TABLE 1: 32F8001/8002 Frequency Boost Calculations, K = 1.31703 (10 BOOST (dB)/20 - 1)

Assuming 13 dB boost for VBP = VPTAT

$$\frac{VBP}{VPTAT} \cong \frac{\left(10^{(FB/20)}\right) - 1}{3.73}$$

Boost	K	VBP / VPTAT	Boost	K	VBP / VPTAT
1 dB	0.16	0.033	6 dB	1.31	0.267
2 dB	0.34	0.069	7 dB	1.63	0.332
3 dB	0.54	0.110	8 dB	1.99	0.405
4 dB	0.77	0.157	9 dB	2.40	0.488
5 dB	1.03	0.209	10 dB	2.85	0.580
			11 dB	3.36	0.683
			12 dB	3.43	0.799
			13 dB	4.57	0.929

or,

$$\text{boost in dB} = 20 \log \left[3.37 \left(\frac{VBP}{VPTAT}\right) + 1\right]$$

VBP / VPTAT	Boost	VBP / VPTAT	Boost
0.1	2.753 dB	0.6	10.206 dB
0.2	4.841 dB	0.7	11.153 dB
0.3	6.523 dB	0.8	12.006 dB
0.4	7.391 dB	0.9	12.784 dB
0.5	9.142 dB	1.0	13.5 dB

TABLE 2: Calculations

Typical change in ƒ-3 dB point with boost

Boost (dB)	Gain@ƒc (dB)	Gain@ peak (dB)	ƒpeak/ƒc	ƒ-3dB/ƒc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87
14	11	13.06	1.53	2.93

Notes:
1. ƒc is the original programmed cutoff frequency with no boost
2. ƒ-3 dB is the new -3 dB value with boost implemented
3. ƒpeak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., ƒc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then ƒ-3 dB = 19.8 MHz
ƒpeak = 11.07 MHz

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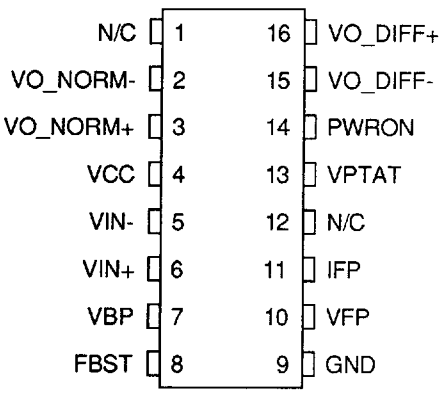
PACKAGE PIN DESIGNATIONS
(Top View)



16-Lead SON, SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

THERMAL CHARACTERISTICS: θja

16-Lead SON (150 mil)	105°C/W
16-Lead SOL (300 mil)	100°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8001		
16-Lead SOL	32F8001-CL	32F8001-CL
16-Lead SON	32F8001-CN	32F8001-CN
SSI 32F8002		
16-Lead SOL	32F8002-CL	32F8002-CL
16-Lead SON	32F8002-CN	32F8002-CN

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